Wojciech.Dulinski@ires.in2p3.fr

Status of Vertical Integration and plans for medium-size pixel tracker based on heterogeneous CMOS layers

Outline

- Vertical Integration: definitions
- Technology choice
- Architecture and simulation results of the proposed device
- Conclusions and future plans

Wojciech.Dulinski@ires.in2p3.fr

Vertical Integration (3D electronics) is generally referred as a technology to fabricate an electronics device (chip) comprised of 2 or more layers of active semiconductor devices that have been thinned, bonded, and interconnected to form a "monolithic" circuit.

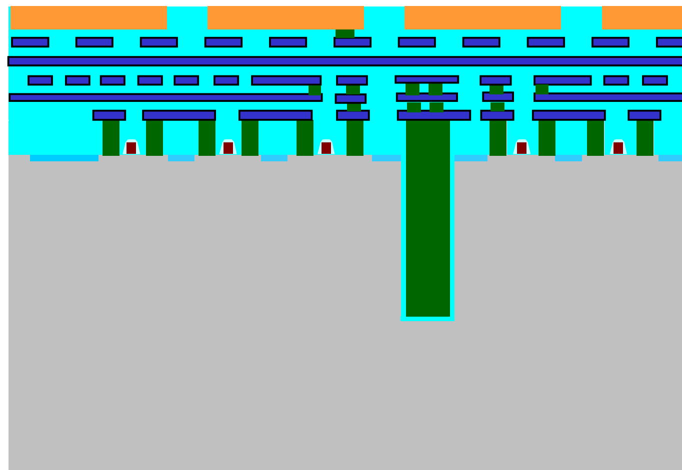
Often the layers (sometimes called tiers) are fabricated in different processes and each layer can be individually optimized for different task (sensor layer, analog processing layer, digital layer, optoelectronics layer).

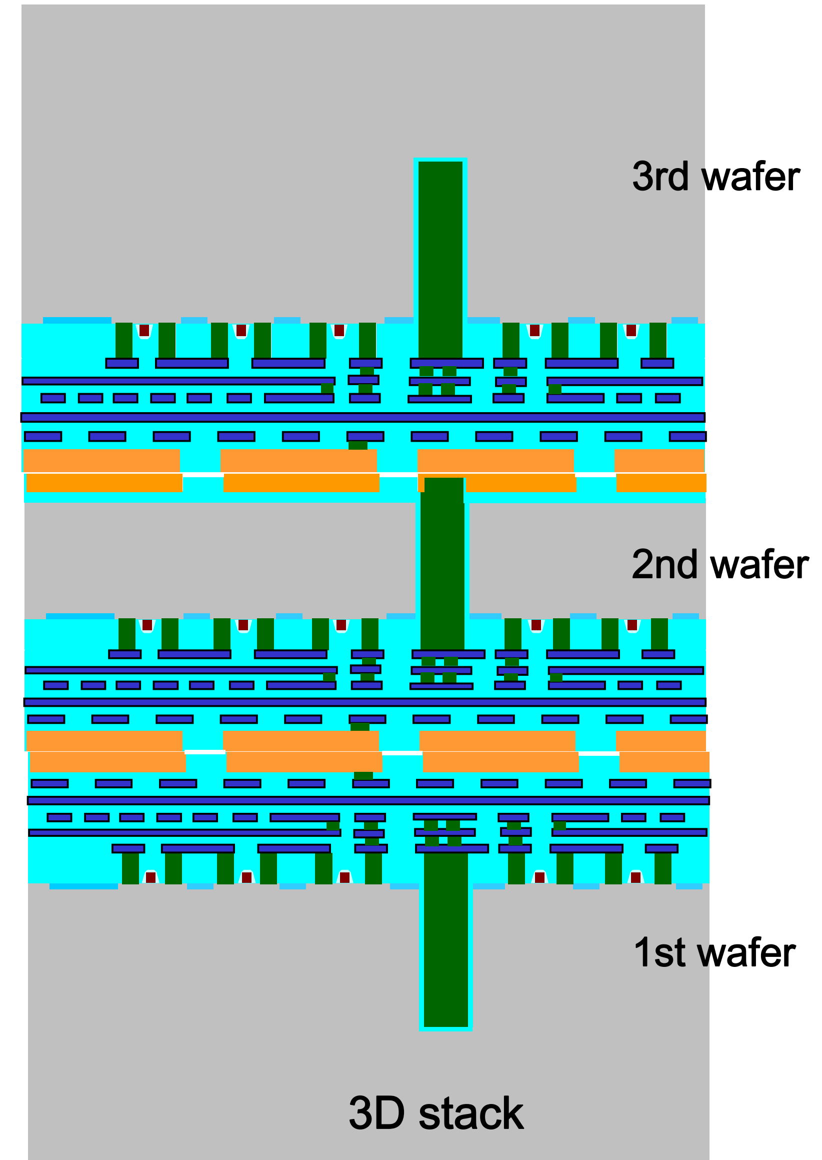
Industry is moving toward 3D to improve circuit performance (limited by interconnect): speed, power consumption, complexity. This approach is also extremely promising for a new generation of 'monolithic' sensors…

Wojciech.Dulinski@ires.in2p3.fr

Key technologies for Vertical Integration Process

-Wafer thinning (down to ~10 microns)
- High precision wafer alignment followed by wafer-to-wafer (or chip-to-wafer) bonding using various techniques: oxide bonding, metal-metal thermo-compression or fusion,..
- Layer-to-layer electrical interconnection using metal-filled, <u>through-silicon vias (TSV)</u>


1st wafer with integrated TSV



3D stack

Wojciech.Dulinski@ires.in2p3.fr

For our first exercise with Vertical Integration using heterogeneous CMOS wafers, we propose MAPS on high-resistivity (depleted) epitaxial substrate with first stage buffer amplifier on the sensor wafer, 3D-coupled to the rest of readout electronics implemented on top of each pixel. This approach removes most of existing limitations of standard (planar) MAPS, still keeping most of their advantages.

Goals for the first prototype:

Speed: frame readout time <<10µs and/or time resolution of ~100 ns

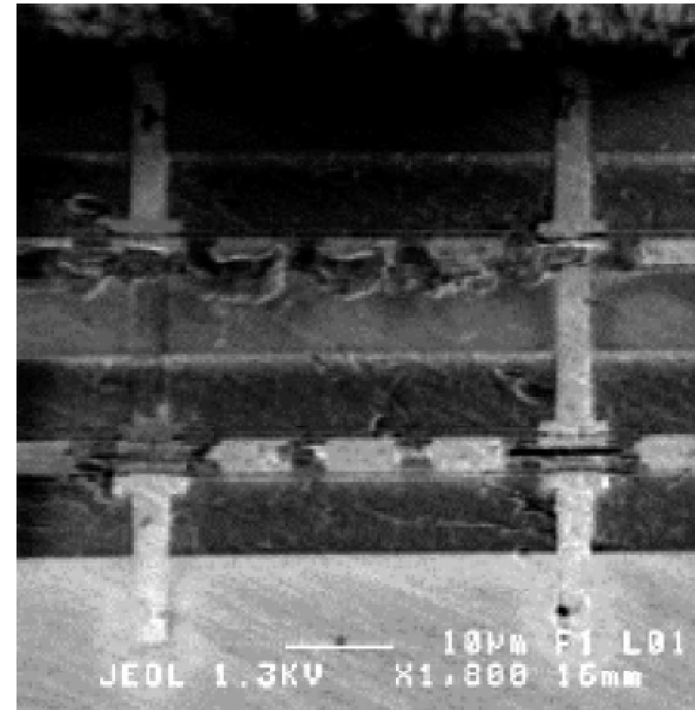
High precision: pixel pitch <20 µm, spatial resolution ~2-3µm

Radiation tolerant: > 10^{14} n/cm^2

Ultra thin: ~50-100 µm (Si equivalent)

Wojciech.Dulinski@ires.in2p3.fr

Technology choice: industrial (or close to) 3-D integration process, with a standard use of TSV (through-silicon-vias)



Example from Tezzaron*: two or more stacked wafers (tiers). Typical interconnection pitch < 5 µm, typical TSV Cp < 5 fF, typical TSV Rs < 0.5 Ω, typical interconnecting metal fill factor ~30%.

*** B.Patti, Proc.IEEE Vol.94, No. 6, June 2006**

Wojciech.Dulinski@ires.in2p3.fr

3-D integration technology is offered by Tezzaron/Chartered as a standard technology (similar constrains as for VLSI submission), but limited (at least for us as a small user) to one CMOS process (0.13 microns)

To bond our wafers from another CMOS supplier (XFAB OPTO PIN, well suited for the sensor layer) we plan to use another 3D-integration semi-industrial process: DBI® (Direct Bond Interconnect) from Ziptronix or Micro-bump bonding from ZyCube ®

Wojciech.Dulinski@ires.in2p3.fr

Integration process flow

3-D wafer integration offered by Tezzaron/Chartered (3DIC Consortium)

- similar constrains as for VLSI chip submission
- 0.13 microns CMOS process
- through-silicon vias (TSV) fabrication included in FEOL (via first approach)
- direct metal-metal thermo compression for wafer-to-wafer bonding

DBI® (Direct Bond Interconnect) from Ziptronix

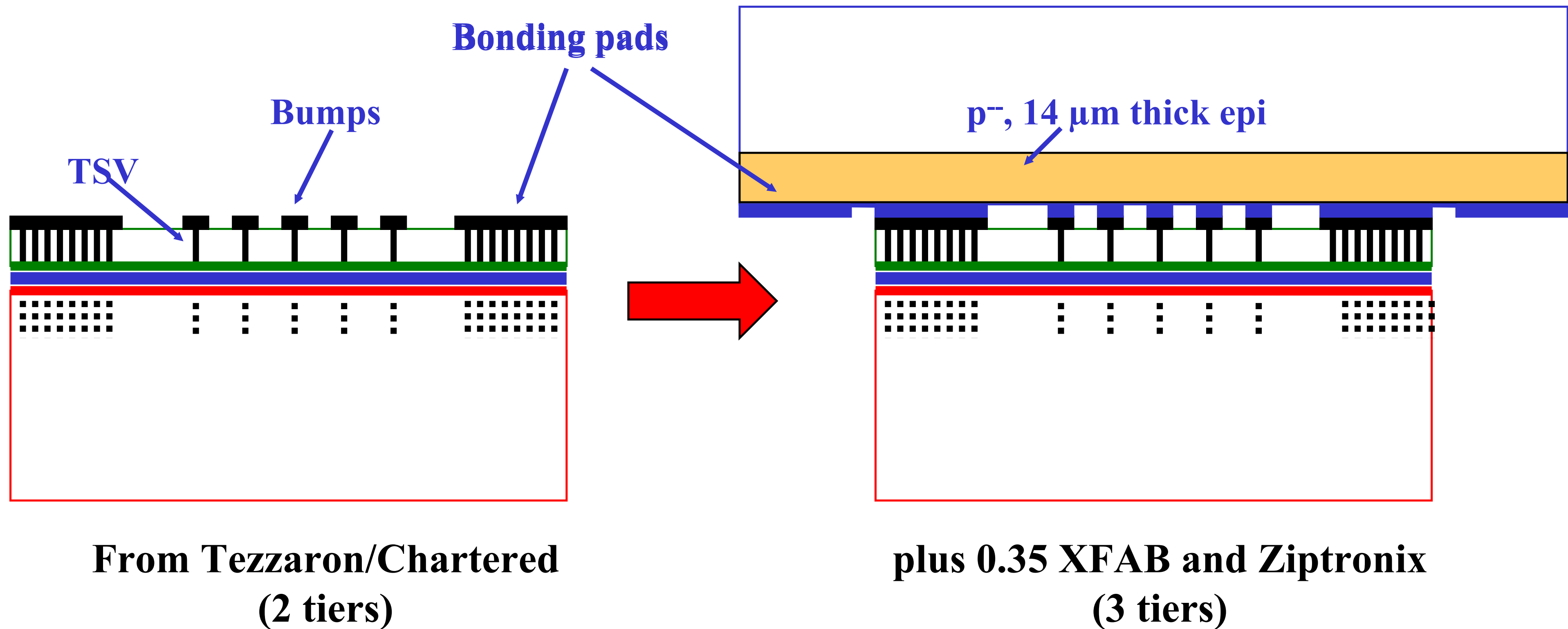
- Low Temperature CMOS Compatible Direct Oxide Bonding
- Highest Density 3D Interconnections (<1µm pitch possible)
- very low mass (>95% of bond area is silicon oxide)
- mechanically stronger than silicon, allowing for consecutive wafer thinning
- seems to be directly compatible with any modern CMOS BEOL process having W-plugs and CMP planarization steps

Alternative solution to DBI® : ZyCube micro-bump bonding

- better tolerance to wafers topography and surface quality
- chip-to-chip bonding possible, as well as further sensor thinning

Wojciech.Dulinski@ires.in2p3.fr

Integration flow, first stage: 3D stacking



Wafer view at intermediate and after final stage (Tezzaron/Chartered chip-to-XFAB wafer bonding)

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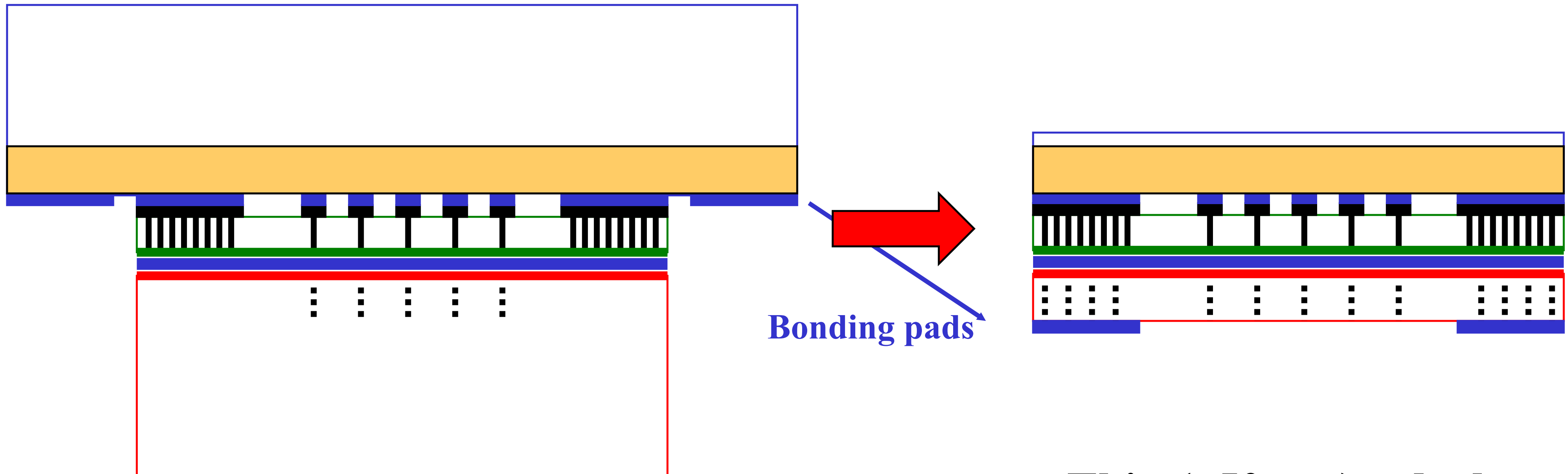
Integration flow, second stage: thinning down to ~50 µm



XFAB and 2xChartered (3 tiers, first stage)

Thin (~50 µm), edgeless final sensor

Packaging problem: how to handle, interconnect and at the end built a ladder with such a thin device?

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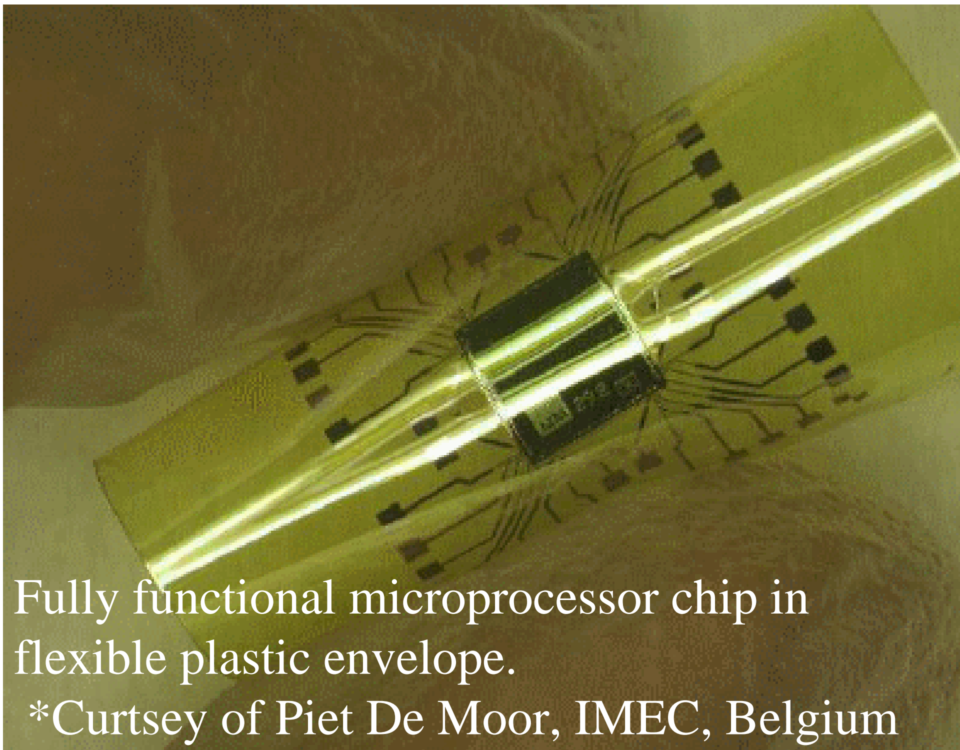
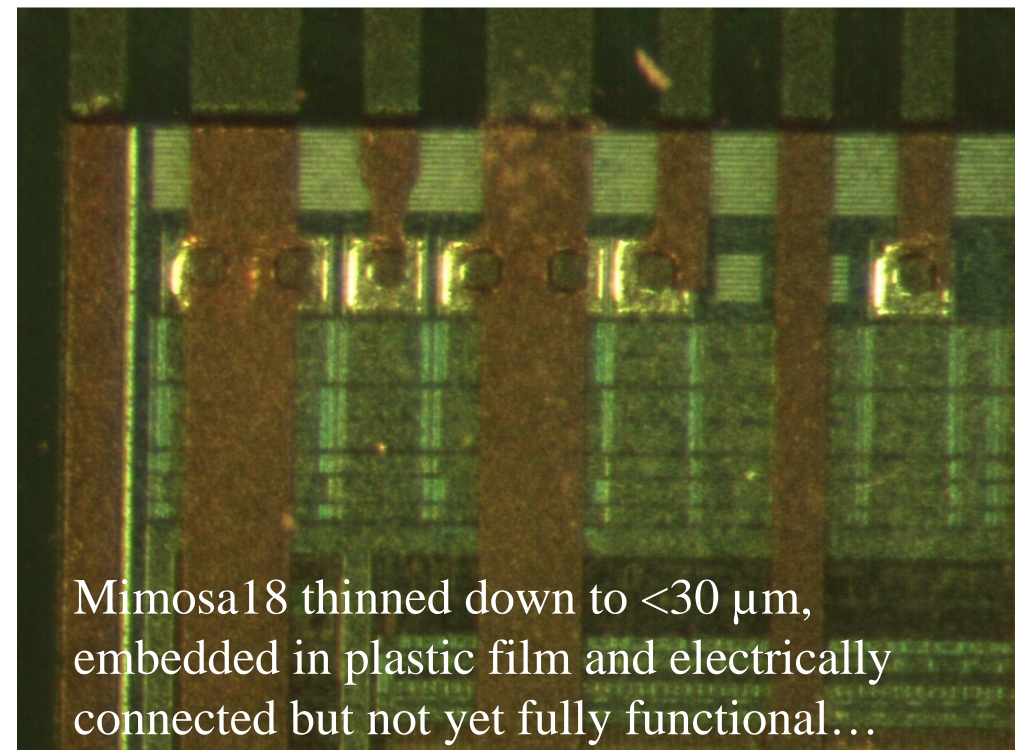
Possible solution: embedding in thin flexible substrate (BCB, silicone, polyamide). Chip interconnect at bond pad level using electroplated Cu. No wire bonding!



Fully functional microprocessor chip in flexible plastic envelope.
*Curtsey of Piet De Moor, IMEC, Belgium



Mimosa18 thinned down to <30 μm, embedded in plastic film and electrically connected but not yet fully functional…

Solution for a cylindrical vertex detector layer?
Subject of on-going study using standard (planar) MAPS…

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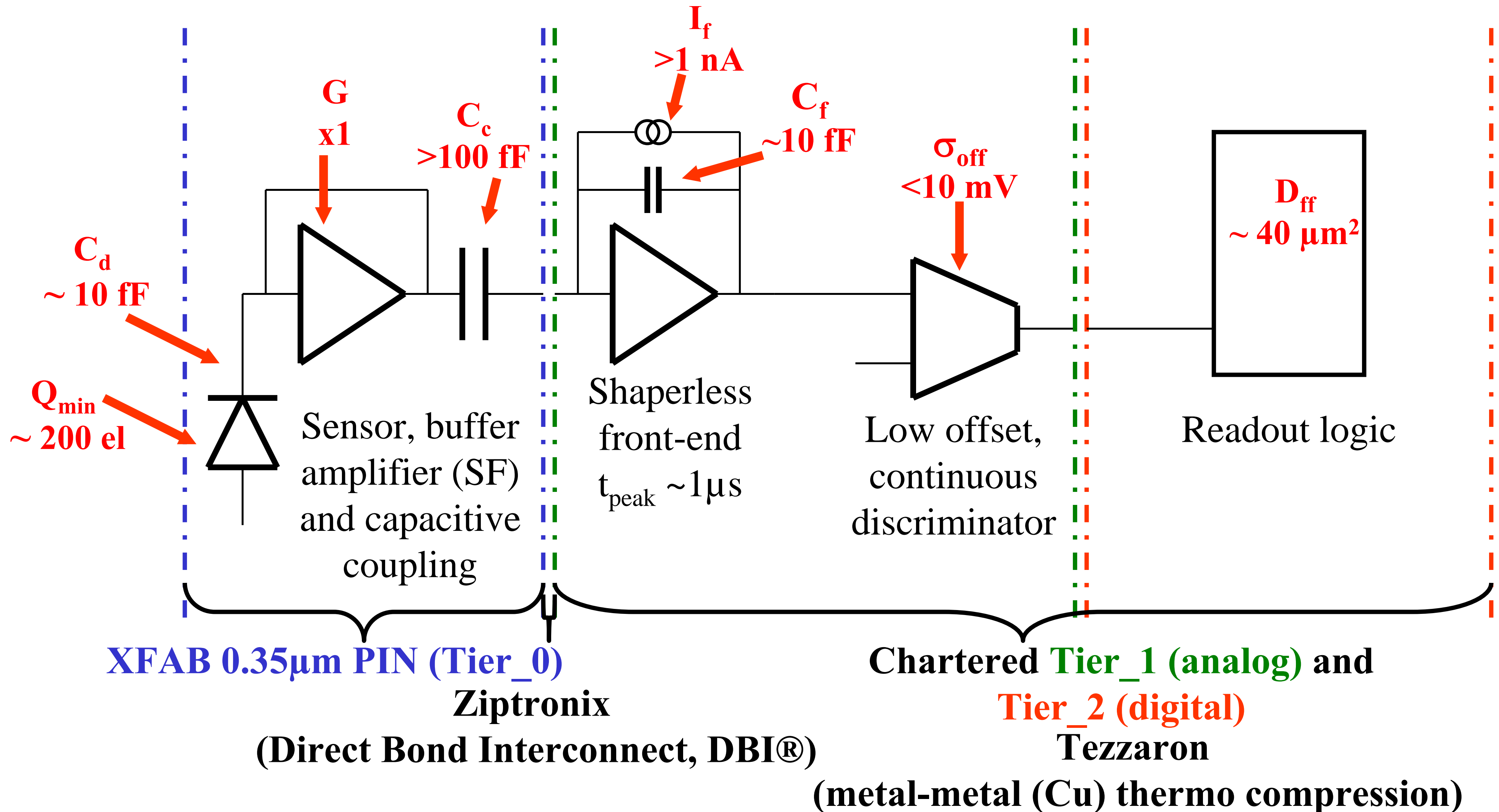
Block diagram of Self Triggering Pixel Strip-like Tracker (STriPSeT)



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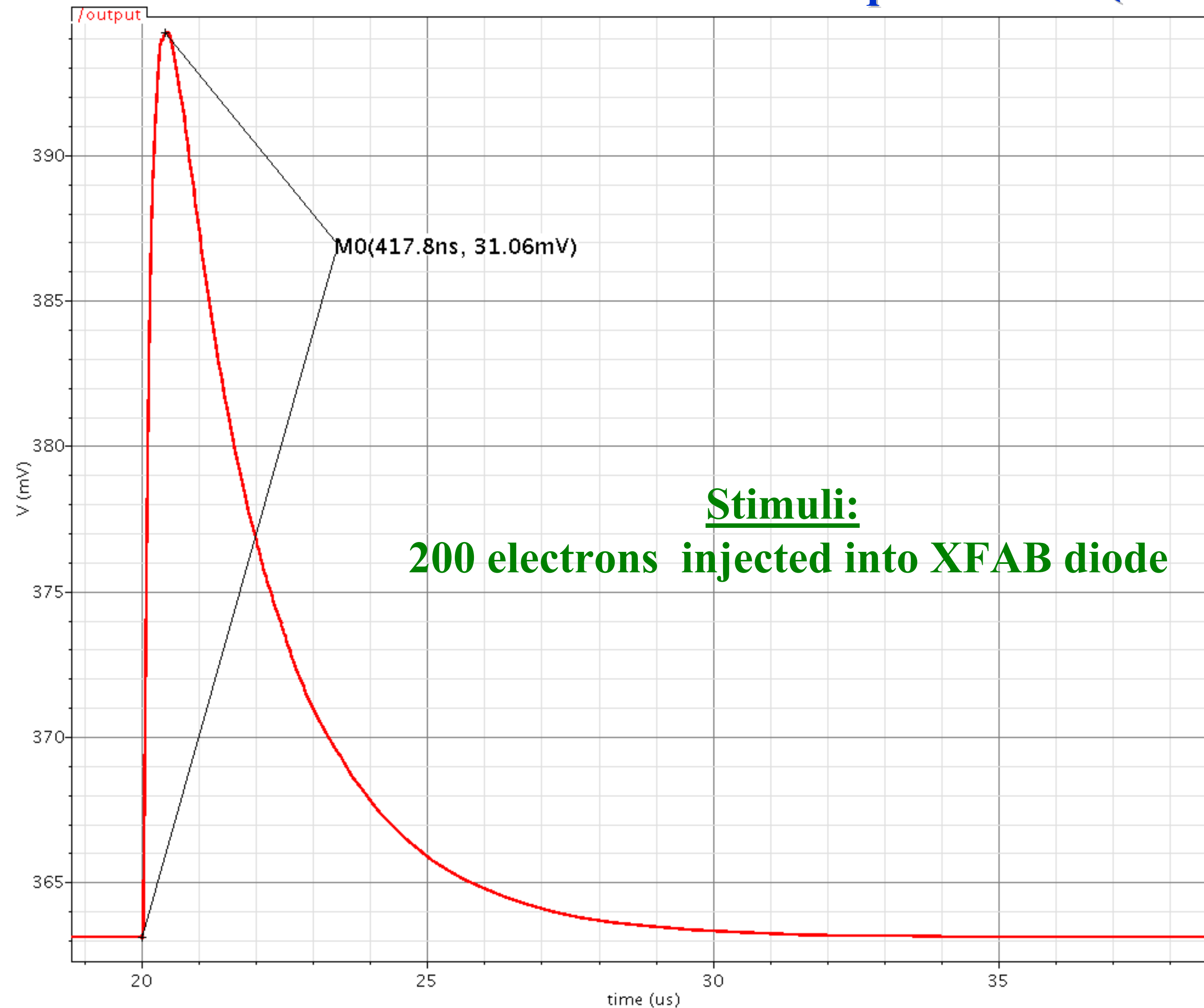
Combined simulation XFAB+Charterer (SF+ShaperlessFE)
Two versions of SFE: C_f=11 fF (MiM) and 5.5 fF (VPP)



Stimuli:

200 electrons injected into XFAB diode

Results:

Peaking time ~400 ns

Gain: ~150µV/el (300 µV/el)

ENC ~12 electrons

Time walk ~200 ns

Power: ~ 5µW/pixel

With a high-res epi substrate for a sensor layer we expect:

S/N_{Landau}>50

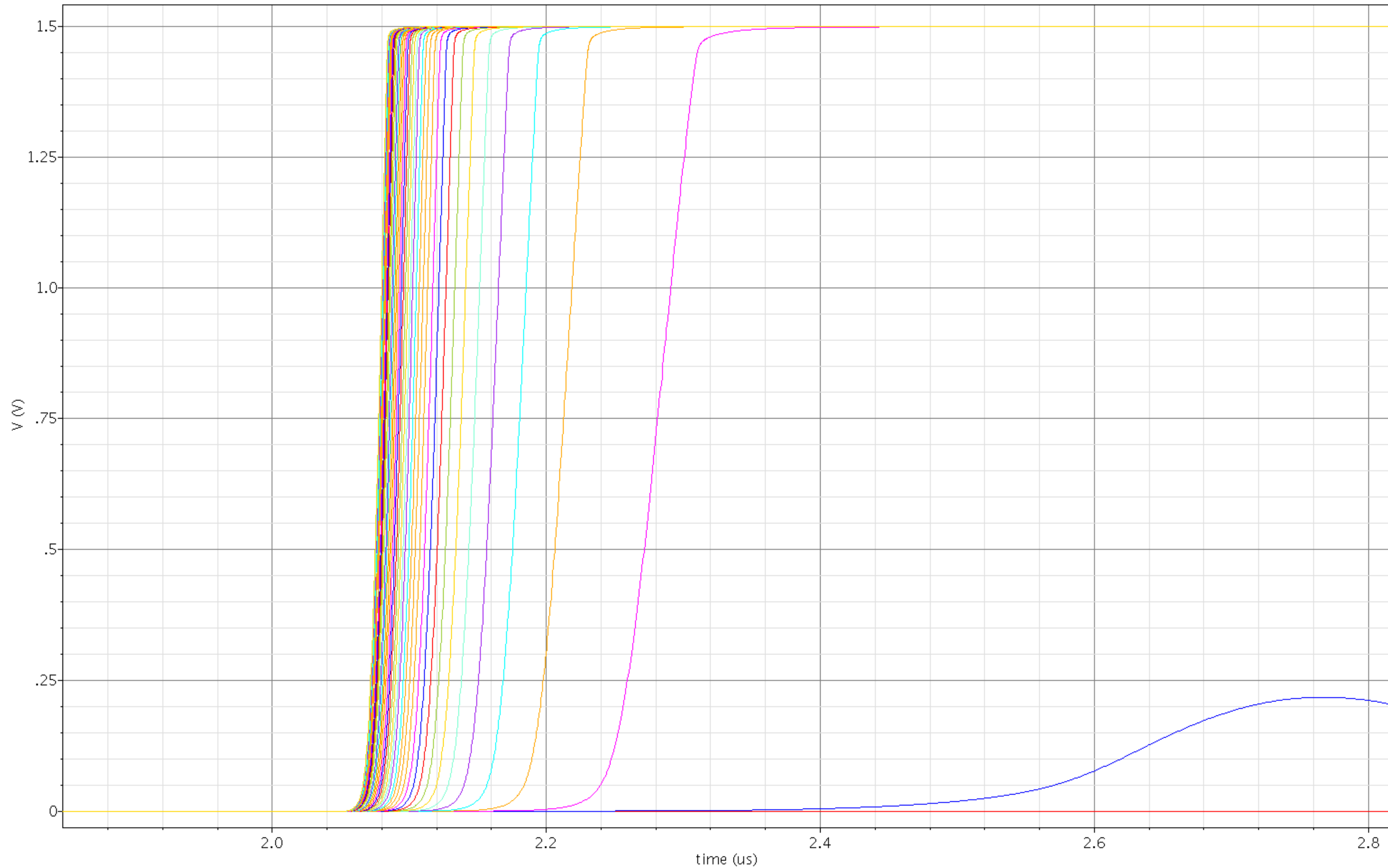
and

$Cut_{\sim 100\%eff}$/Noise>10

Wojciech.Dulinski@ires.in2p3.fr

Combined simulation XFAB+Charterer (SF+ShaperlessFE)

Time-walk of the comparator output : 100-4000 electrons (step 100 e); thr. ~150 e



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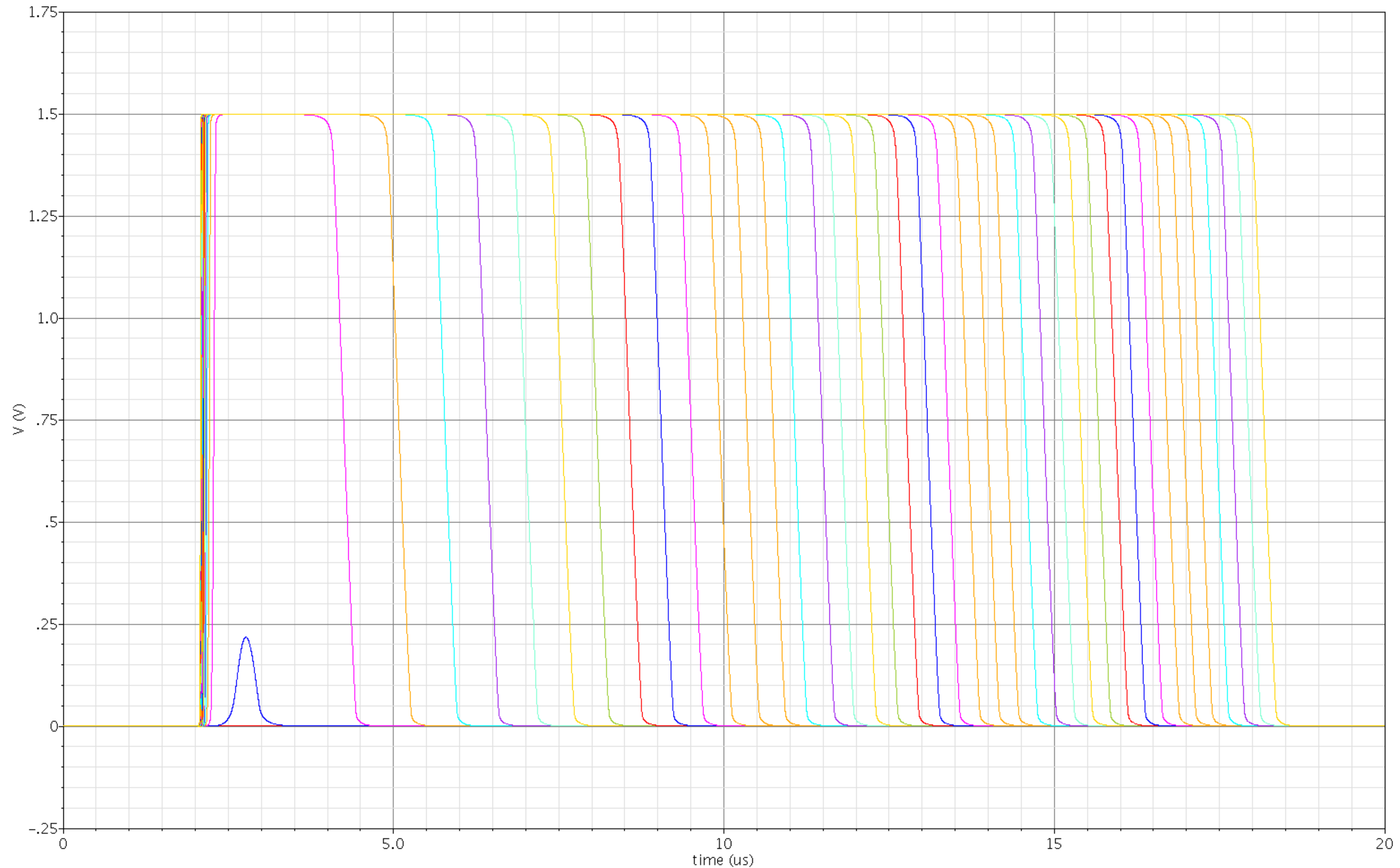
Combined simulation XFAB+Charterer (SF+ShaperlessFE)

Comparator output : 100-4000 electrons (step 100 e); threshold ~150 e



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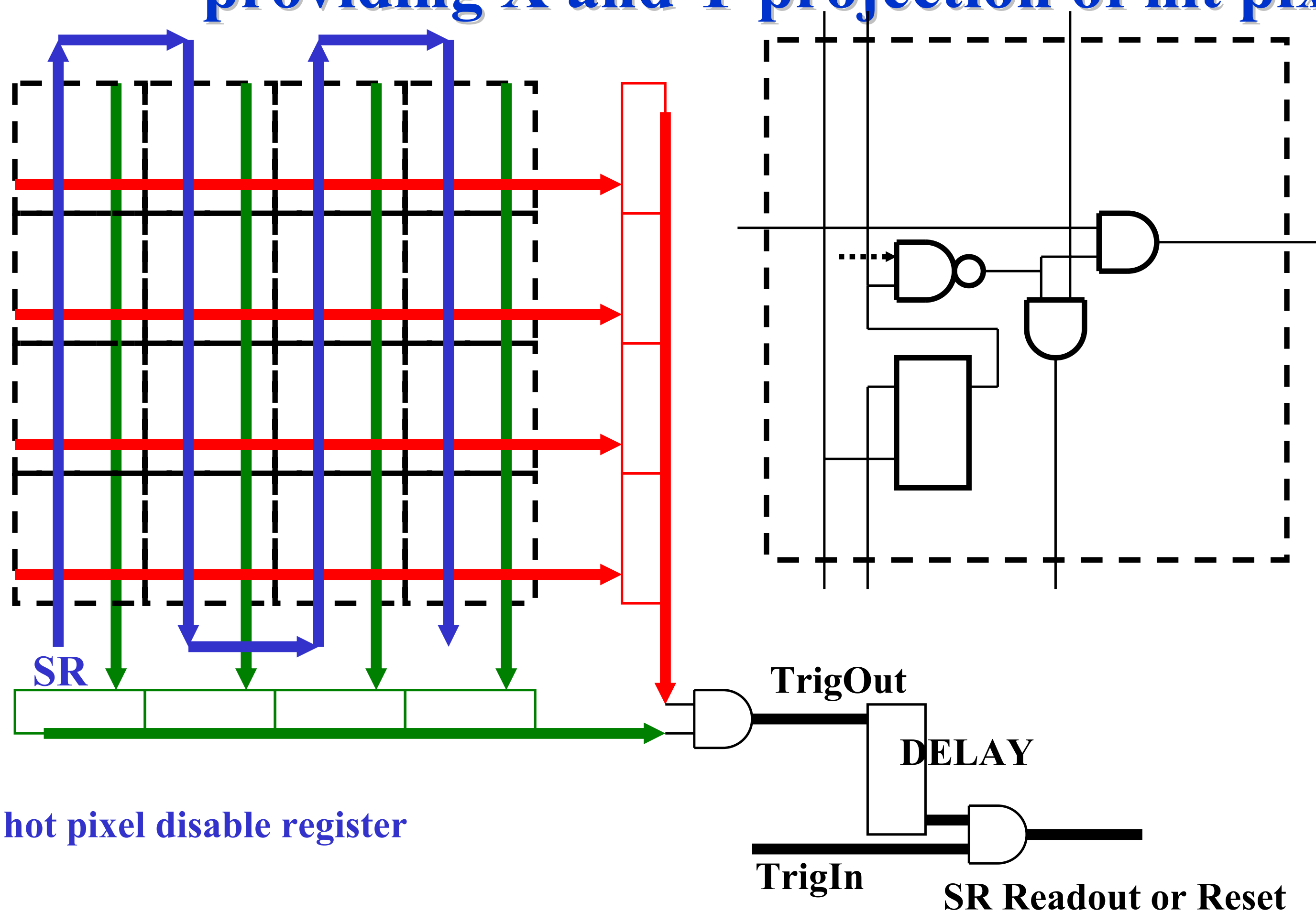
STriPSeT: Data driven (self-triggering), sparsified binary readout providing X and Y projection of hit pixels pattern



SR: hot pixel disable register

Main features:

250x250 pixel array, 20 µm pitch → 5x5 mm² area

readout clock : 160 MHz

2 output lines ≡ Array readout time: ~2µs

Programmable Active Area (through pixel disable SR)

Readout compatible with existing digital DAQ developed at IPHC.
Possible application: general purpose fast beam telescope → extension/improvement of EUDET

Wojciech.Dulinski@ires.in2p3.fr

Our first experience with 3D Integration shows that the road is long and rugged…

- end 2008: Tezzaron/Chartered kit installed, with April 2009 as a goal for submission
- several iteration of DRC rules, "final" submission in June 2009
- data handling errors within 3DIC and at the interface 3DIC/Tezzaron, Tezzaron/Chartered
- mask set accepted for processing ~April 2010
- first two iteration of processing ended with TSV problems, the third one started in July
- still hope to get prototypes in autumn 2010, but already anticipate serious problems with the second 3DIC submission (change of processing fab?)

However there are also some signs of positive evolution: 3D MPW submissions soon available through CMP/MOSIS…

Wojciech.Dulinski@ires.in2p3.fr

Proposal for the next Chartered/Tezzaron submission (AIDA?)

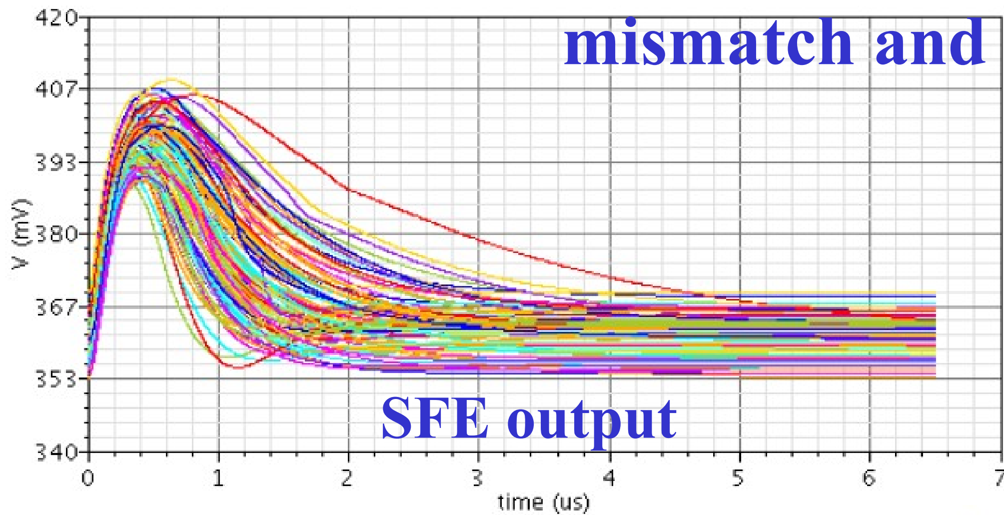
Larger area (~1 cm^2), being extension of the present StripSet . Such device may find immediately practical applications (fast and high precision beam telescope for example) and we may expect more collaborators and more financial resources for this.

Proposed device will be based on StripSet architecture (diode + SF on the first tier, optimized SFE on the second tier and simple (but fast and data driven) digital readout on the third one.

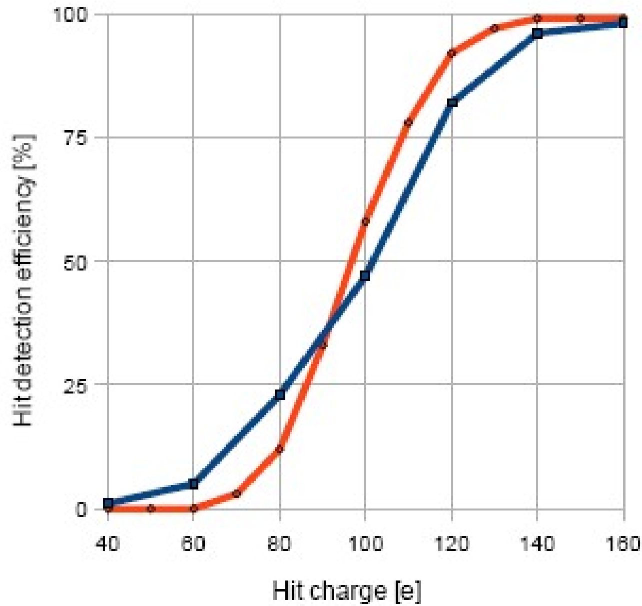
Possible (and proposed) extensions: Time-Over-Threshold ADCs at the end of lines and columns (to improve both spatial and time resolution and to allow for low-resolution spectroscopy) and possibility of bonding of other (instead of XFAB CMOS) sensors: silicon, diamond or others. Important point is that today we know much more about requirements and rules of ZyCube and Ziptronix, and these requirements will be better respected (not really the case of the first submission, submitted in a hurry more than a year ago).

Wojciech.Dulinski@ires.in2p3.fr

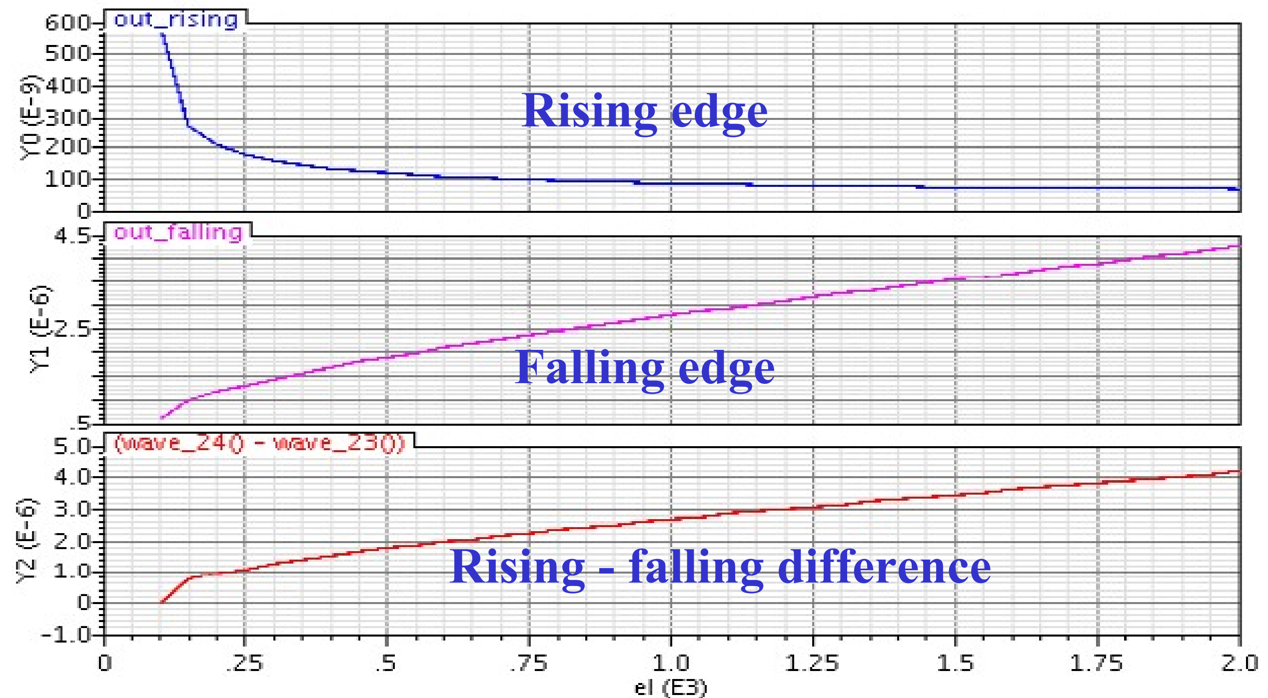
On-going work on SFE optimization: MC simulation results (device mismatch and noise contribution)



SFE output



Discri transfer: old vs. new



Discri out vs. input charge

Wojciech.Dulinski@ires.in2p3.fr

Conclusions

- 3D integration of heterogeneous CMOS wafers is very attractive and straightforward approach in order to improve performance of monolithic sensors. It provides tremendous increase of flexibility of readout schemes with an optimal choice of functions for each layer
- 3D integration is efficient approach in order to reduce power consumption, which is essential in case of thin detectors
- The main goal of proposed exercise is to explore and test all the most promising industrial technologies under (rather fast) development
- First results expected still in 2010: reception and tests of Chartered/Tezzaron chips submitted last year through 3DIC Consortium
- Submission (November) of optimized SFE (2D MPW Chartered run)
- Early 2011: submission of XFAB-035 high resistivity epi sensors. Second Tezzaron/Chartered submission. Ziptronix (or ZyCube) bonding will follow…