CALICE DAQv2

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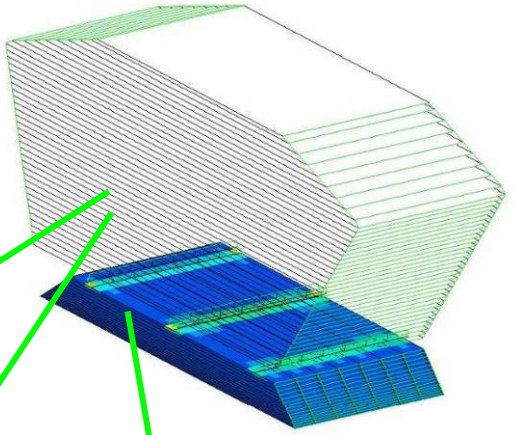
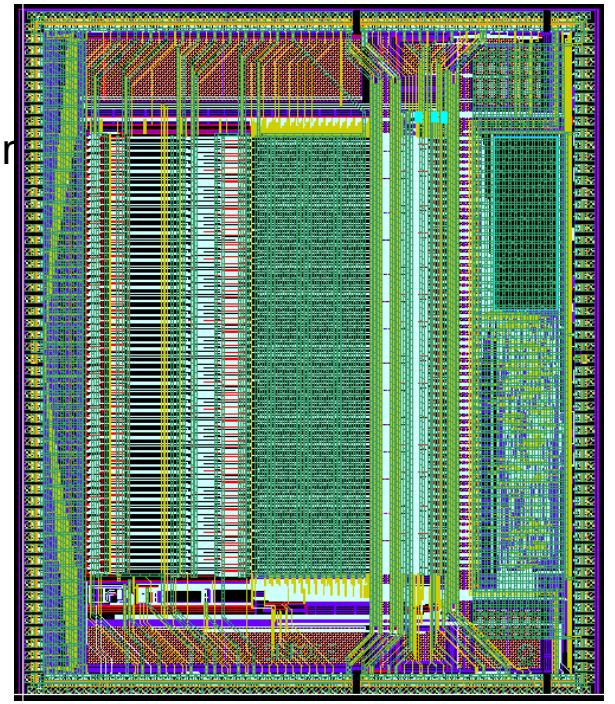
EUDET Annual meeting
DESY, 29/09/2010

Second generation ASICs

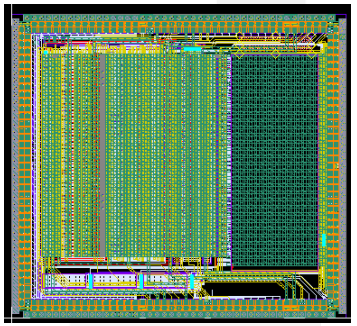
- Add auto-trigger, analog storage, digitization and token-ring readout !!!
- Include power pulsing : <1 % duty cycle
- Address integration issues asap
- Optimize commonalities within CALICE (readout, DAQ…)



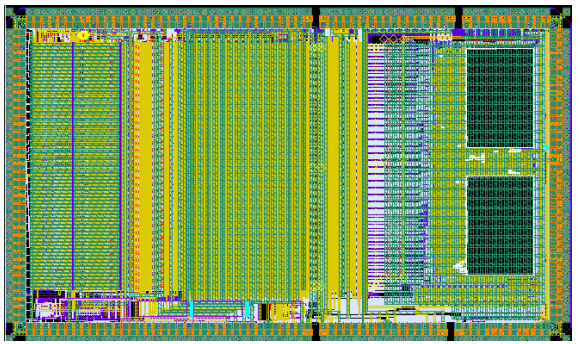
SKIROC2
ECAL Si
64 ch 70 mm



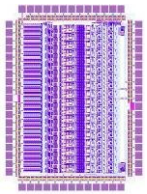
HARDROC2
SDHCAL RPC
64 ch 16 mm²



SPIROC2
AHCAL SiPM
36 ch 30 mm²

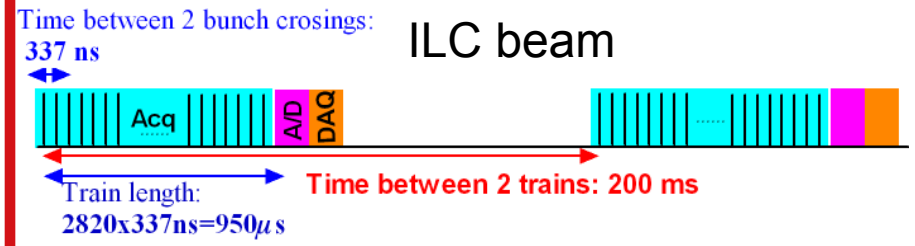


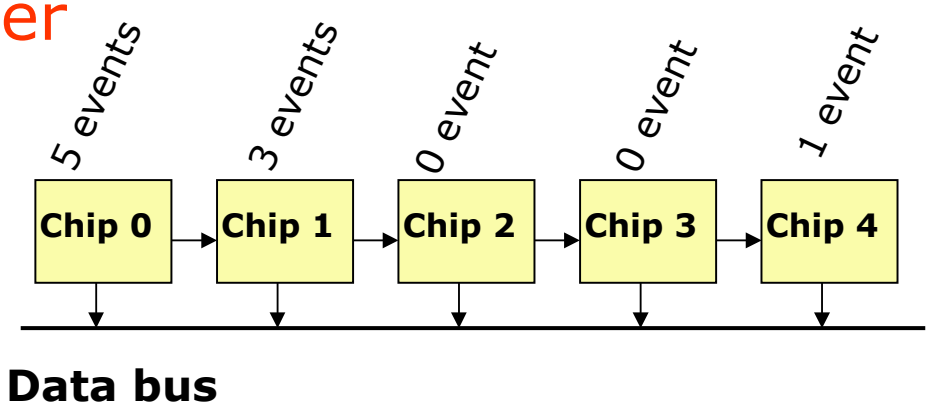
FLC_PHY3 (2003)

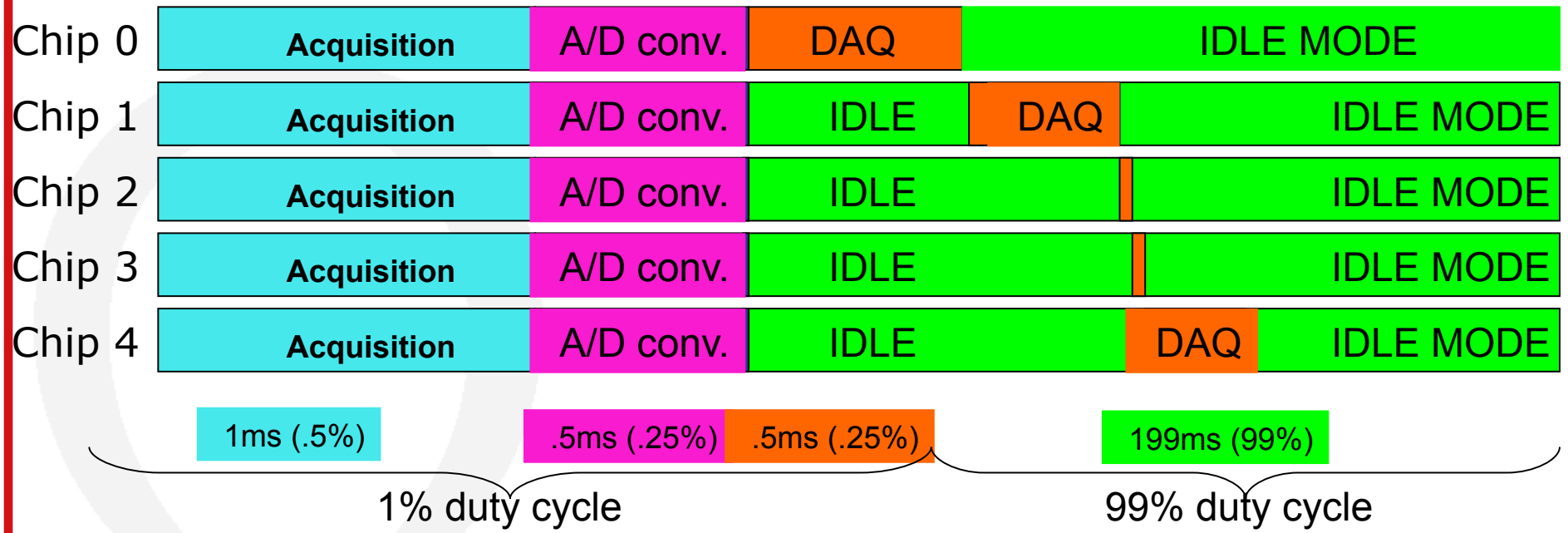


Read out: token ring

- Readout architecture common to all calorimeters
- Minimize data lines & power







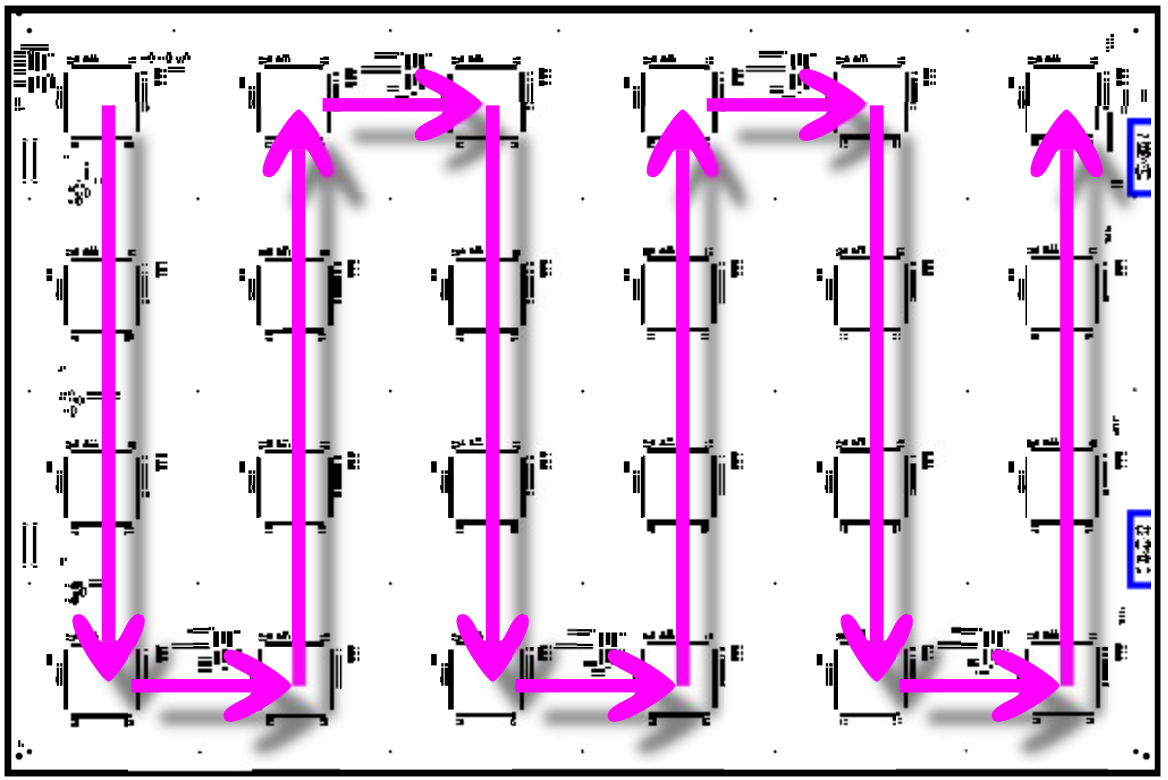
ECAL DAQ : data volume and rate

- Raw Data volume
  - 2 bytes Energy data/Channel, 20 Million channels
  - Raw data per bunch train ~ 20M × 5000 × 2 ~ 200GBytes ECAL
  - No way to digitize inside the ~ ms train
  - 10 kbytes/channel/train ~ 50 kbytes/ch/s
  - Physics data rate : 90 Mbytes/train = ~20 bytes/ch/s

- Zero suppression mandatory
  - 10^3 rate reduction -> drastic for power dissipation
  - Digitize only signals over 1/2MIP with noise < MIP/10
  - Allow storage in front-end ASIC

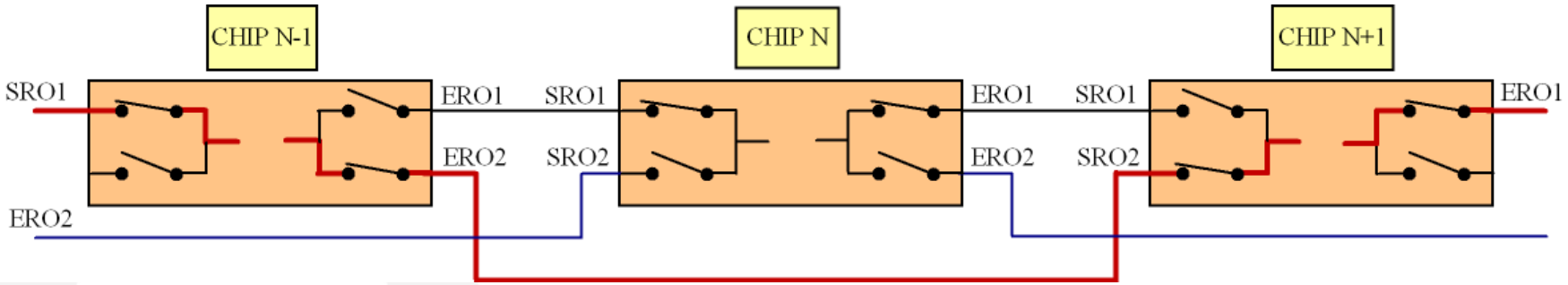
The ASU board: clock lines

- Clocks : 2 lines, drive every other chip, terminated at the end,
- 100 ohm resistance in series inside the chip
- Clock switched off inside the chip when not used



Readout protocol : token ring

- Bypass one dead chip : 2 inputs seleted by slow control

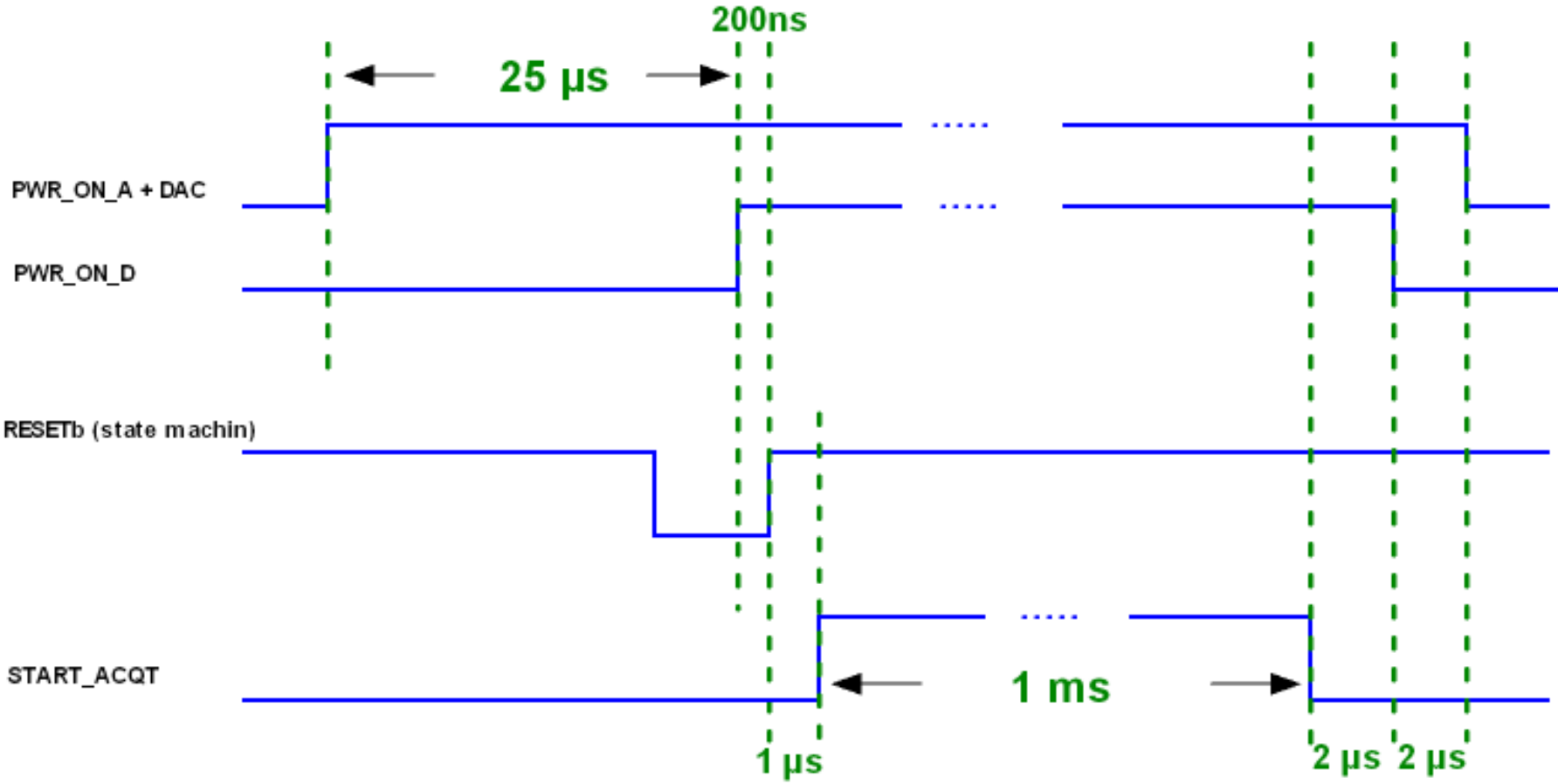


The ASU board: data lines

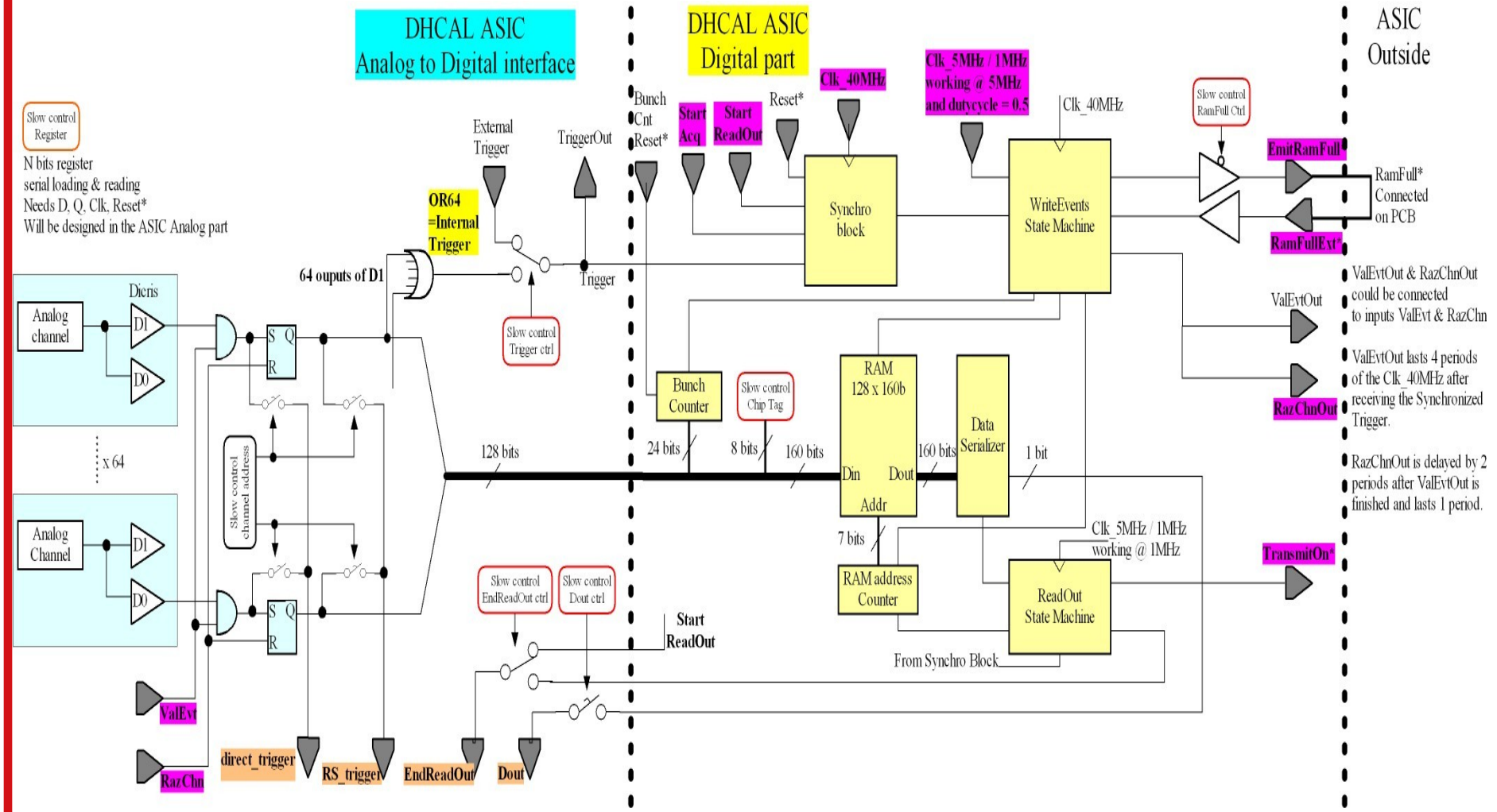
- Data : 4 lines : 2, doubled for redundancy
- Each chip has 2 data outputs that can be removed from each line by slow control

Power pulsing sequence

- 4 Power pulsing lines : analog, conversion, dac, digital
- Each chip can be forced on/off by slow control



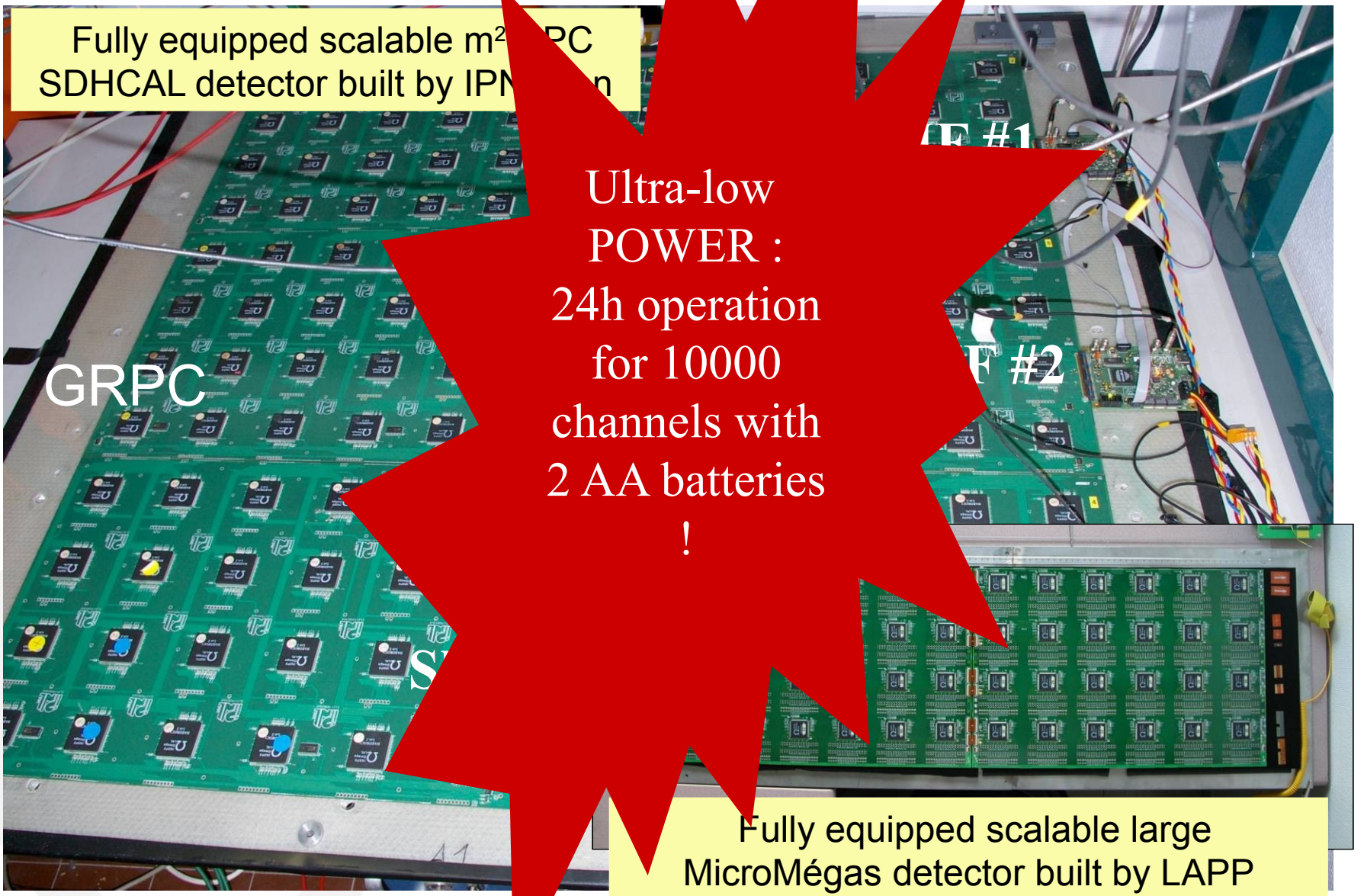
HARDROC1: digital part



Towards an ILC technological prototype

Omega

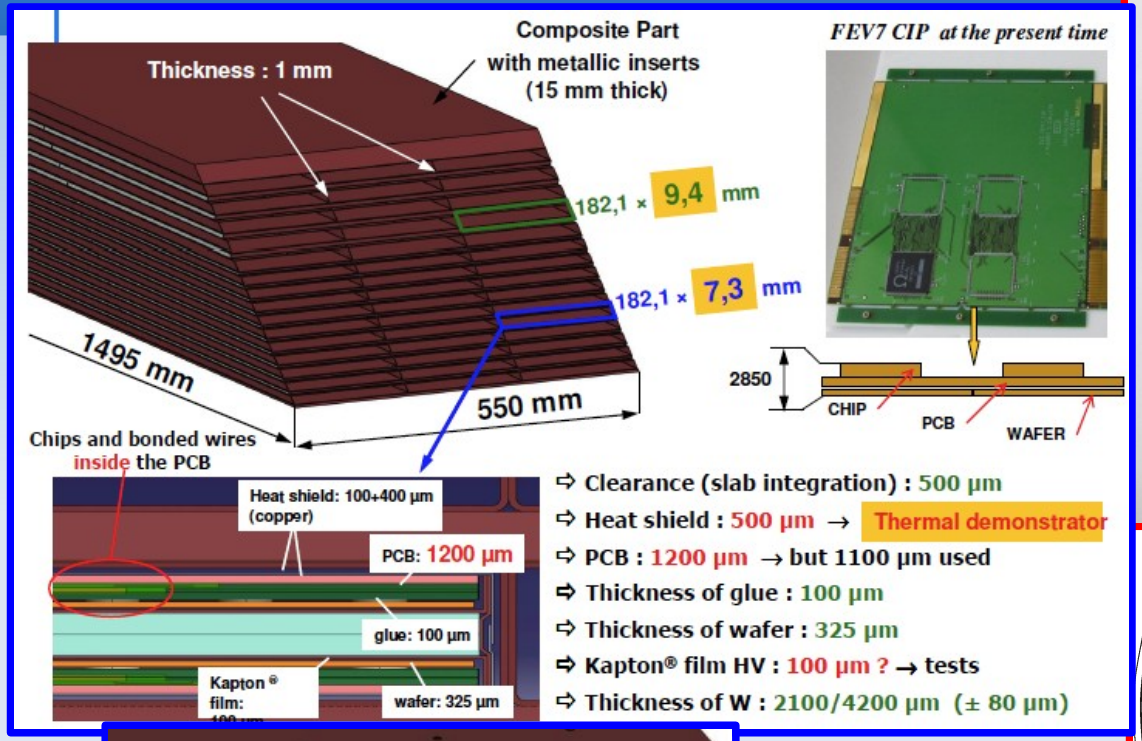
Fully equipped scalable m² RPC SDHCAL detector built by IPN

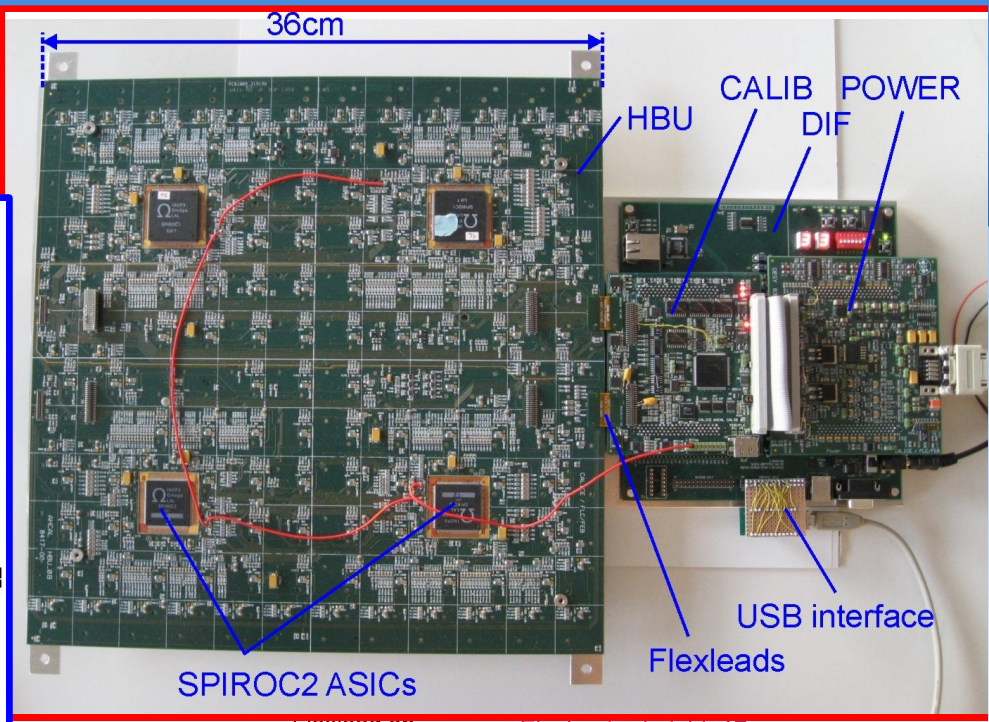


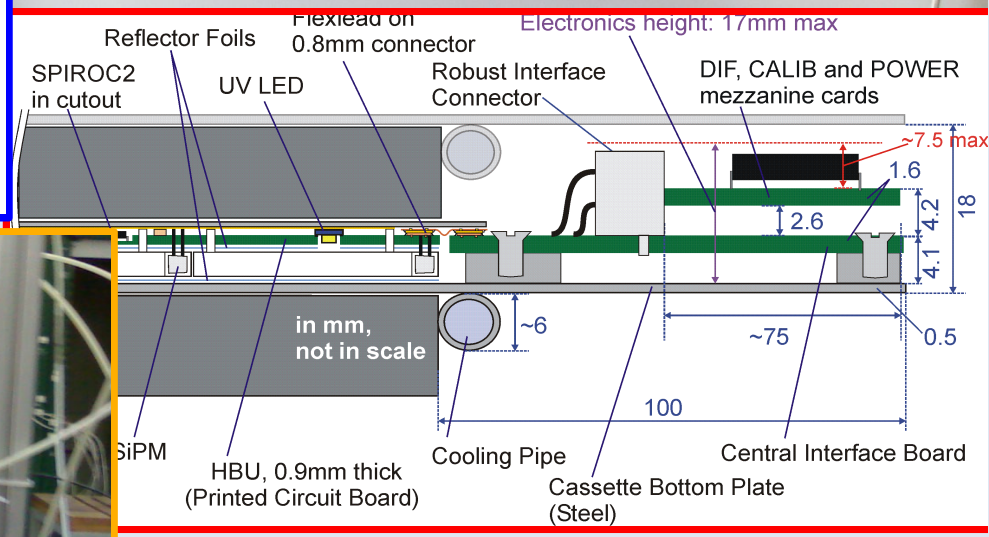
Ultra-low POWER : 24h operation for 10000 channels with 2 AA batteries !

Fully equipped scalable large MicroMégas detector built by LAPP Annecy

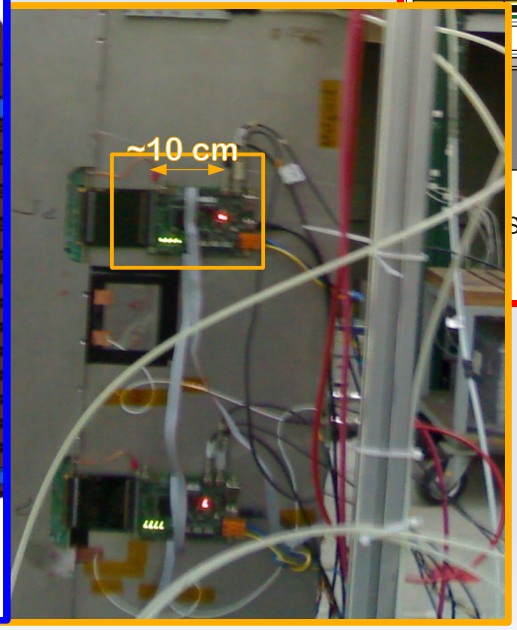
Detector interfaces







ECAL

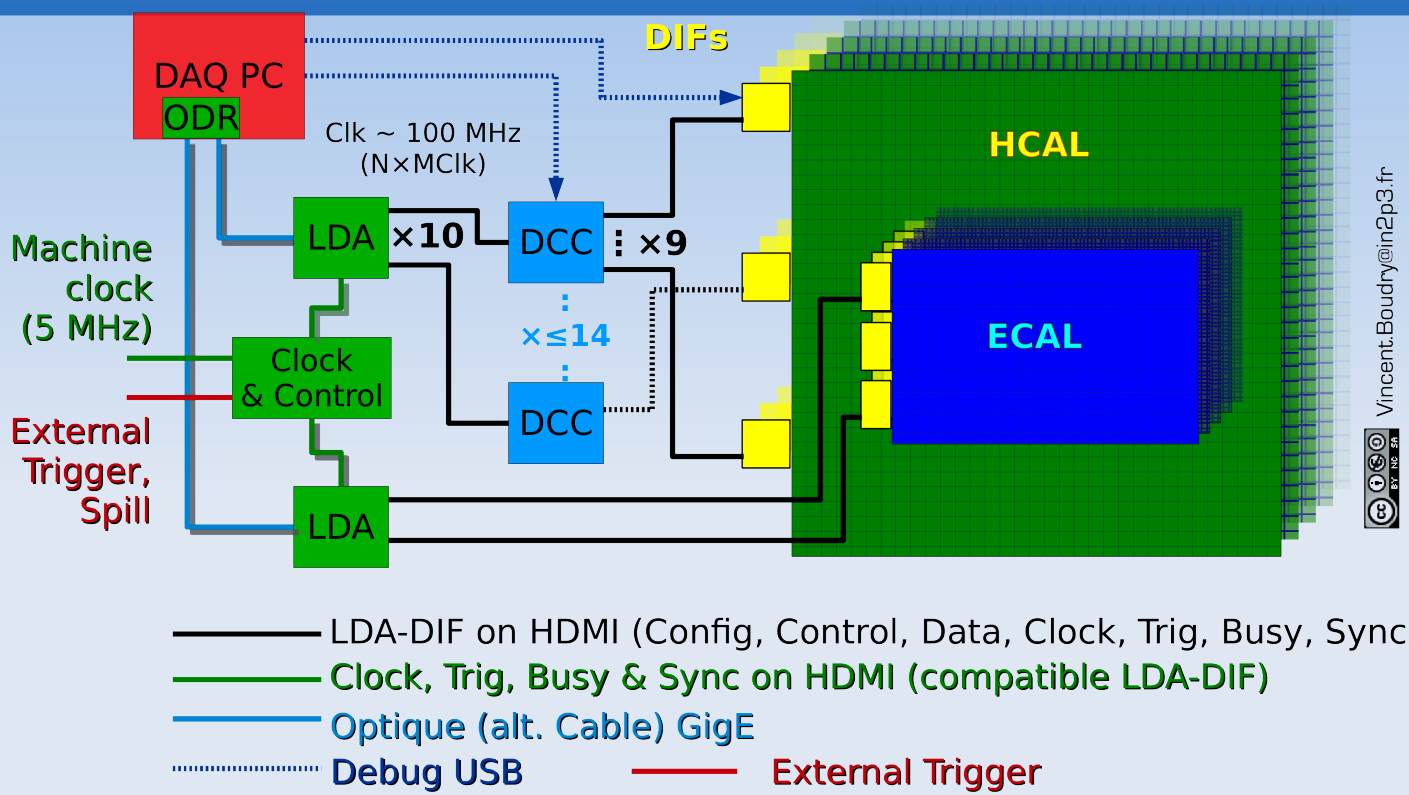


AHCAL

SDHCAL

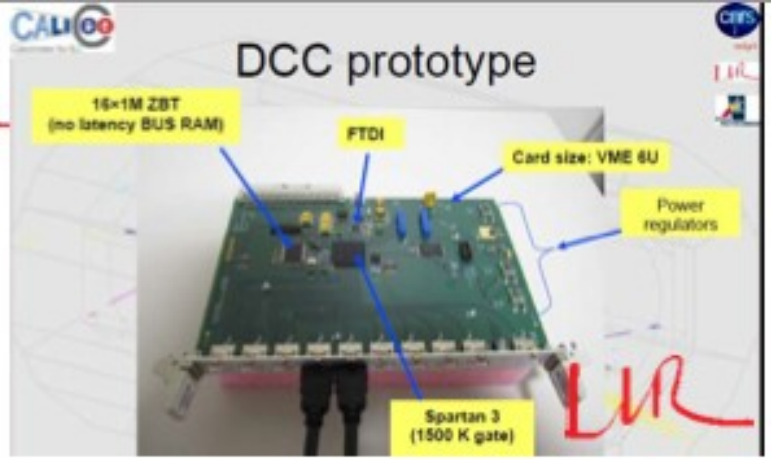
CALICE DAQ2 scheme

Big effort for CALICE!!
~15 individuals from:
- UK: CAM, MAN, UCL
- FR: LLR, LAPP, IPNL
- DE: DESY



Most of Code, Manual and HW description is available on CALICE twiki: https://twiki.cern.ch/twiki/bin/view/CALICE/CALICEDAQ

- Provide the digital readout of CALICE embedded front end
  - All calorimeter seen through 1 Detector InterFace board (DIF)
  - 1 (opt. 2) Concentrator cards level
  - 1 Clock and Control Card (CCC) for the fast signal distribution and collection
  - HDMI cables (aka 5 twisted shileded pairs) for physical transmission; add-hoc comm. Protocol
- 3 prototypes en route: SDHCAL (120 DIFs, 400.000 digital ch), ECAL (30 DIFs, 22.000 anal. ch), AHCAL (40 DIFs, 52.000 Anal. (En. & time) ch)



LDA

- The LDA (from Enterpoint) consists of :
  - Mulldonoch2 baseboard;
  - add-on HDMI board to connect to 10 DIFs;
  - an add-on ethernet board to connect to an ODR.
- Firmware development :
  - DIF <=> LDA link running;
  - new code soon to be posted to svn;
  - same format as ODR in svn repository.

DCC and LDA are essentially similar to an ethernet switch but using a low level protocol

They both fan-out/in fast isochronous signals on a dedicated path and commands on the 8b/10b serial link

LDA has a fast link : Gb ethernet to the upper level = ODR, and can connect to 10 DIFs or DCC with the 8b/10b serial link
DCC can connect to 1 LDA and 9 DIFs using the 8b/10b serial link, data from DIF are buffered and sent to the LDA

CCC

- Overall status unchanged for a while.
- Fans out clocks, fast commands and control signals.
- Fans in busy.
- Full complement of 10 boards with power supplies tested.
- One in LLR and one in LAPP.
- CCC link to LDA still needs to be done :
  - Board designed and firmware developed for testing;
  - Soon to produce enough boards for all LDAs.

ODR

- Receive data on 4x fibre (RX),
- Write to disk FAST (>150MB)
- Send data up fibre (TX)
- Controlled from Linux driver
- DOOCs Interface

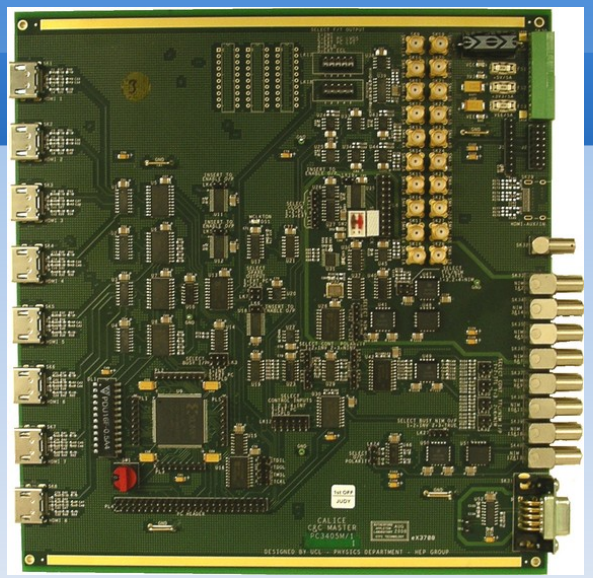
Documentation / repository

- All components *should* have extensive documentation on twiki : it is being updated and as components are basically done, can soon be finalised.
- Twiki main :

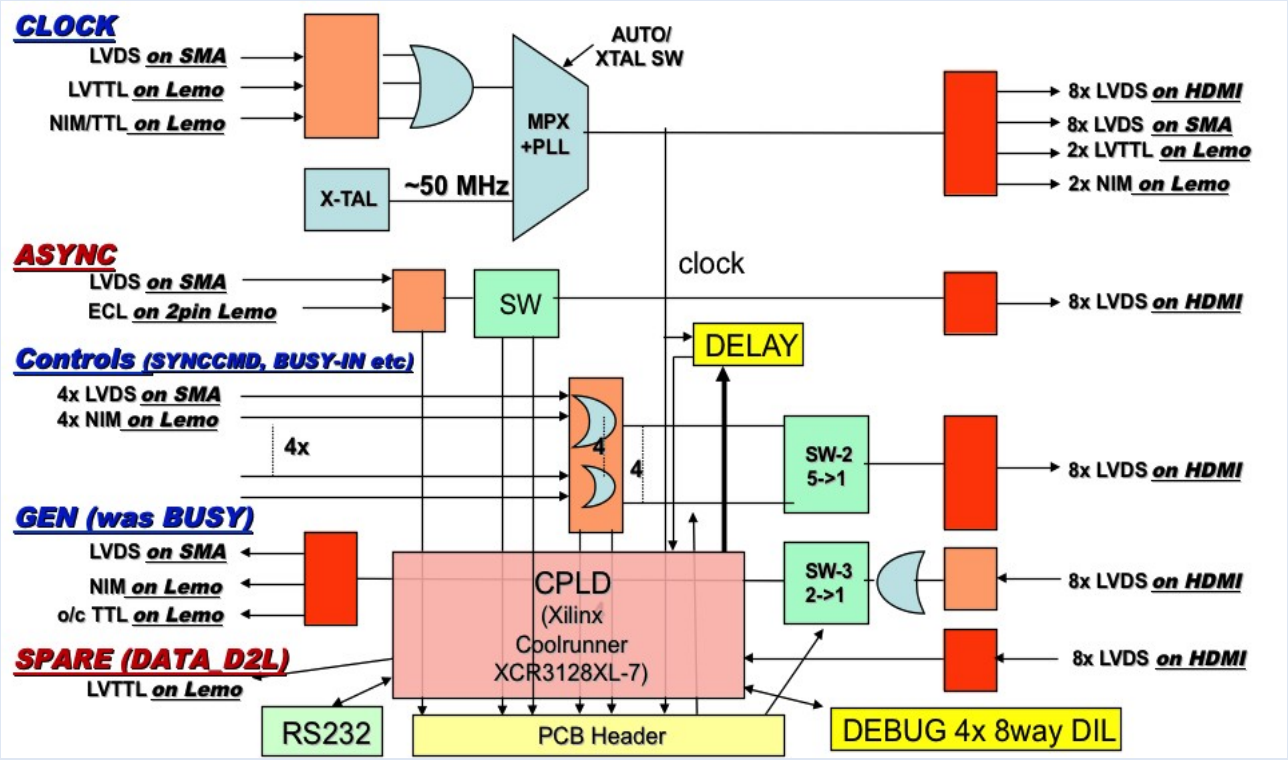
  https://twiki.cern.ch/twiki/bin/view/CALICE/CALICEDAQ
- Also list of hardware availability /status started.

  https://twiki.cern.ch/twiki/bin/view/CALICE/HardwareList

Clock and Control Card



- Developped in UCL (M. Warren, M. Postranecky)
- Distributes on 8 channels (HDMI, SMAs, NIM, …) via dedicated circuiterie
  - Int | ext clock
  - Fast Signal (Trigger | Sync)
- Sums-up BUSY
- Performs Trigger logics
  - CPLD
- Was used as DIF-Master (dev^{t} of LAPP)
  - Aka also sending hard-coded commands to DIF directly



Beam InterFace card

Basis:

- CALICE chips use auto-trigger
  - Readout can be triggered by single event using external trigger (e.g. beam hodoscope)

    → “Single event” mode

    History of Chip is usable (e.g. in case of selective ext. trigger)
  - Readout triggered by environmental internal or extern trigger
    - Chip full
    - ILC-like mode (end-of-spill)
- Require some device to radout the beam line parameters
  - Scintillators; Cherenkov PM (coding of CEDAR bits)
  - Time of event (⊃ rec for wire chambers)

Implementation

- 2 solutions
  - Add-hoc card for interfaces with a CALICE ROC (SPIROC ?) + 1 DIF
  - Small adaption (buffers) card on a DIF + “simulation” of a digital ROC in the FPGA
- Both offer full compatibility with CALICE DIF ofr the DAQv2.
- To be implemented for 2nd version of CALICE beam test
- One of the task of AIDA (WP8.6.2)

HW status

- 10 ECAL DIF ready and working; 10 in prod; mat for 40 in total (CAM)
- DHCAL DIF: 165/170 cards tested & ready (LAPP)
- AHCAL DIF: in design, prod in NIU → 4 unit
- CCC: 10 cards ready; 4 in use in 4 labs; 3 more shipped → LLR
- DCC: 3 prototypes ready; 2 cards being tested → 20 end of october
- LDA: 20 main board OK
  - 5 v1 + 15 v2 Ethernet mezzanine : ✔
  - 6 CCC mezzanine; clock OK — Busy & Trigger not yet tested (TBC)
  - 20 HDMI Mezzanine: faulty connectors on 8 → in repair
- ODR + PC
  - 8 ODR ready ; network card being used instead for debugging
  - 6 PC available: 1 in LLR ; 3 other ready; OS needs to be upgraded
- Future BIF: to be developped (part of AIDA)

~ No more basic problem with HW
Reliability of HDMI connectors mechanics ?

FW status

LDA+CCC comm

Reuse MUX from DCC

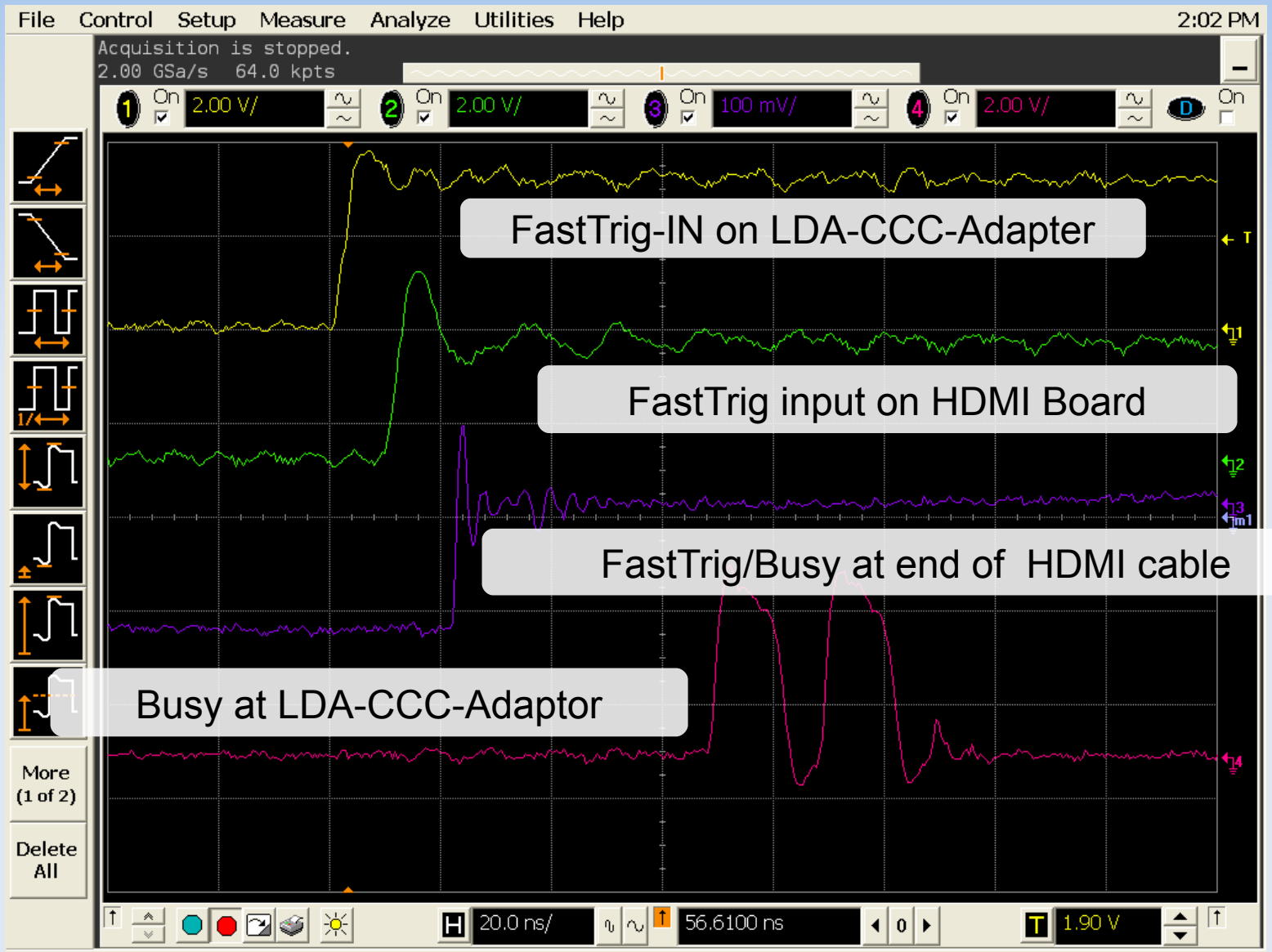
	LDA	DCC	DIF's
Ethernet	✔ at full speed		
CCC	Clk; Trig; Busy	Clk; Trig; Busy	Clk; Trig; Busy
Nlinks up	9/10 conn. no MUX	9	1
Fast Commands	✔	✔	✔
Block transfert	✔	✔	✔
Data[1)]	✔ (< 50 MHz)	✔ (< 50 MHz)	✔ (<50 MHz)
ROC			Structure ✔ Adapt SDHCAL USB Code on going...

- FW have been advancing rather fast during the last 3 months

Generic code for all DIFs

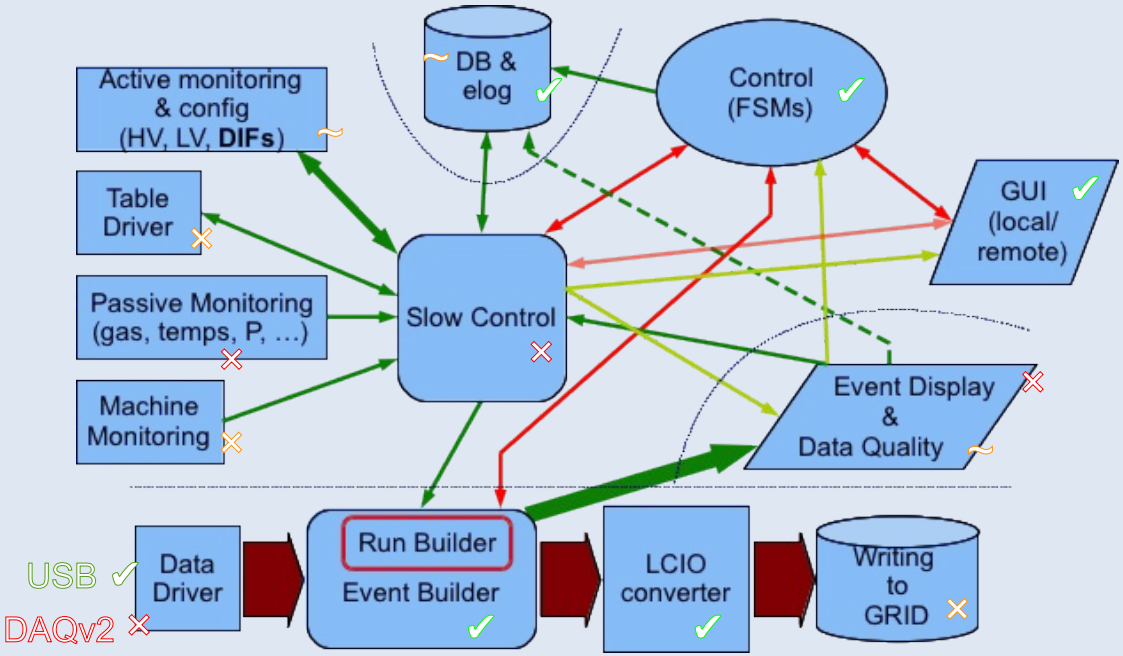
Many progresses recently
End of October for first full minimal usable chain ?

CCC←→LDA Fast signals tests (from 29/09/2010 15:45!)



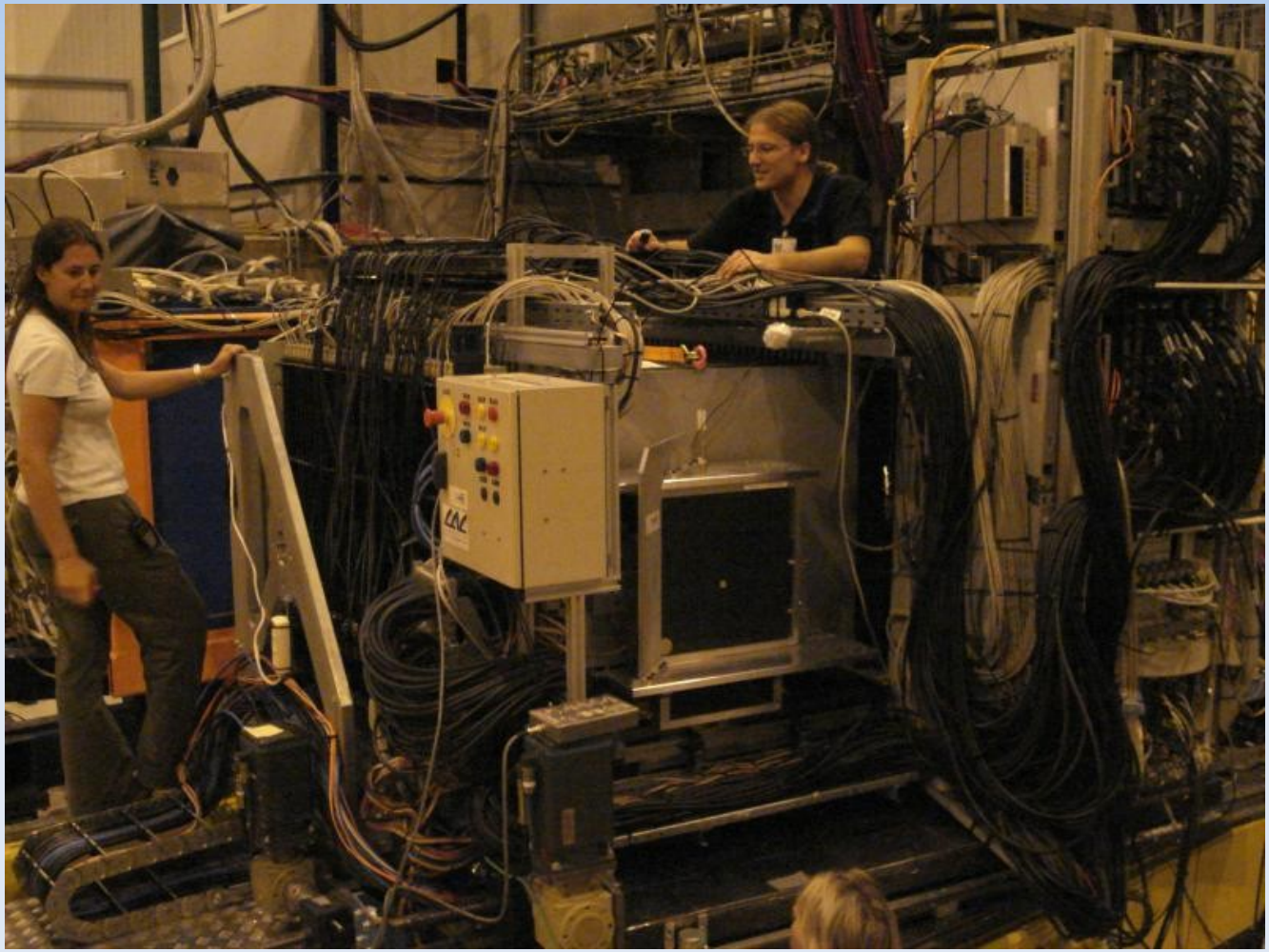
SW status

- Many progress
  - XDAQ (L. Mirabito, Ch. Combaret) “critical part“ complete:
    - Writing of LCIO data in RAW format
    - versatile online analysis framework (root histos)
  - DAQ2 interface ←→ XDAQ being worked on (D. Decotigny, G. Vouters)
- Missing utilities
  - Semi-automatic noisy channels spotting & correcting (moniting) ←←←
  - Clean Slow control
  - interface to CondDB;
  - event display (most probly DRUID)
  - interface to the GRID
  - interface to the machine
- Analysis environment (IPNL)
  - rec. data format in LCIO



Installation

- mechanics
  - mod. VME crate for
    - DCC
    - CCC
  - Special box for LDA
  - Support for cables
- Final set-up not yet known:
  - stand alone SDHCAL
  - stand alone ECAL
  - Stand alone AHCAL
  - Combined test
- → 5 m long HDMI cables
  - halogen free;



Conclusions

- Technological prototypes of CALICE are getting close (1st will be SDHCAL → Spring 2011)
  - 2nd version of ROC chips available
  - Being integrated in large prototypes → extensive TB in 2011
- All DAQ HW elements available
  - FW almost ready
  - Accomplishment of a long process
- SW: XDAQ surviced natural selection
- Combined (with other system) ≥ 2012
  - Prepare HW and SW beforehand
    - SW & HW ←→ TLU & EUDAQ first