JRA3 DAQ Task Status report

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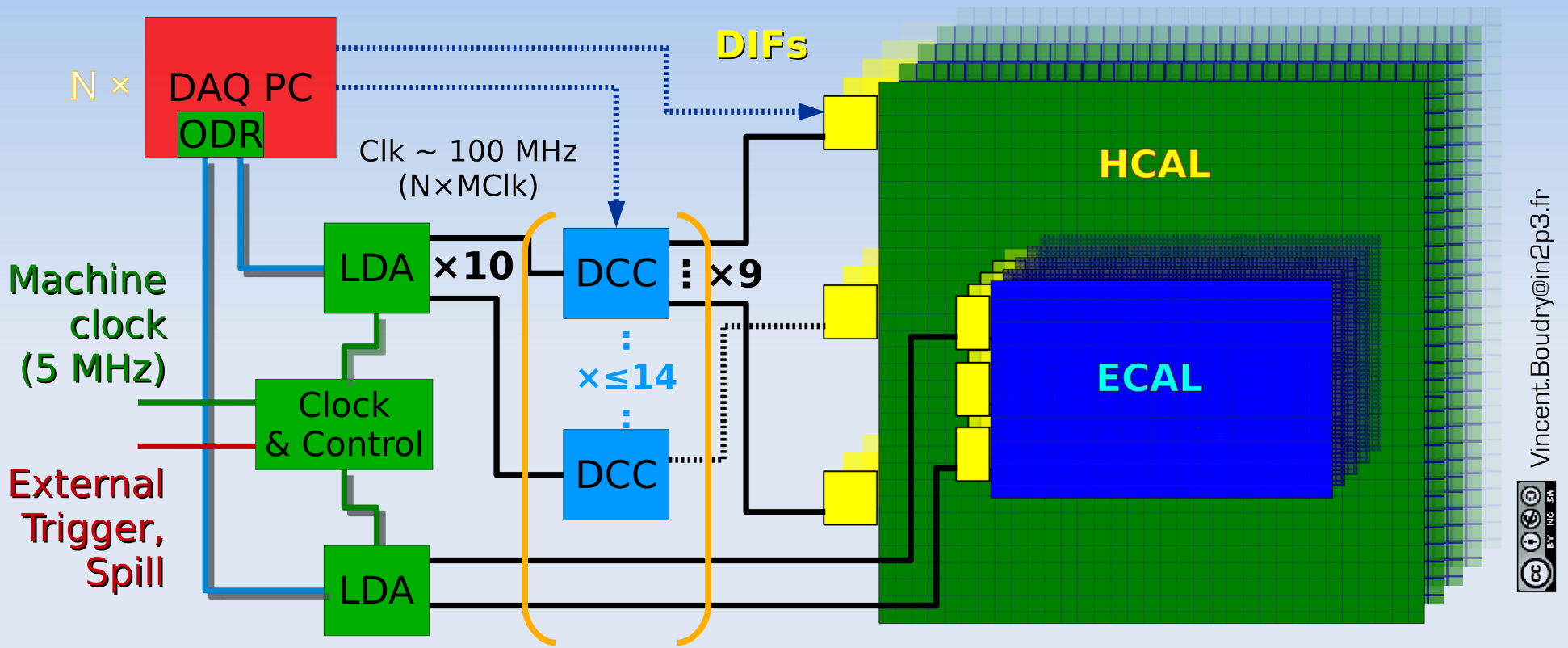
EUDET Final Annual meeting
DESY, 30/09/2010

DAQ Task goal

- "Generic" DAQ based AMAP on commercial boards
  - Extensible for Large Detectors
- Provide the **digital** readout of CALICE embedded front end (ROC* chips)
  - All calorimeters seen through standard Detector InterFace board (DIF)
    - Pass configuration; fast commands; clocks;
    - Receives Data; Busy
  - 1 (opt. 2) Concentrator cards level
  - 1 Clock and Control Card (CCC) for the fast signal distribution and collection
  - Advanced Off-detector receiver (FPGA based event builder)
  - All signals on 1 cables; add-hoc communication protocol
    - 8b/10b coding

- 3 CALICE prototypes en route:
  - SDHCAL : ~400.000 ch; digital → 2b/ch,
  - ECAL : ~22.000 ch; Energy,
  - AHCAL : ~52.000 ch: Energy & time

CALICE DAQ2 scheme



LDA-DIF on HDMI (Config, Control, Data, Clock, Trig, Busy, Sync)

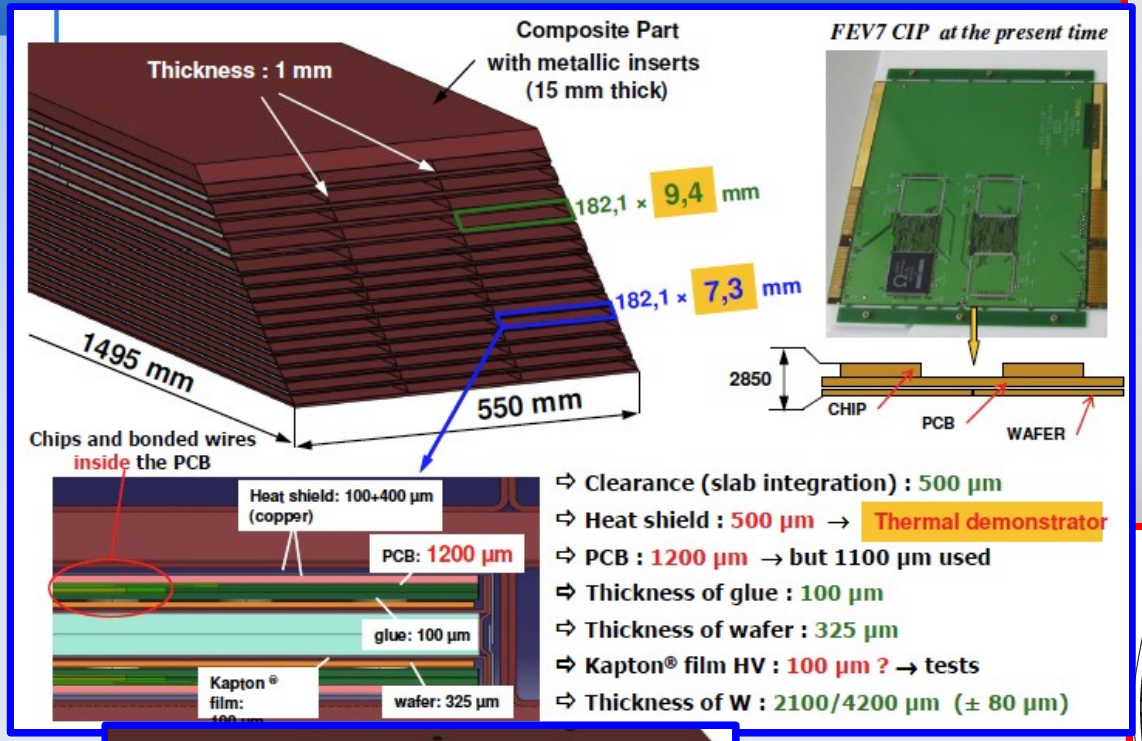
Clock, Trig, Busy & Sync on HDMI (compatible LDA-DIF)

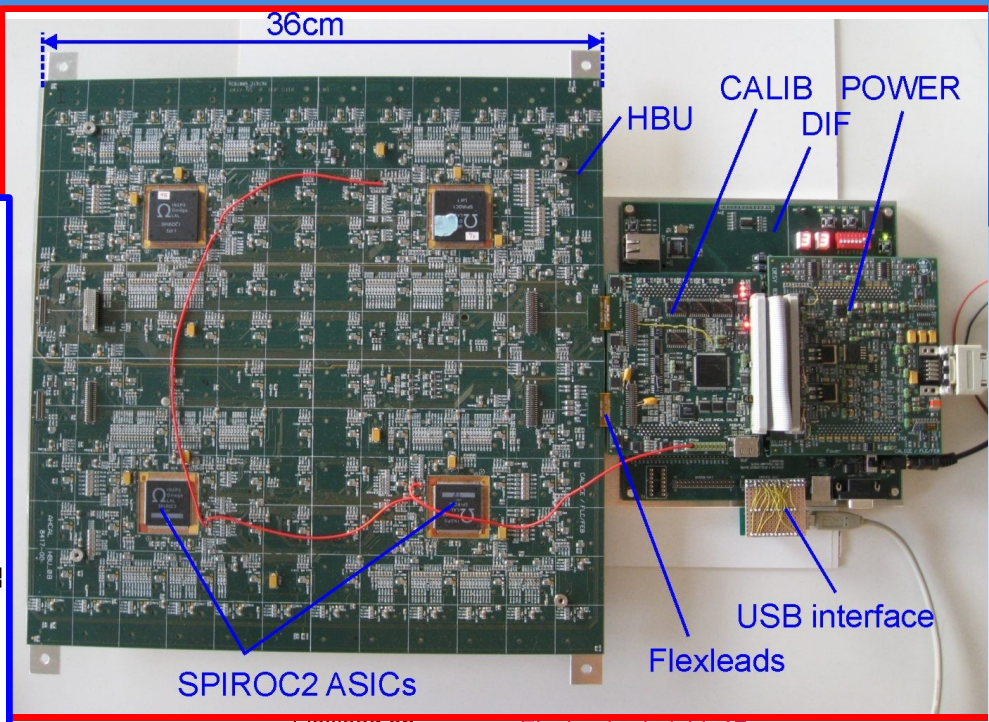
Optique (alt. Cable) GigE

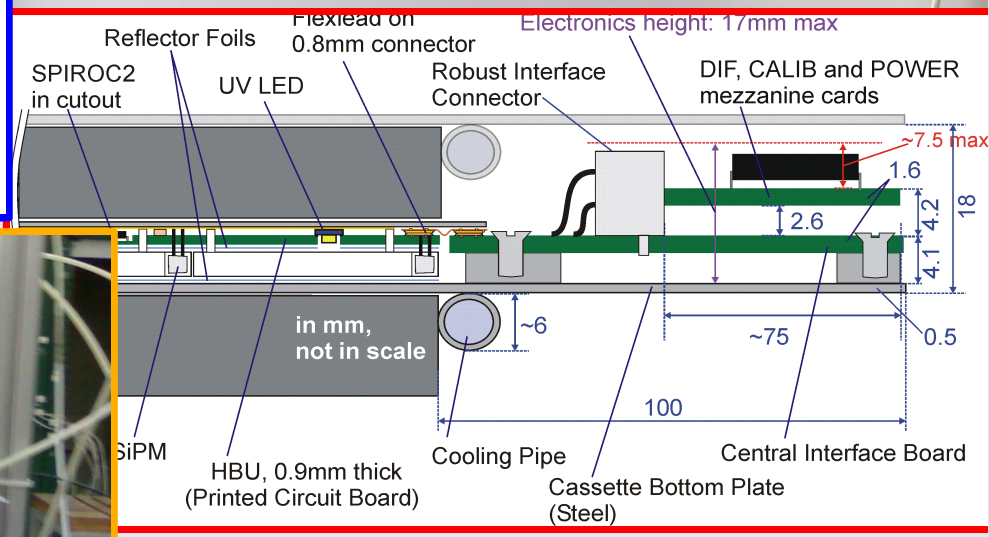
Debug USB

External Trigger

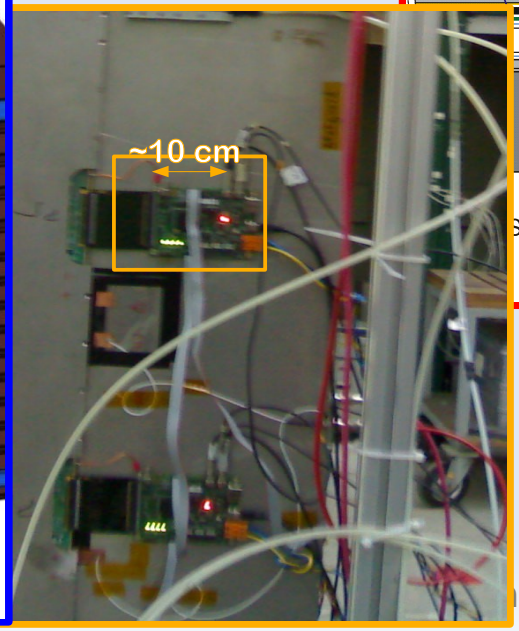
Detector interfaces







ECAL

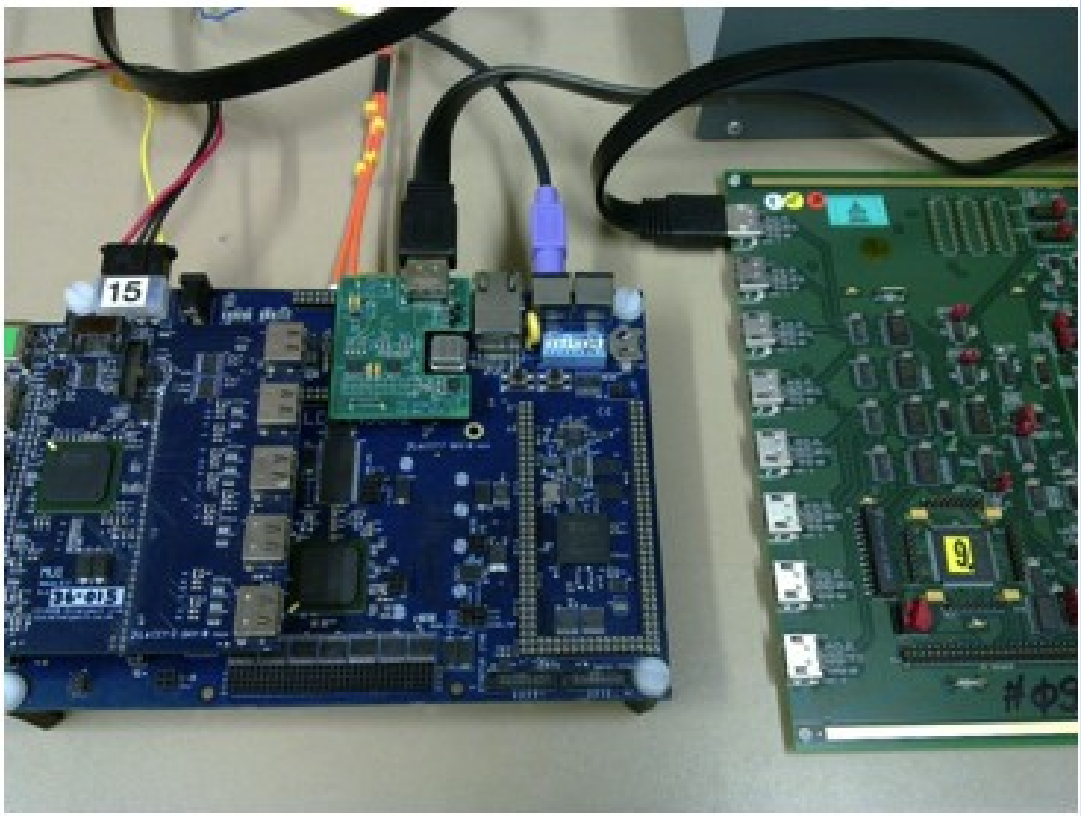


AHCAL

SDHCAL

CCC

- Overall status unchanged for a while
- Full complement of 10 boards with power supplies
- One in LLR and two in LAPP



Recent work :

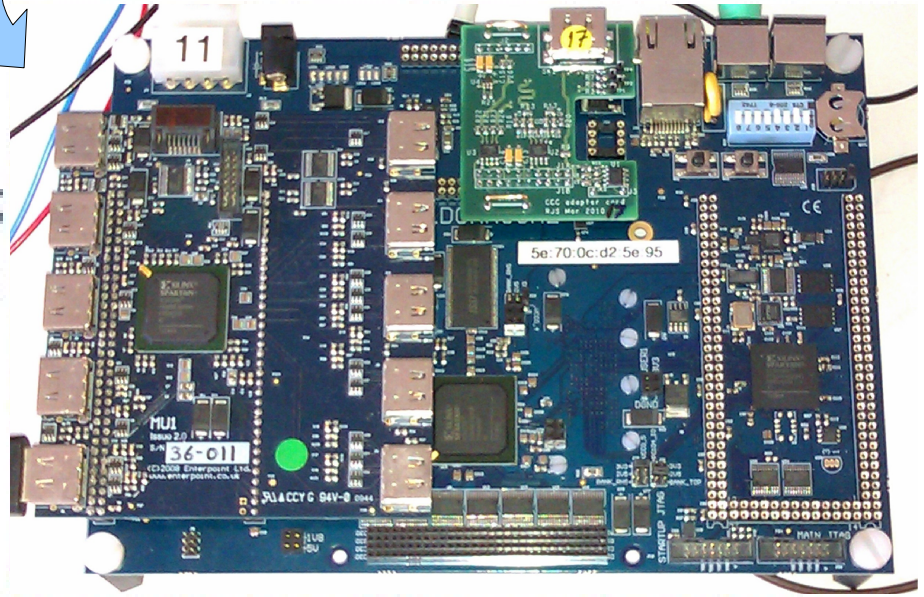
- CCC link to LDA has been done
- Board designed at UCL and built at Cambridge
- Produced 25 boards (one for each LDA), tested and ready for use (summer students)
- Capacitor changed on CCC; supplied with wrong value (summer students)

CCC + add-on in use (supplying a clock) in system tests

- Was used as DIF-Master (dev^{t} of LAPP) in beam test:
  - Sending hard-coded Fast Commands & signals to DIF directly
  - DIF readout done by USB

LDA

Requires add-hoc protection
(contrains, chocs, physicists)



- The LDA (from Enterpoint) consists of :
  - Mulldonoch2 baseboard;
  - add-on HDMI board to connect to 10 DIFs;
  - an add-on ethernet board to connect to an ODR;
  - a CCC add-on board.

- Hardware status—recall all three (Enterpoint) boards had problems and needed re-design :
  - another came along with the production run; some HDMI connectors broke or broke the cable. Care needed on (un-)plugging; ease is cable dependent;
  - SAMTEC admitted fault in their connectors; 8 boards with manufacturer for repair;
  - decided to get a few more spares ...
  - added termination resistors on all HDMI boards at UCL (improves signalling and reduces FPGA power)
  - all boards apart from those in repair at UCL

REM: ”Happy end” of a long saga

Beam InterFace card

Basis:

- CALICE chips use auto-trigger
  - Readout can be triggered by single event using external trigger (e.g. beam hodoscope)

    → “Single event” mode

    History of Chip is usable (e.g. in case of selective ext. trigger)
  - Readout triggered by environmental internal or extern trigger
    - Chip full
    - ILC-like mode (end-of-spill)
- Require some device to radout the beam line parameters
  - Scintillators; Cherenkov PM (coding of CEDAR bits)
  - Time of event (⊃ rec for wire chambers) within a 5 MHZ clock period

Implementation

- 2 solutions
  - Add-hoc card for interfaces with a CALICE ROC (SPIROC ?) + 1 DIF
  - Small adaption (buffers) card on a DIF + “simulation” of a digital ROC in the FPGA
    - Part of the coding can be “tricky”
- Both offer full compatibility with CALICE DIF for the DAQv2.
- To be implemented for 2nd version of CALICE beam test
- One of the task of AIDA (WP8.6.2)
  - For “standalone” CALICE tests
  - Functionnalities ⊃ in JRA1 TLU

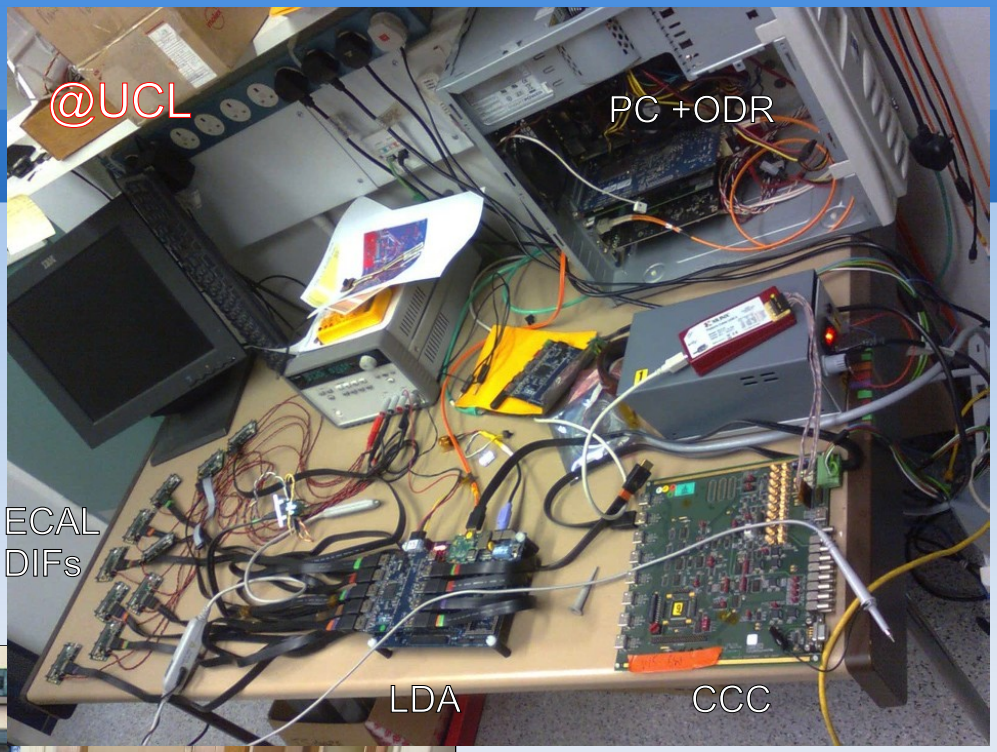
HW status

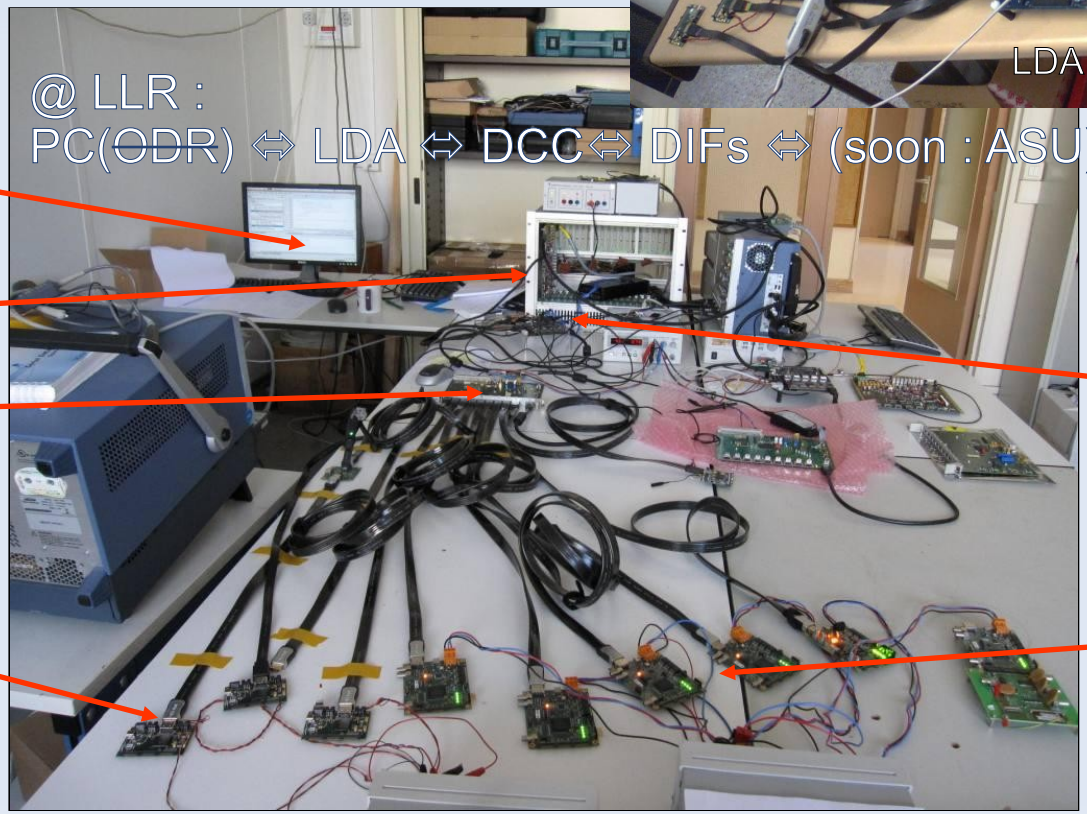
- **DIFs**
  - **ECAL** DIF ready and working; **22 ready; mat for 40** in total (CAM)
  - **DHCAL** DIF: **165**/170 cards tested & **ready** (LAPP)
  - **AHCAL** DIF: proto exist, **in design**, prod in NIU → 4 unit
- **CCC**: **10 cards ready**; 4 in use in 4 labs; 3 more shipped → LLR
- **DCC**: 3 prototypes ready; **2 prod cards being tested** (✔) → **20** end of october
- **LDA**: **25** main board scheduled (**½ done**; ½ to be done)
  - 5 v1 + 15 v2 Ethernet mezzanine : ✔
  - 6 CCC mezzanine ✔
  - 20 HDMI Mezzanine: faulty connectors on 8 → in repair
- ODR + PC
  - **8 ODR** ready ; network card being used instead (debugging, ease of use)
  - **6 PC available**: 1 in LLR ; 3 other ready; OS needs to be upgraded
- BIF: **none** (to be developped in AIDA)

~ No more basic problem with HW
Reliability of HDMI connectors mechanics ?

Integration tests

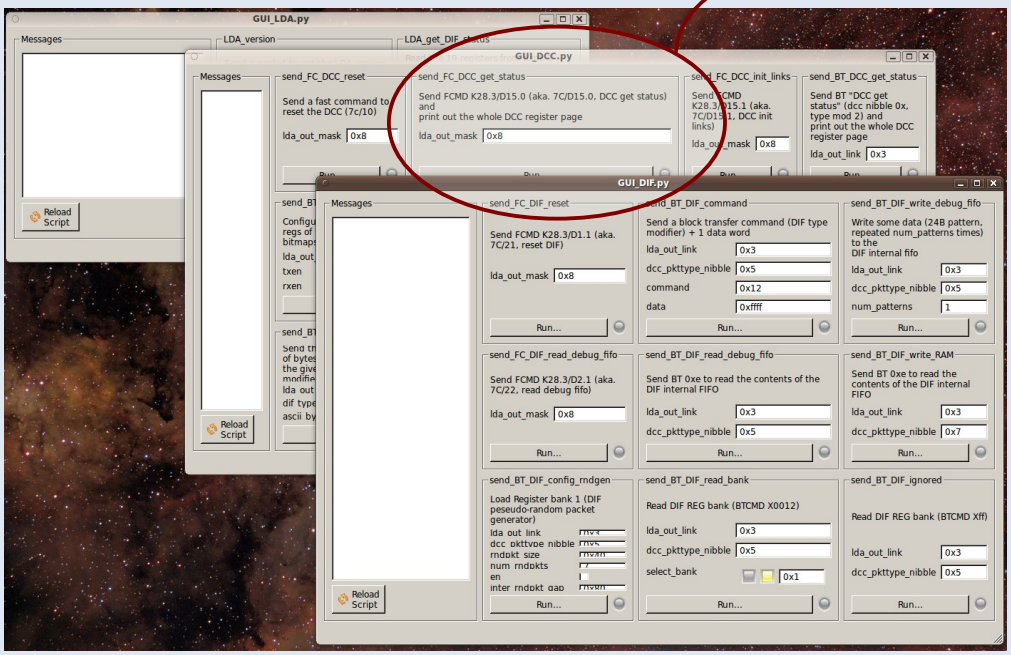
- Systems available @ UCL, LLR and now Cambridge
- Whole chain established :
  DAQ PC with ODR ⇔ LDA ⇔ DIF and CCC source
- Multiple (9, maybe 10) DIF ⇔ LDA links established
- FastTrig and Busy signals functional.





Python Test toolkit

- Interactive hardware test software (GUI)
  - Each HW test easily scriptable: simple user-friendly python API: each function defined ↔ 1 graphical pane with “Run” button
  - Intensively used by Franck/Remi
  - Available to anyone working with USB/RS/Ethernet devices
- C libraries implementing the complete **DIF Task force** protocole




```
File  Edit  Options  Buffers  Tools  Python  Help

def send_FC_DCC_get_status(INT0x_lda_out_mask = 0x8):
    """Send FCMD K28.3/D15.0 (aka. 7C/D15.0, DCC get status) and
    print out the whole DCC register page"""
    comma  = commons.encode_8b10b_kd(28, 3)
    data   = commons.encode_8b10b_kd(15, 0)
    ans    = LDA.do_lda_send_fastcmd(INT0x_lda_out_mask, comma, data)
    calicediag.GUI.set_statusbar_message("Get_Status FCMD sent")

    return _unpack_DCC_get_status_page(ans[16:]) is not False

--:---  DCC.py       47% (189,0)   SVN-1428  (Python)----------
calicediag.register_action(DCC.send_FC_DCC_reset)
calicediag.register_action(DCC.send_FC_DCC_get_status)
calicediag.register_action(DCC.send_FC_DCC_init_links)

calicediag.register_action(DCC.send_BT_DCC_get_status)
calicediag.register_action(DCC.send_BT_DCC_config_tx_rx)
calicediag.register_action(DCC.send_BT_DCC_start_RTT)
calicediag.register_action(DCC.send_BT_DCC_stop_RTT)
calicediag.register_action(DCC.send_BT_DCC_relock_DCM)
calicediag.register_action(DCC.send_BT_DCC_register_blob)

--:---  GUI_DCC.py    Bot (7,0)     SVN-1428  (Python)----------
```

https://svn.in2p3.fr/calice/online-sw/trunk/pyserdiag/

Reliability tests

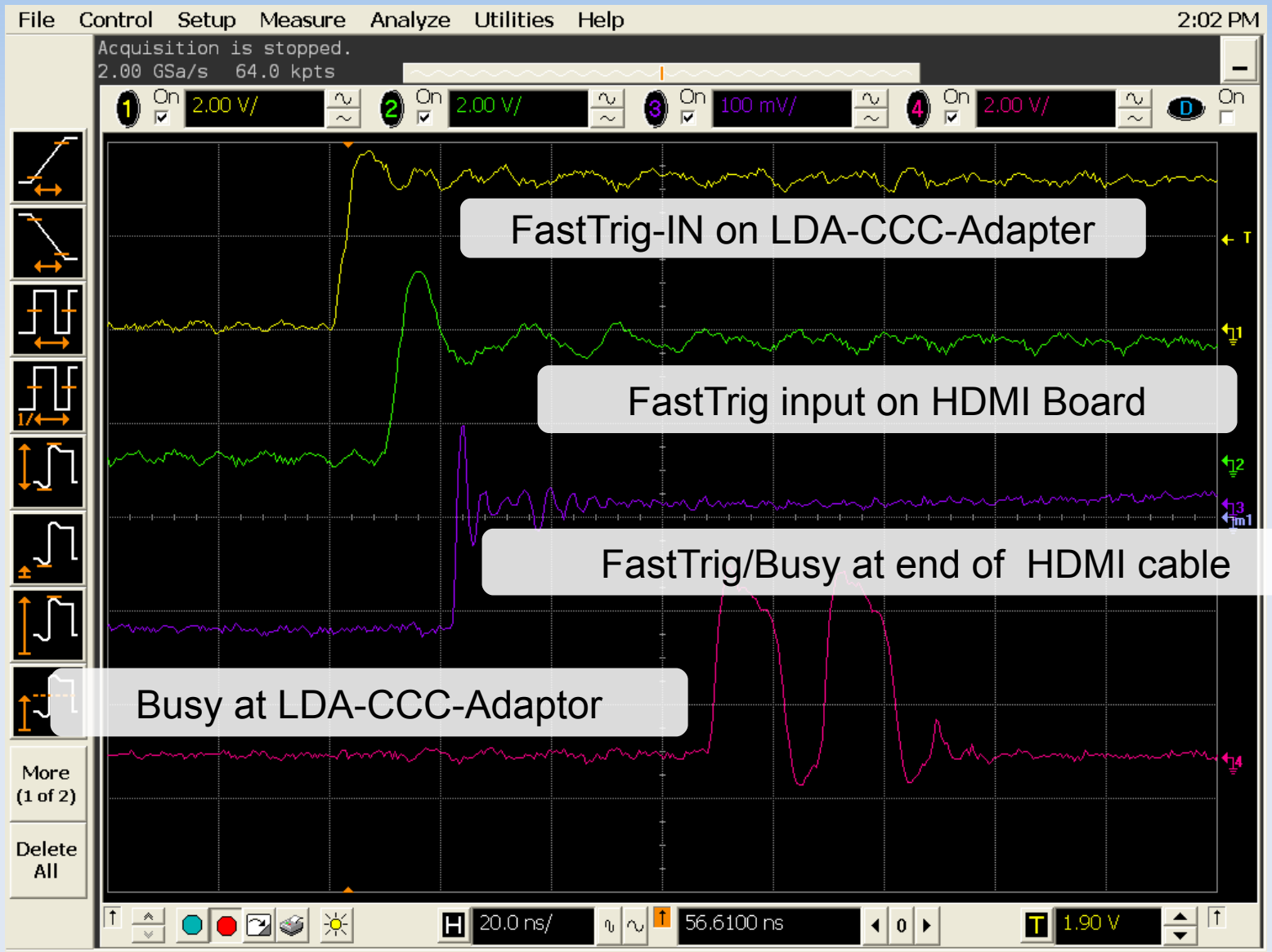
Stress tests using pseudo-random generator

- 9×DIF → 1×DCC → 1×LDA → PC
  - 4 DIFs generate pseudo random data
- Results
  - Direction DIF → LDA ✔
  - Maximum DCC → LDA link occupancy (40Mbps) ✔
  - Up to 5.6 TB transferred (2 weeks), no error

End-to-end test: FIFO write/read

- PC ↔ 1×LDA ↔ 1×DCC ↔ 1×DIF
  - Tests both fast-commands and block transfer “read” requests
- Results:
  - PC ↔ LDA Ethernet OK with built-in delais (1 ms)
    - fixed 2 wks ago for Block transfer (Config), still issues when interleaving Fast Commands
  - Still to be fixed Buffer overflow on non-connected links

CCC←→LDA Fast signals tests (from 29/09/2010 15:45!)



FW status

LDA+CCC comm

Much delay due to cut and leave from key Enginneer in 2009

Reuse MUX from DCC [?]

	LDA	DCC	DIF's
Ethernet	✔ at full speed		
CCC	Clk; Trig; Busy	Clk; Trig; Busy	Clk; Trig; Busy
Nlinks up	**9**/10 conn. no MUX	9	1
Fast Commands	✔	✔	✔
Block transfert	✔	✔	✔
Data[1)]	✔ (< 50 MHz)	✔ (< 50 MHz)	✔ (<50 MHz)
ROC			Structure ✔ Adapt SDHCAL USB Code on going...

- FW have been advancing rather fast during the last 3 months

Generic code for all DIFs

Many progresses recently
End of October for first full minimal usable chain ?

Performances

- Rather low demanding in term of bandwidth
  - SDHCAL : ~ 20MB/s in Spill
  - ECAL: ~100MB/s
  - AHCAL: ~ 300 MB/s
- Data limited by ASICs readout
- Some code (System C, by D. Decotigny) exists for simulation of full chain
- Many other studies...

DAQv2 data flux

N DIF/LDA	N DIF/DCC	LDA-DIF Dclk [MHz]	LDA-DIF FLUX [MB/s]	LDA Dclk [MHz]	LDA FLUX [MB/s]	ODR FLUX [MB/s]	Disk Flux [MB/s]
10	9	50	6.25	1000	125	1000	170

Detector	DHCAL	Evt Size	Mem Size	ASIC Dclk [MHz]	ASIC FLUX [MB/s]
		20 B	128	2.5	0.31

from LC-DET-2004-029

Mode	Calib/Noise Single	Calib/noise Burst	TB Single	TB Burst	Demo
N ASIC/DIF	48	48	4.8	4.8	4.8
σ (NASIC)	0	0	2.6	2.6	2.6
Touched DIF/pla	3	3	1	1	1
ASIC	20 B	2 560 B	20 B	2 560 B	2 560 B
R/O time 1	*64 µ s*	*8 192 µ s*	*64 µ s*	*8 192 µ s*	*8 192 µ s*
R/O time ALL	***3 072 µ s***	***393 216 µ s***	***307 µ s***	***39 322 µ s***	***39 322 µ s***
DIF	960 B	122 880 B	96 B	12 288 B	12 288 B
R/O time	*154 µ s*	*19 661 µ s*	*15 µ s*	*1 966 µ s*	*1 966 µ s*
LDA w/o DCC	9 600 B	1228 800 B	320 B	40 960 B	40 960 B
R/O time	*77 µ s*	*9,830 µ s*	*3 µ s*	*328 µ s*	*328 µ s*
DCC	8,640 B	1,105,920 B	288 B	36,864 B	36,864 B
R/O time	*1 382 µ s*	*176 947 µ s*	*46 µ s*	*5 898 µ s*	*5 898 µ s*
LDA w/ DCC	86,400 B	11,059,200 B	2,880 B	368,640 B	368,640 B
R/O time	*691 µ s*	*88 474 µ s*	*23 µ s*	*2 949 µ s*	*2 949 µ s*
ODR	172,800 B	22,118,400 B	5,760 B	737,280 B	737,280 B
1000MB/s	*173 µ s*	*22 118 µ s*	*6 µ s*	*737 µ s*	*737 µ s*
Disk	172,800 B	22,118,400 B	5,760 B	737,280 B	737,280 B
170MB/s	*1 016 µ s*	*130 108 µ s*	*34 µ s*	*4 337 µ s*	*4 337 µ s*
Max R/O time	***3 072 µ s***	***393 216 µ s***	***307 µ s***	***39 322 µ s***	***39 322 µ s***
Min Freq	0.33 kHz	0.00 kHz	3.26 kHz	0.03 kHz	0.03 kHz
Min. evts Freq		0.33 kHz		3.26 kHz	3.26 kHz

19MB/s

Occupancy for 100 GeV π in TB evts	
Mean	4.8
sigma	2.6
+3σ /√MemSize	5.49

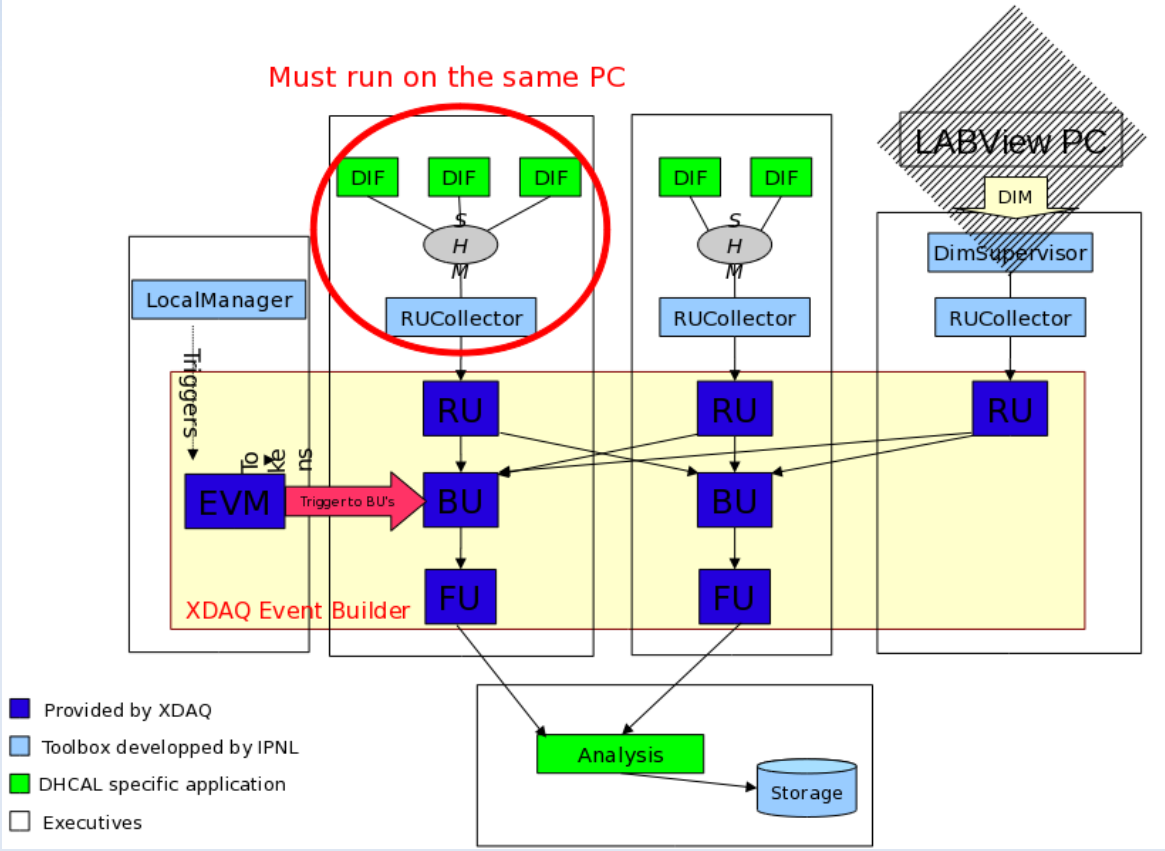
Parameters codes
Hardware (~fixed)
DAQ (achievable)
Physics (occupancies)

Software: XDAQ framework

- dev[ts] started @IPNL for electronics test using XDAQ in 2008
  - Ch. Combaret
  - Gained (a lot of) impulsion with involvment of L. Mirabito (resp. of DAQ SW for CMS tracker)
- Ran for ≥ 1 year in TB, Cosmics & Electronics test
  - USB readout
  - Interface to old LabView program
- Recent development
  - Writing of LCIO data in RAW format
  - versatile online analysis framework (root histos)

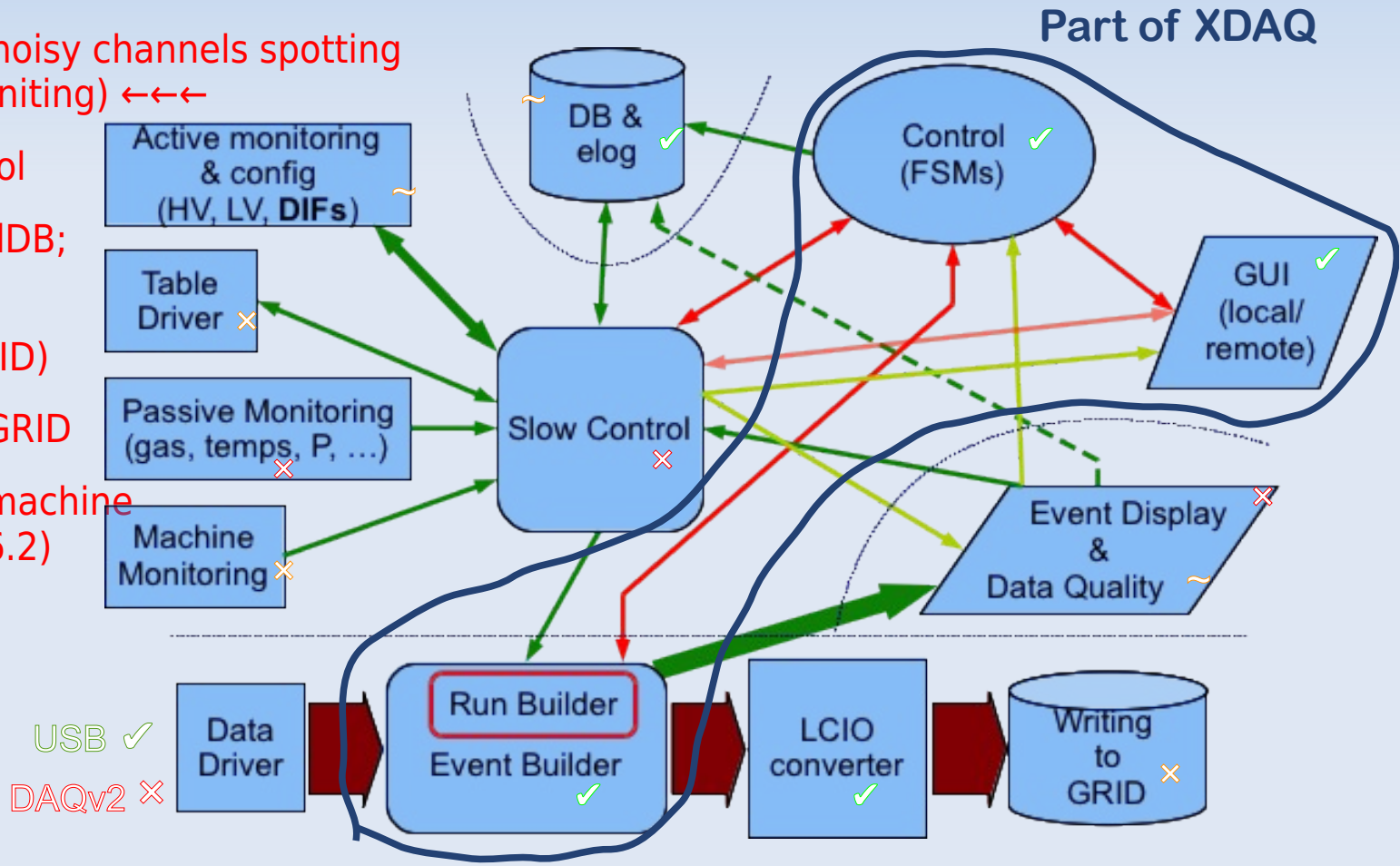
    → Marlin Based

- XDAQ vs DOOCS vs TANGO vs ...
  - Some developpements done in DOOCS
    - lacks of manpower & expertise
    - "killed" in the transition region



SW status

- Missing critical elements
  - Configuration DB (being worked on)
  - DAQ2 interface ←→ XDAQ being worked on
- Missing utilities
  - Semi-automatic noisy channels spotting & correcting (moniting) ←←←
  - Clean Slow control
  - interface to CondDB;
  - event display (most prob^{ly} DRUID)
  - interface to the GRID
  - interface to the machine (⊃ in AIDA WP8.6.2)



Documentation

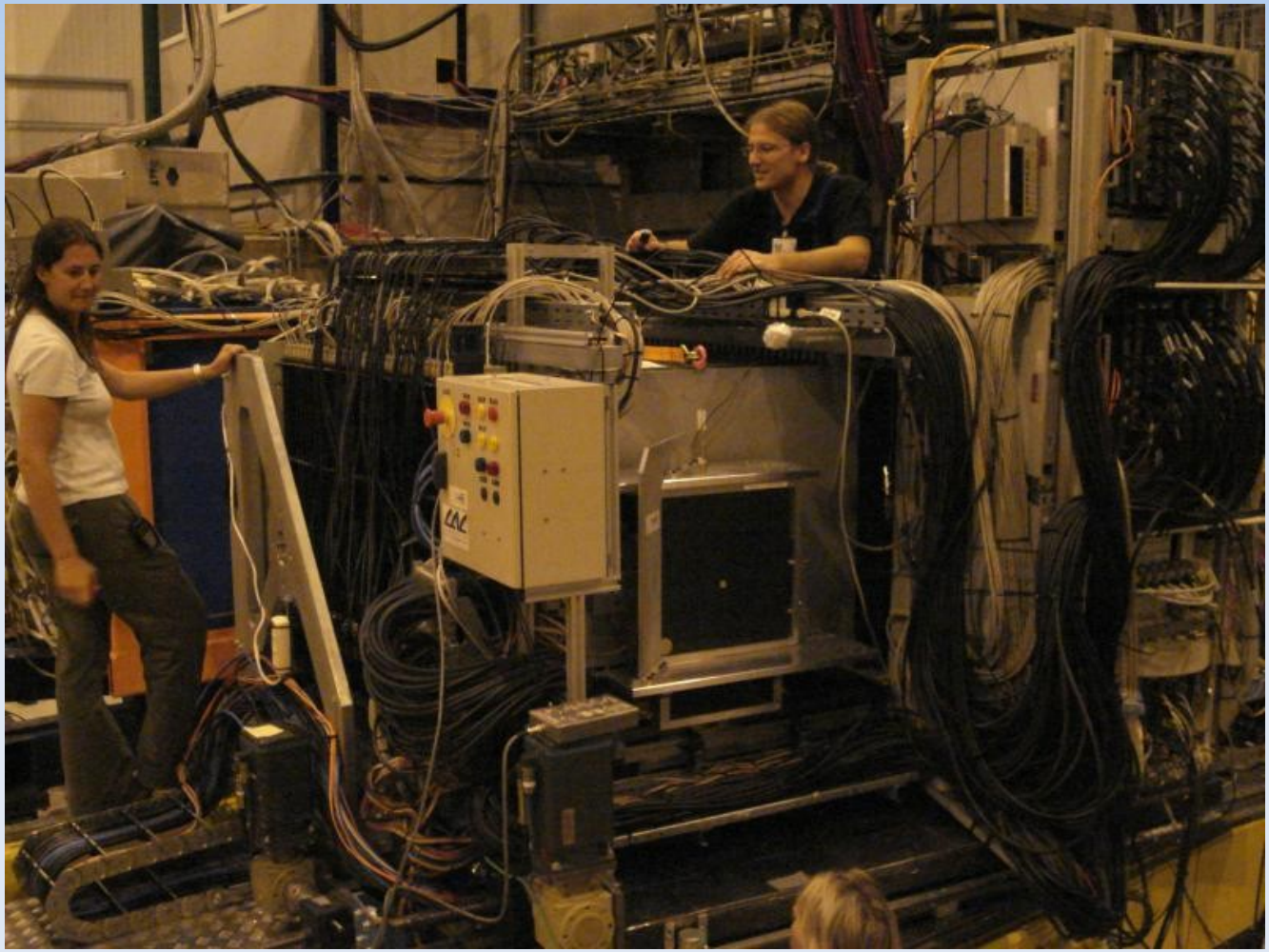
- EUDET Memos's
- Most of Code, Manual and HW description is available on CALICE twiki: https://twiki.cern.ch/twiki/bin/view/CALICE/CALICEDAQ
- Some part's of FW is still scattered on various SVN servers

Delivery

- HW ready to be delivered to labs
  - CCC already in use in 4 labs
- Wait another 1.5–2 months for v0 of complete FW and SW integration
  - Preparatory work on specific FW and SW can already start (≤1 month)

Installation

- mechanics
  - mod. VME crate for
    - DCC
    - CCC
  - Special box for LDA
  - Support for cables
- Final set-up not yet known:
  - stand alone SDHCAL
  - stand alone ECAL
  - Stand alone AHCAL
  - Combined test
- → 5 m long HDMI cables
  - halogen free;



Conclusions

- Technological prototypes of CALICE are getting close
  - All use 2nd version of ROC chips
  - Being integrated in large prototypes → extensive TB in 2011
    - 1 m³ SDHCAL in Spring; some ECAL slabs in cosmics & beam; some AHCAL slab in beam.
- **The DAQ will be ready for TB**
  - All HW elements available
  - FW & SW almost ready
  - SW: XDAQ survived natural selection (←→ DOOCS)
- Combined (with other system) ≥ 2012
  - Prepare HW and SW beforehand
    - SW & HW ←→ TLU & EUDAQ first

Big effort for CALICE!!
~15++ individuals from:
- UK: CAM, MAN, UCL, RHUL, Imperial
- FR: LLR, LAPP, IPNL
- DE: DESY