SiTRA-JRA2 activity: achievements and outcomes

Aurore Savoy-Navarro, LPNHE University Pierre et Marie Curie/CNRS-IN2P3

On behalf of the SiTRA –JRA2 activity:

Members: HIP Helsinki, LPNHE UPMC/CNRS-IN2P3 Paris, Charles University in Prague, IFCA/CSIC-University of Cantabria Santander

Partners: CNM-IMB Barcelona, Torino INFN and University, HEPHY in Vienna, IEKP Karlsruhe, VTT-Finland

Without forgetting to point out the instrumental contribution from all the SiLC R&D collaboration members

EUDET ANNUAL MEETING, FINAL MEETING, DESY, September 30th 2010

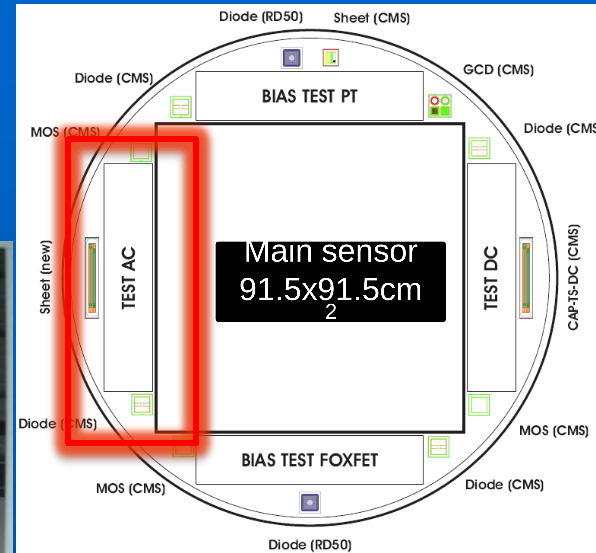
Outline:

- Building the Silicon test beam infrastructure
  - Modules construction
  - Front End Electronics
  - Faraday cage
  - alignment
  - 3D Table
  - DAQ
  - Analysis software
- Test beams
- Transnational Activities
- Outcomes & perspectives

SiLC Sensor order to HPK (end 2007)

SiLC Collaboration ordered at Hamamatsu (HPK):

- 30 pieces single-sided 6” wafer
- 5 pieces. alignment sensors of same layout, but hole for laser in backplane metallization



Specifications:

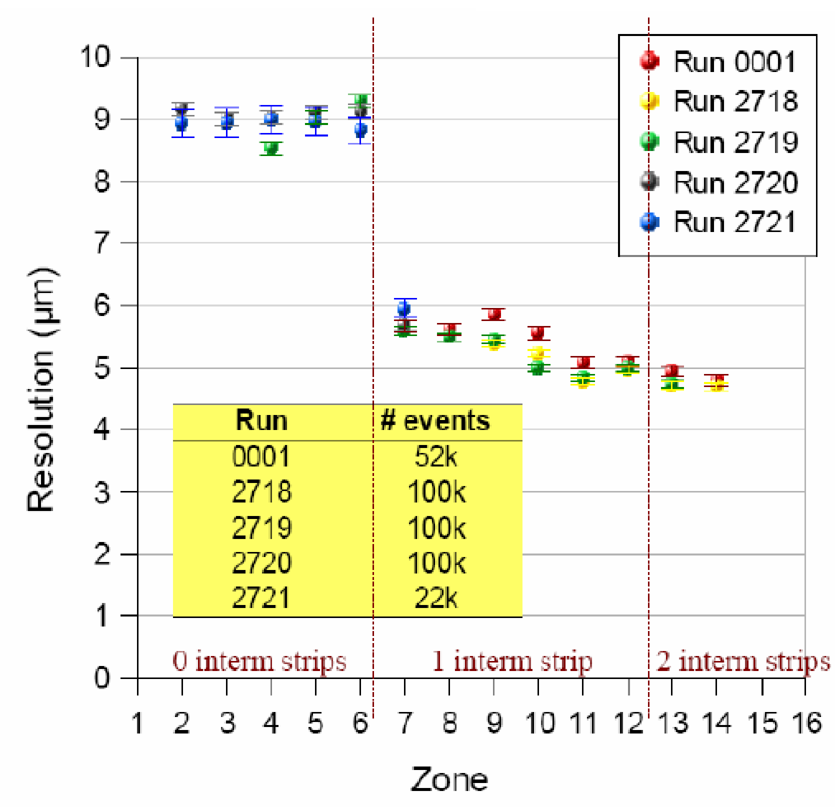
- Wafer thickness : 320 µm
- Depletion voltage around 75V
- 1792 AC-coupled strips, individu via poly-Si resistor (20MOhm)
- Strip pitch: 50 µm pitch,
- Strip width: 12.5µm
- No intermediate strips
- Additional test structures around the wafer

Already a new step w.r.t those in current LHC trackers.
HEPHY fully tested them in order to establish the next steps (test structures).
HEPHY & LPNHE built Si modules with these HPK sensors & characterize them in test beams (see later)

2008-09 SPS beam on test structures

CU Prague

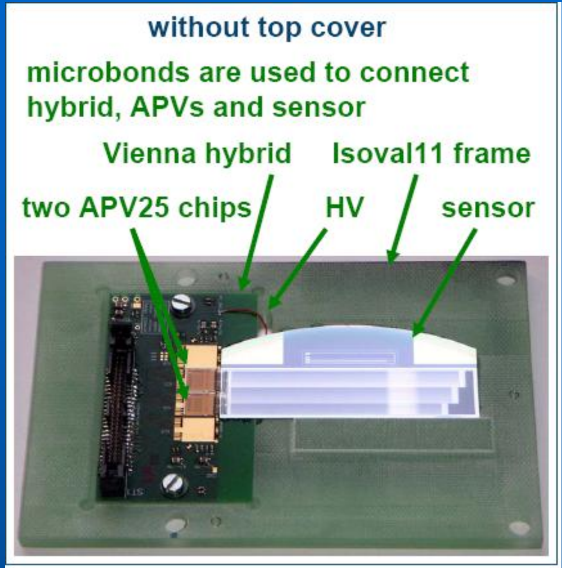
Spatial resolution vs strip geometry

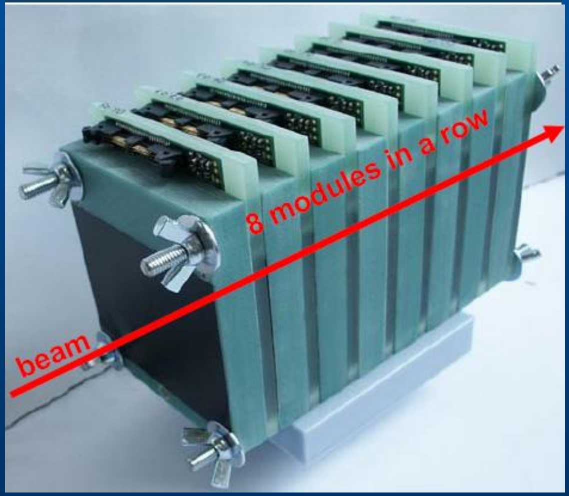


Run	# events
0001	52k
2718	100k
2719	100k
2720	100k
2721	22k

TESTAC:

strip width [µm]	intermediate strips
5	no
10	no
12.5	no
15	no
20	no
25	no
5	single
7.5	single
10	single
12.5	single
15	single
17.5	single
5	double
7.5	double
10	double
12.5	double





- 9 µm resolution if no intermediate strip
- 5 or 6 µm resolution if 1 or 2 intermediate strip

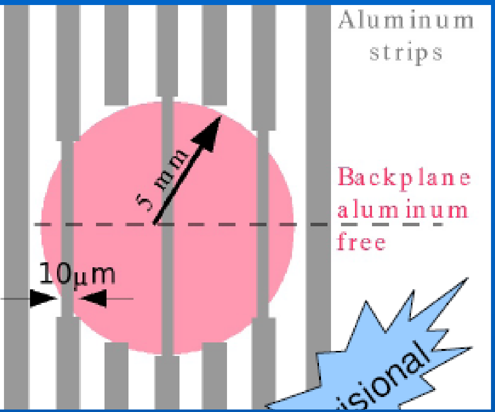
HPK strip sensors for alignment

<u>Implemented</u>:

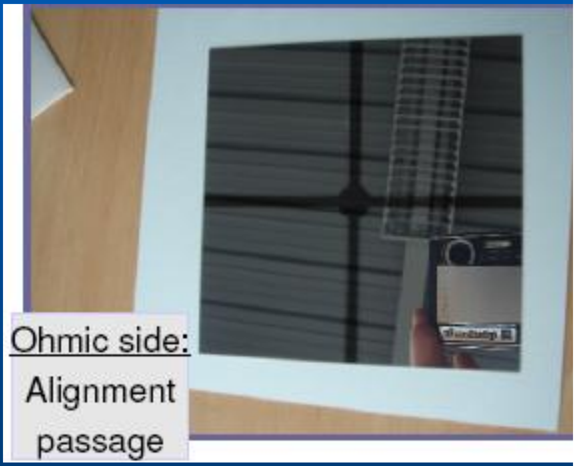
- ∅~10 mm window where Al back-metalization has been removed

<u>Suggested (not cost effective for small batches)</u>:

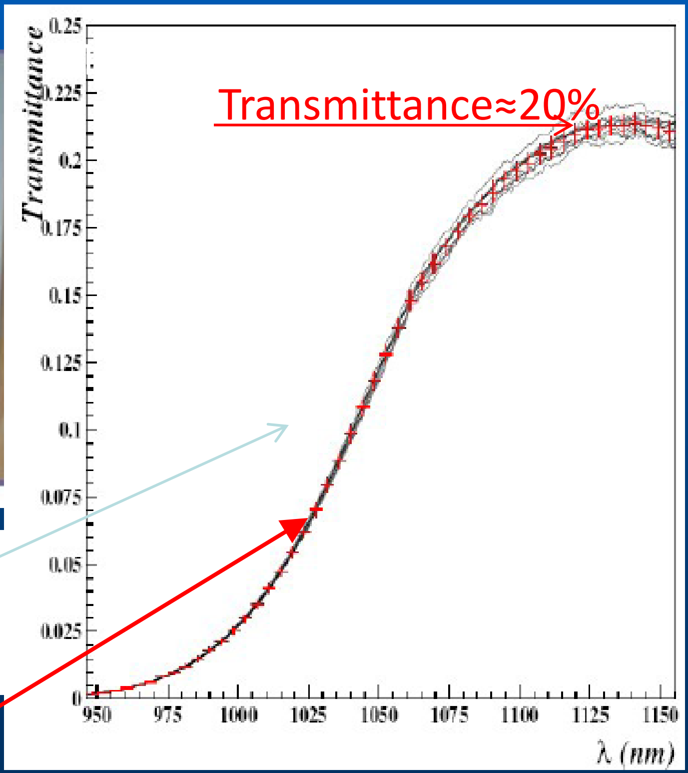
- Strip width reduction (in alignment window)
- Alternate strip removal (in alignment window)



A.F. HPK used to make the alignment system



- They are alignment friendly, but not optimized for transmittance: no Anti-Reflection Coating (ARC).

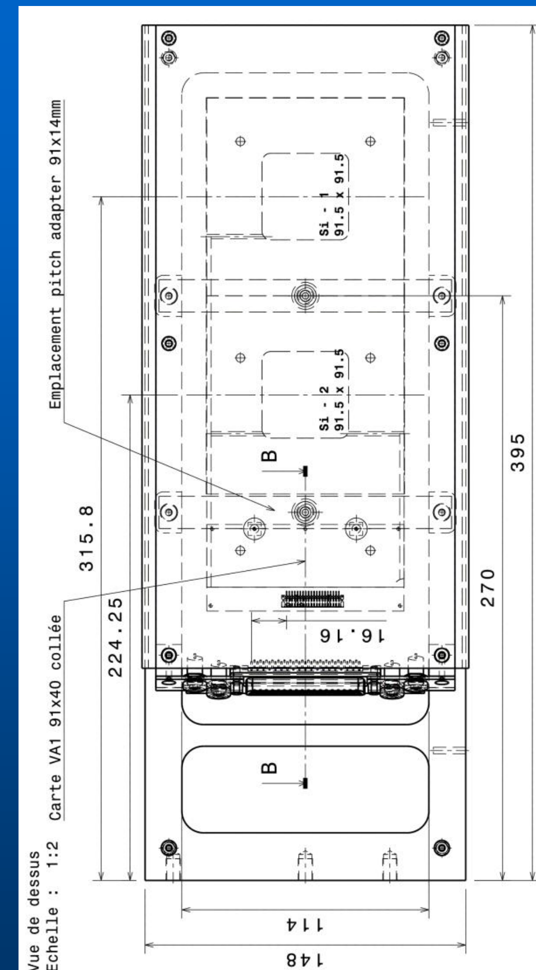


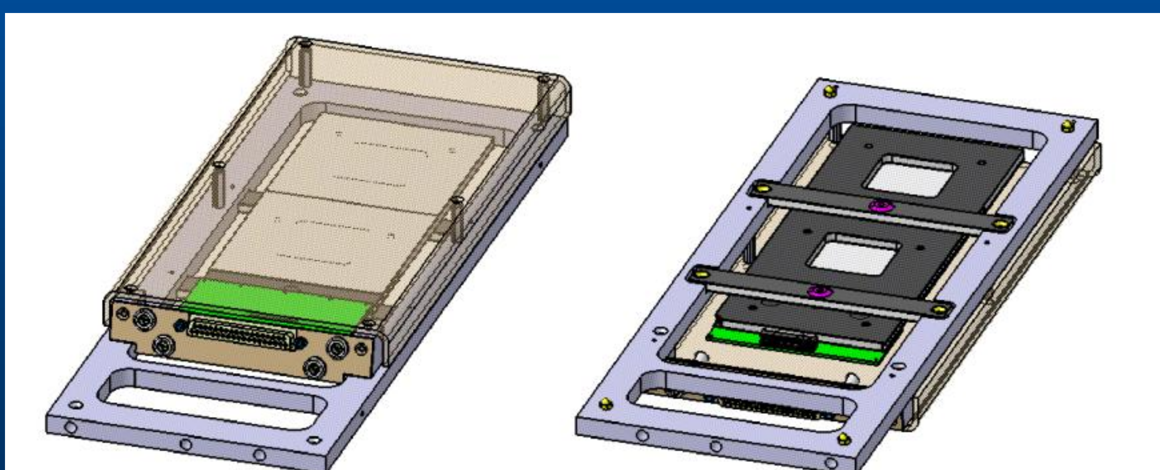
Fully characterized at Lab test bench & May 2010 at CERN SPS

Module construction: Mechanical conception

Module are made of one or more sensors and constructed
With a conservative approach, i.e.:

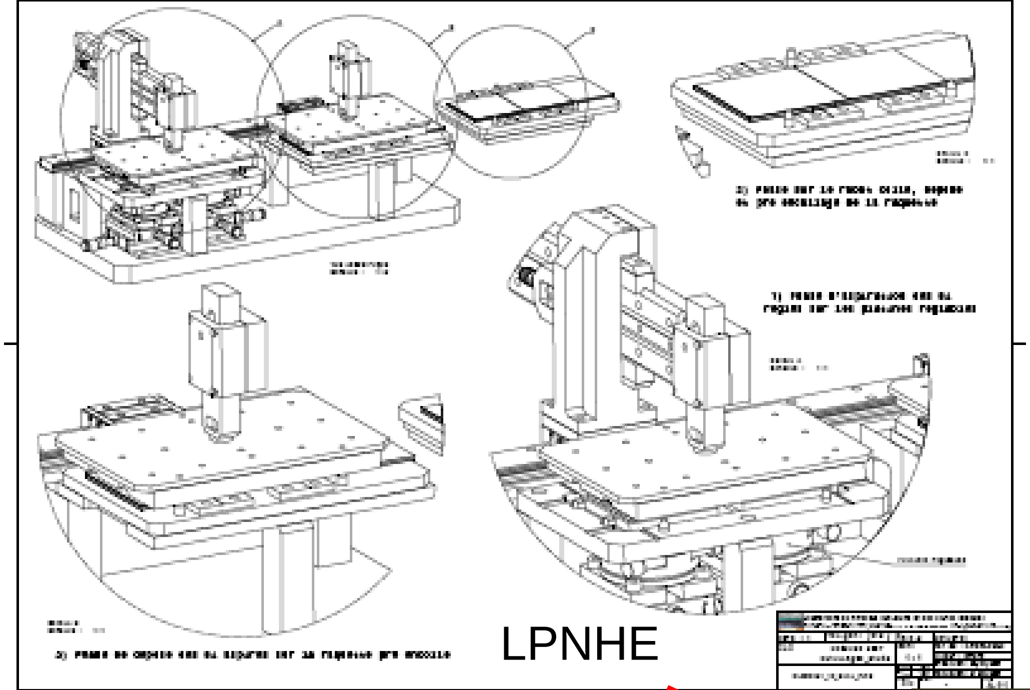
- F.E. Hybrid board ensure some flexibility for connection with front end electronics (depending FE ASIC)
- Choice of robust support structure to ease numerous manipulations at test bench or test beam
- Protection box for transportation or storage.

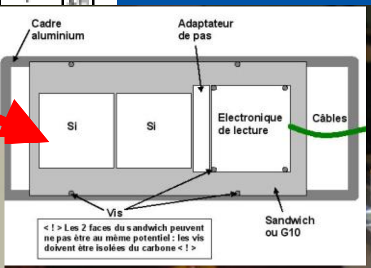




Tools for construction of modules:

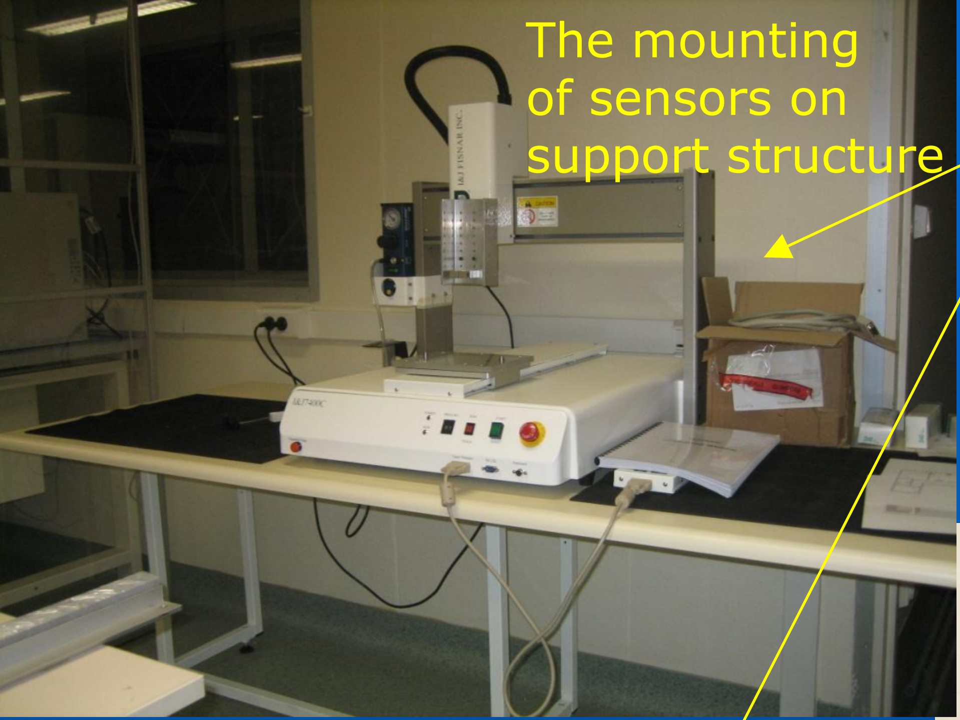
- Need for developing new expertise & tooling at LPNHE and
- Bonding Lab at CERN
- Existing expertise & tooling: IEKP , HEPHY

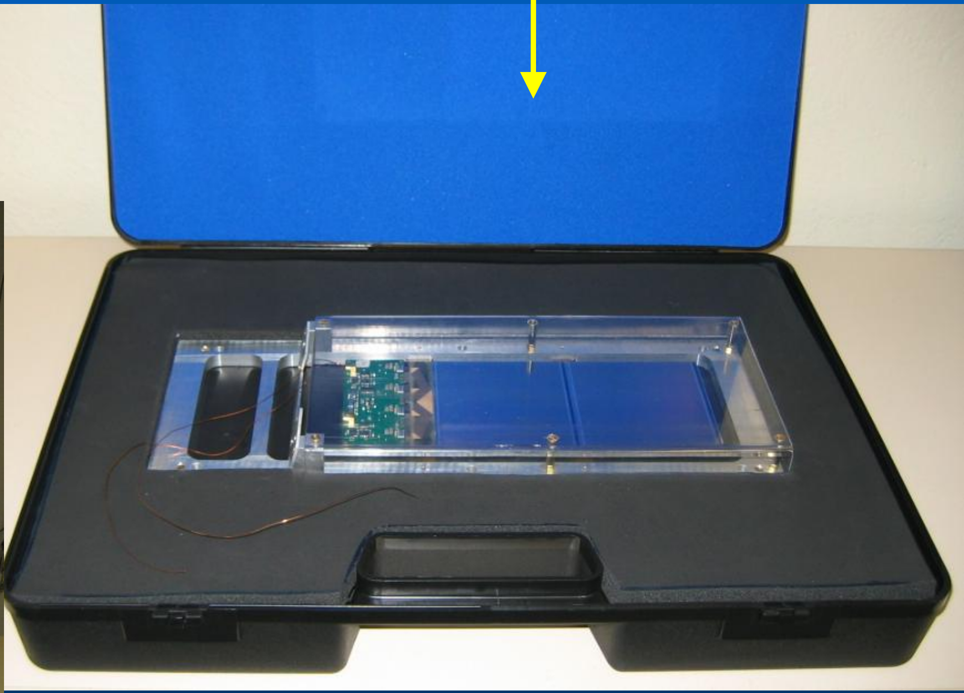




The fabrication and the module

(LPNHE)



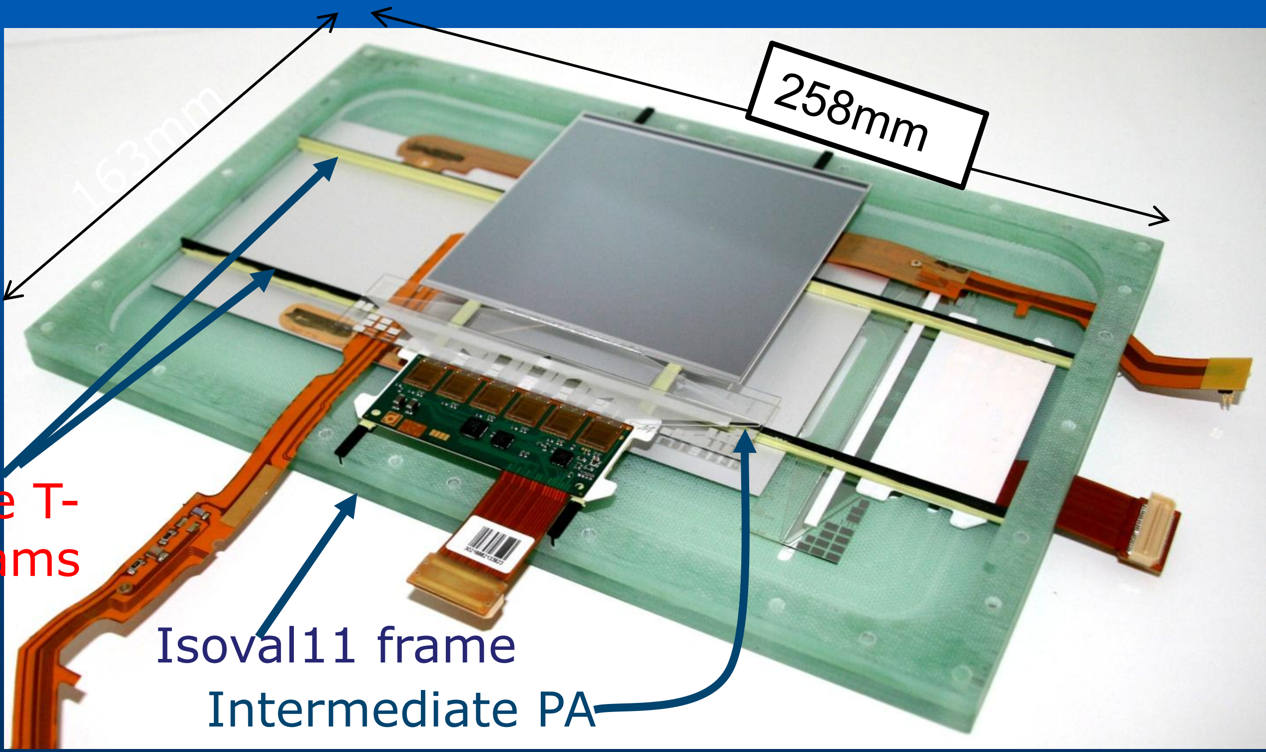


MODULES BUILT for LPTPC *(IEKP+HEPHY)*

- aluminium on quartz **Intermediate Pitch Adapter** to connect the CMS R2 pitch of 143 μm to the readout strips of the HPK sensor with a pitch of 50 μm - Helsinki Institute of Physics (HIP)
- two **carbon fibre T-beams** are the backbone of each silicon detector – 2 rectangular beams from SECAR Technologies glued together

- **Isoval11 frame**: a composite of resin epoxy reinforced with a woven fibreglass material

Total thickness: 18mm



Detector Modules

(HEPHY) –LCTPC test

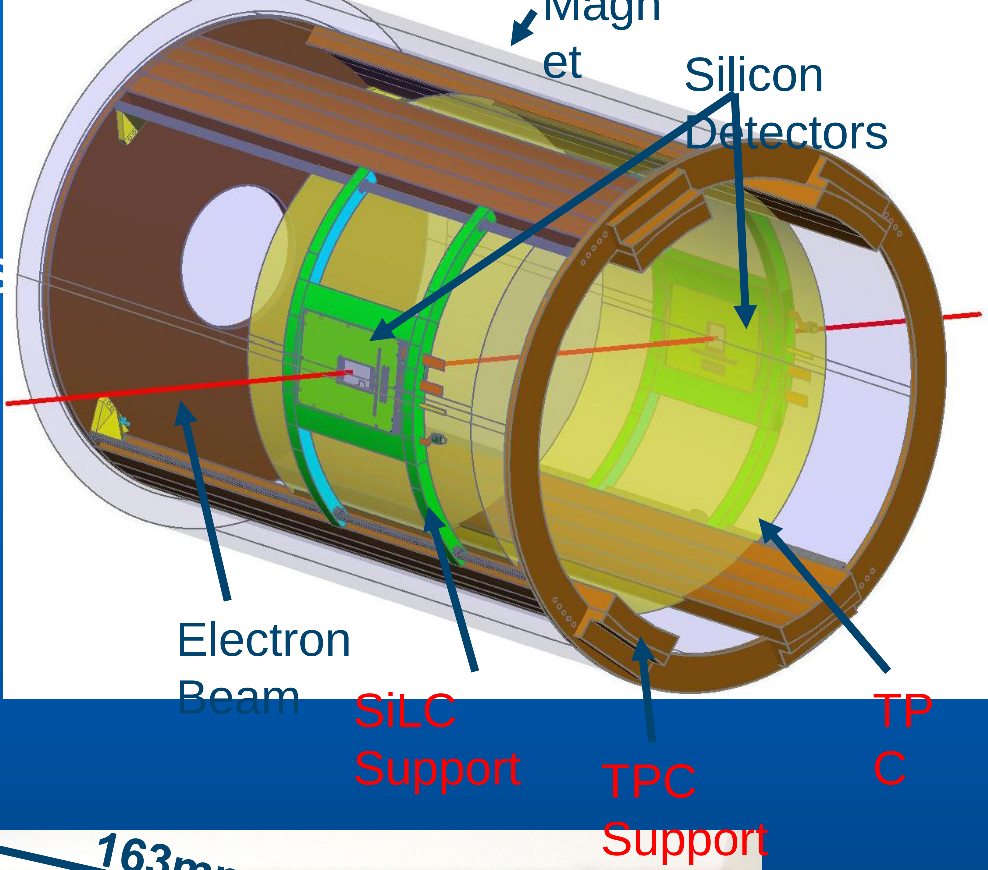
Final detector module **thickness**

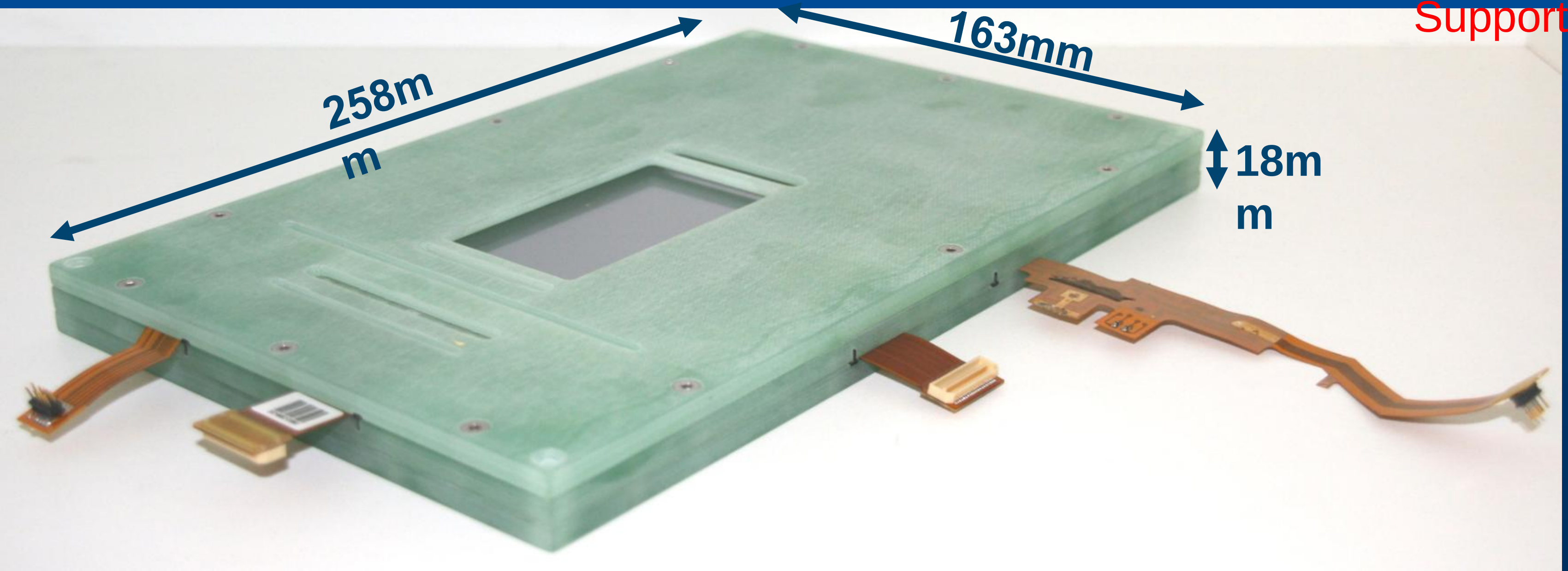
18 mm + about **2 mm** for a light

-tight adhesive foil

- safety clearance of 4 mm to

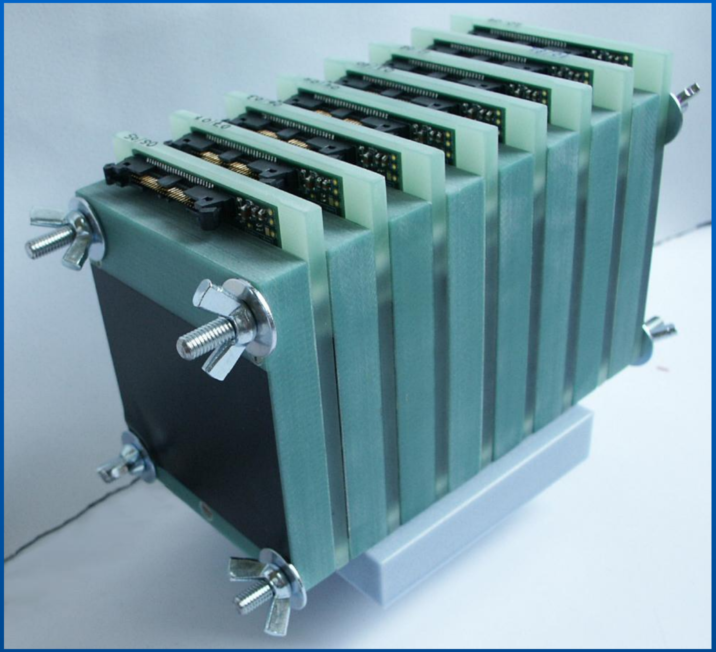
the TPC and the magnet

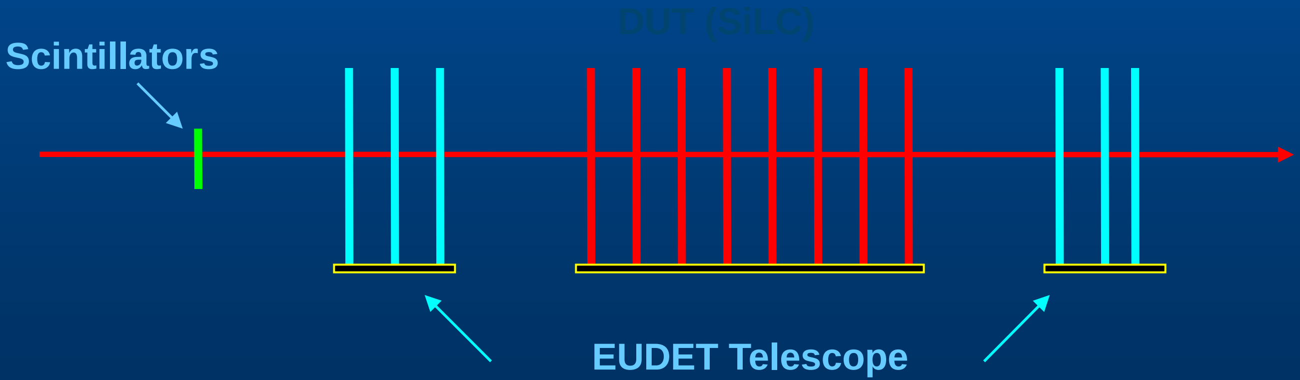




Module Stack

- 8 Modules have been screwed together
- To be mounted in between EUDET telescope
- Stack of 8 modules would allow us autonomous tracking





Faraday and cooling cage

F.E.E. General description

Full readout chain integrated in one chip developed in two steps

EUDET BASELINE

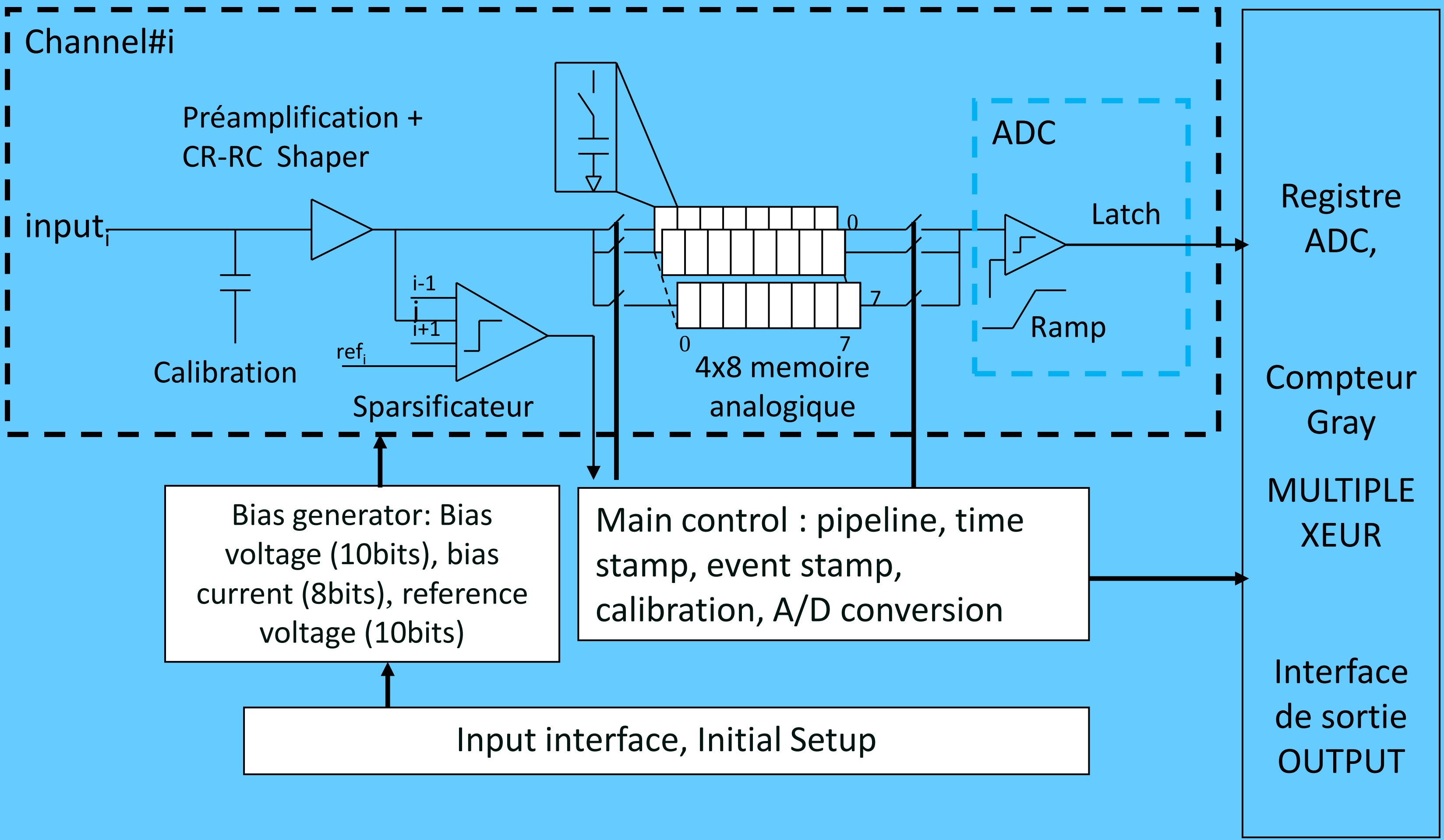
- Preamp-shaper
- Sparsification : Trigger decision on analogue sums
- Sampling : 8-deep sampling analogue pipe-line
- Analogue event buffering: : Occupancy: 8 deep event buffer
- On-chip digitization : 8-bit ADC
- Calibration and calibration management

BEYOND

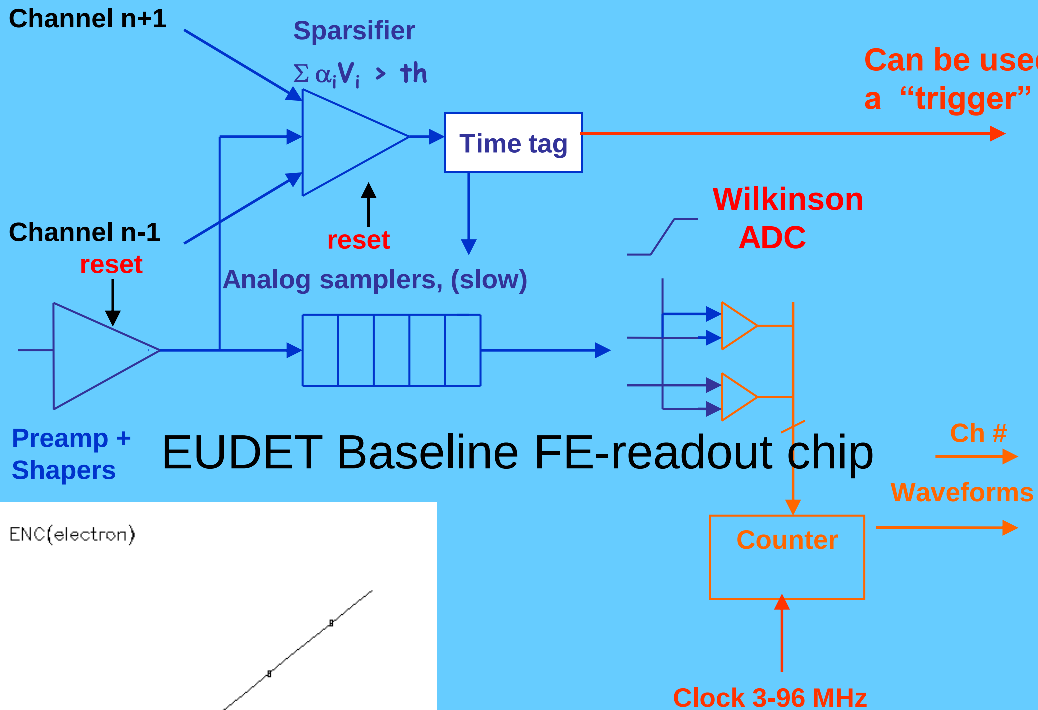
- *Full digital handling of the chip running operation*
- *Power switching (ILC duty cycle)*
- *Fault tolerance*

In addition: two “conventional” FE ASIC: VA1’ and APV25

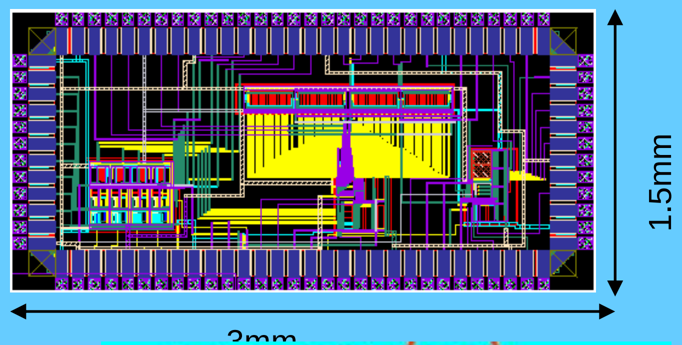
Ultimate goal: Developing a mix-mode FE readout with pulse-height reconstruction, zero suppression, full digital control (highly fault tolerant, flexible/robust) power cycling, in DSM CMOS technology

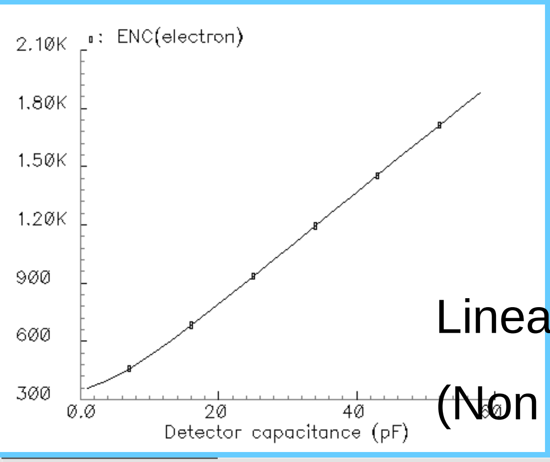


SiTR_130-4



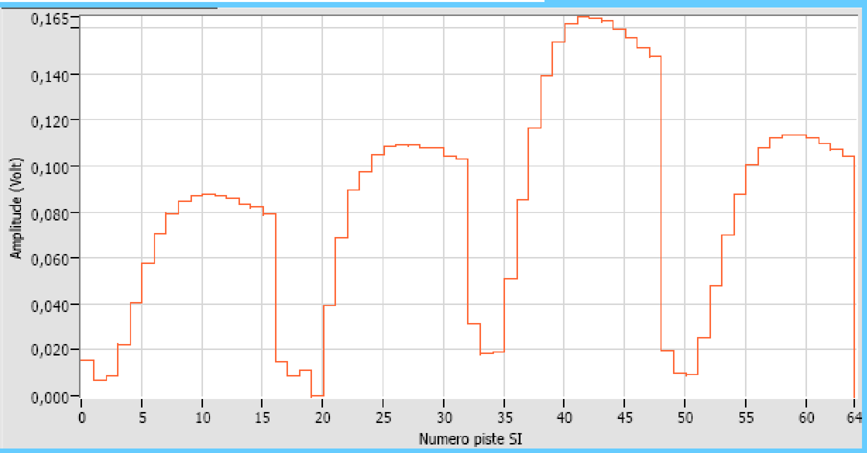
EUDET Baseline FE-readout chip



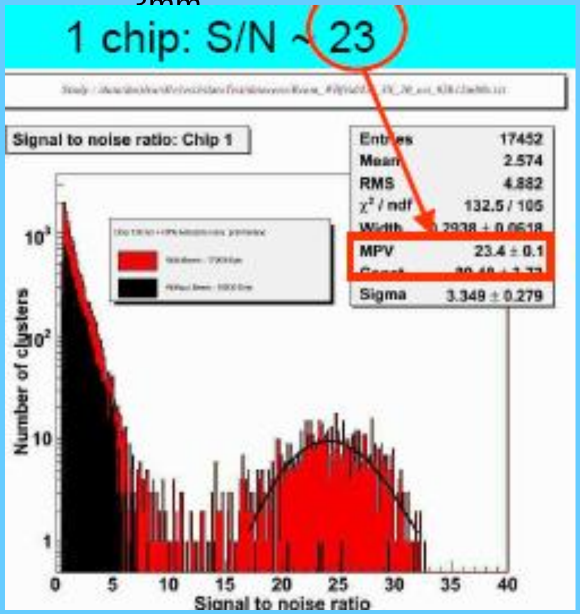


Linear up to 23MIP

(Non linearity 5%)



SPS-CERN
Nov 2007

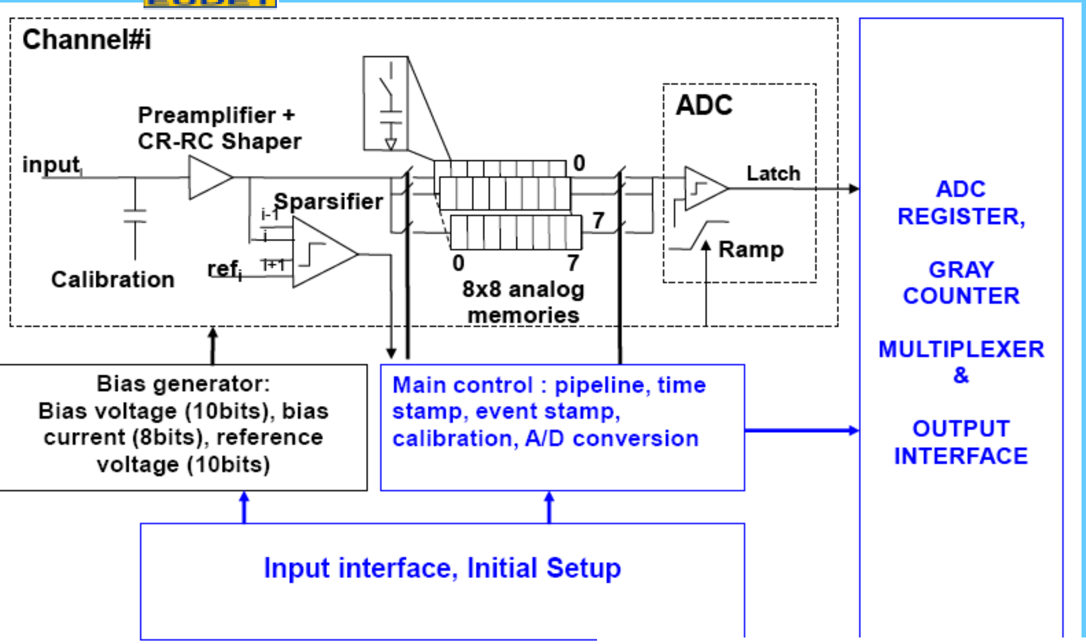


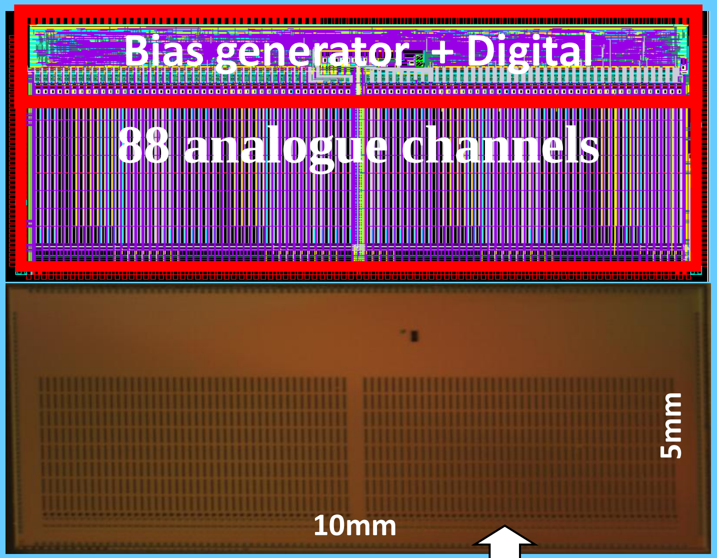
HPK sensor, MPV of S/N = 23

(4 channels clustering with refine algorithm)

(9.15x2=18.3 cm strip length)

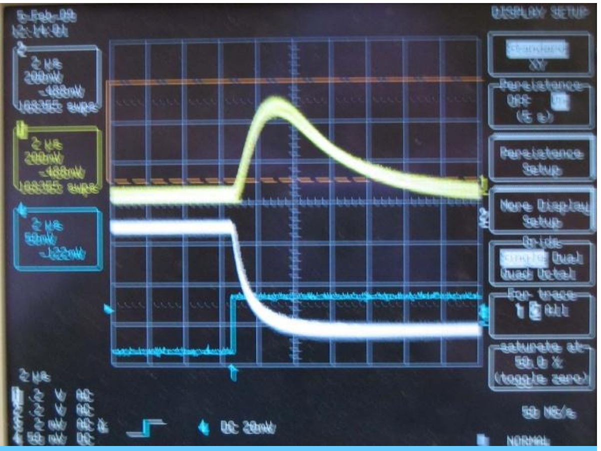
Beyond #1: SiTR_88-130UMC version

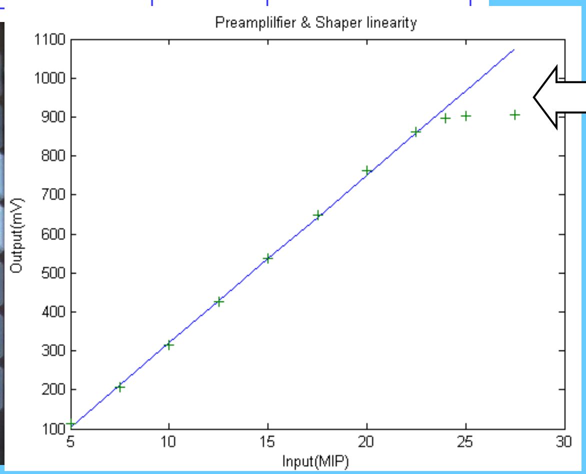




SiTR_88-130 first full mixed mode analogue/digital achieved Using DSM CMOS UMC 130nm

Analogue part well within the specs.





Overall power dissipation per channel: 1.2mWatt

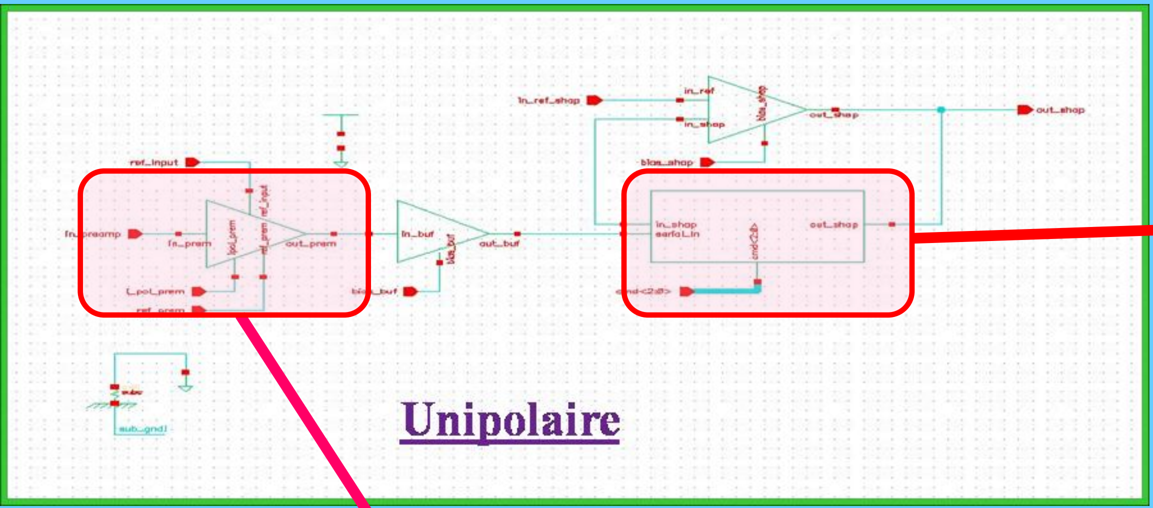
BEYOND #2: Development of SiTR_130IBM-128 full mix mode FE readout ASIC

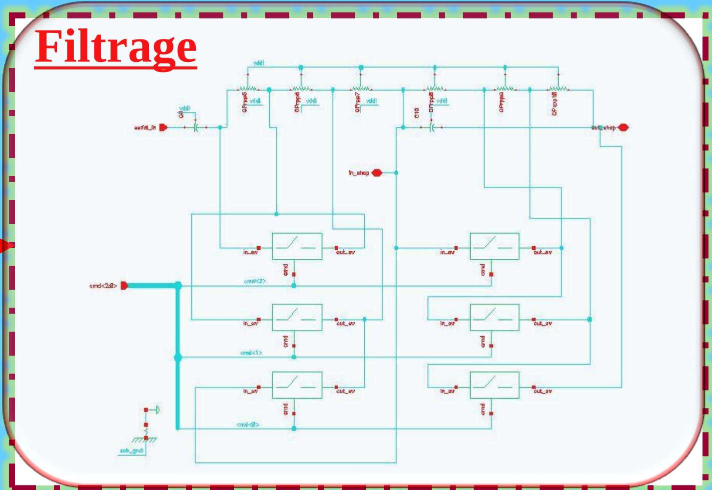
SITR _BLOCS

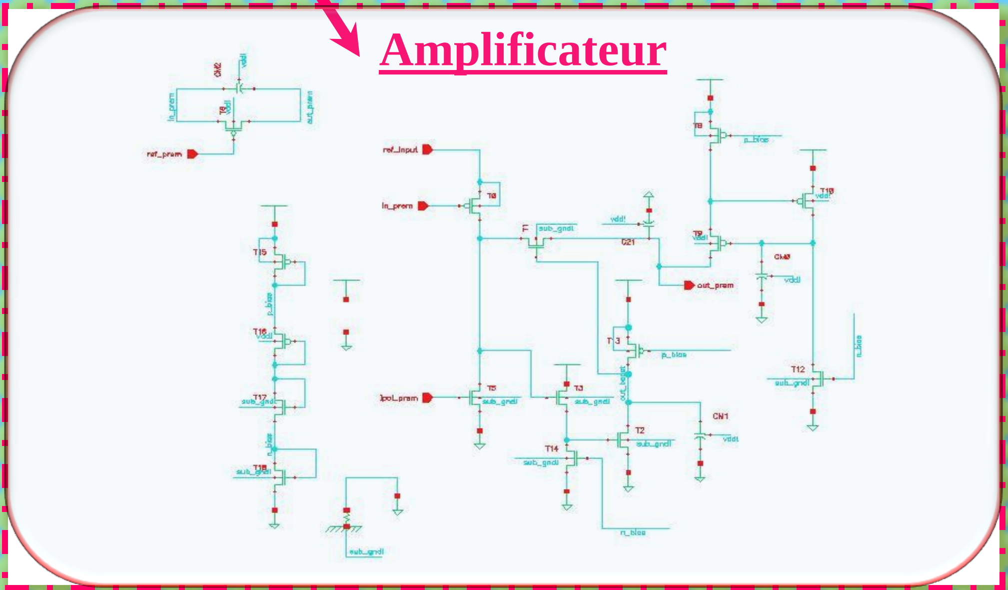
- Revised Design of the main components of the analogue FE architecture of the SiTR ASIC, following the recommendations of the Review Committee of March 15, 2010 (International experts from CERN and E.U. Institutes).
- Work performed at LPNHE with collaboration of Microelectronics Pole Alsace (T.H. Pham & Software experts) and CERN Microelectronics Group
- CMOS IBM 130 nm (1.5 V)
- 3 different amplifier-shaper designs (CR-RC programmable; 3 bit)
- Single ramp Wilkinson ADC (8 bits)
- Analogue memory cell with write/read switches.
- Successfully submitted to IBM Foundry via CERN on June 15

Amplifier - Shaper V1

Rachid Sefri
Thanh Hung Pham







Gain : 19.4 mV/MIP

Sh _Time: 600ns – 1us

Noise @ 1 us : ~ 346 + 19,5 e/pF

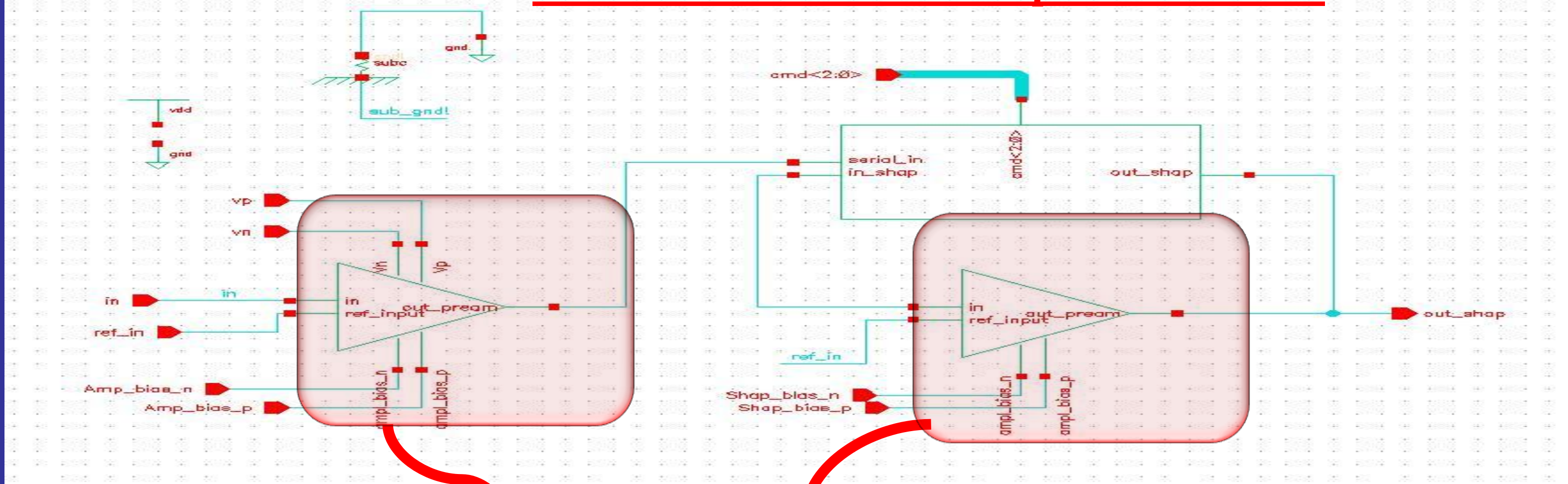
Linearity < 1% (15 MIP)

Power dissipation: 450 uW

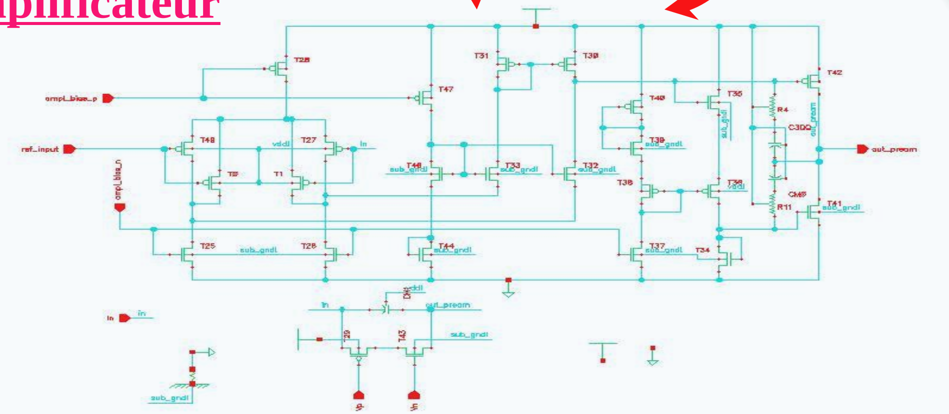
Amplifier - Shaper V2

Rachid Sefri
Thanh Hung Pham

Différentiel en entrée et unipolaire en sortie



Amplificateur



Gain : 20 mV/MIP

Sh _Time: 550ns – 1us

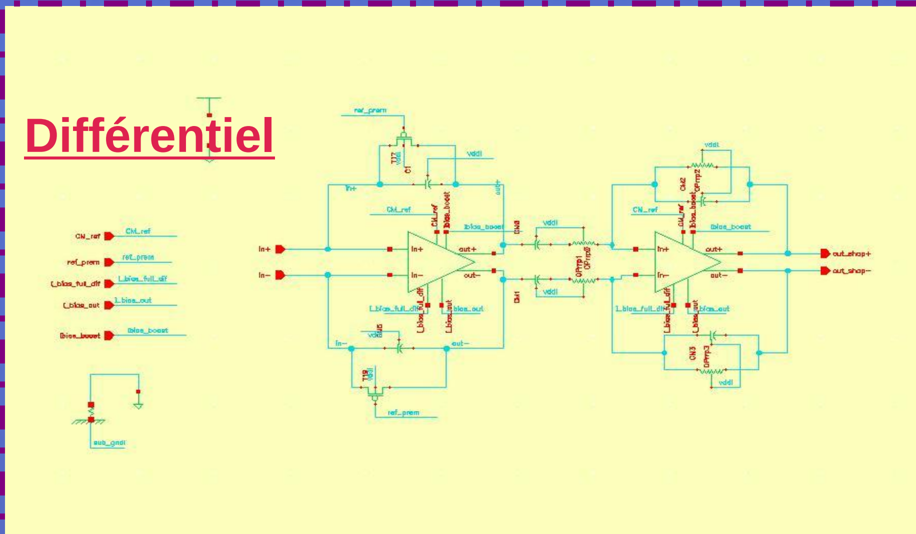
Bruit @ 1 us : ~ 189 + 18,9 e/pF

Linéarité < 1% (15 MIP)

Consommation : 334 uW

Amplifier - Shaper V3

Rachid Sefri
Thanh Hung Pham



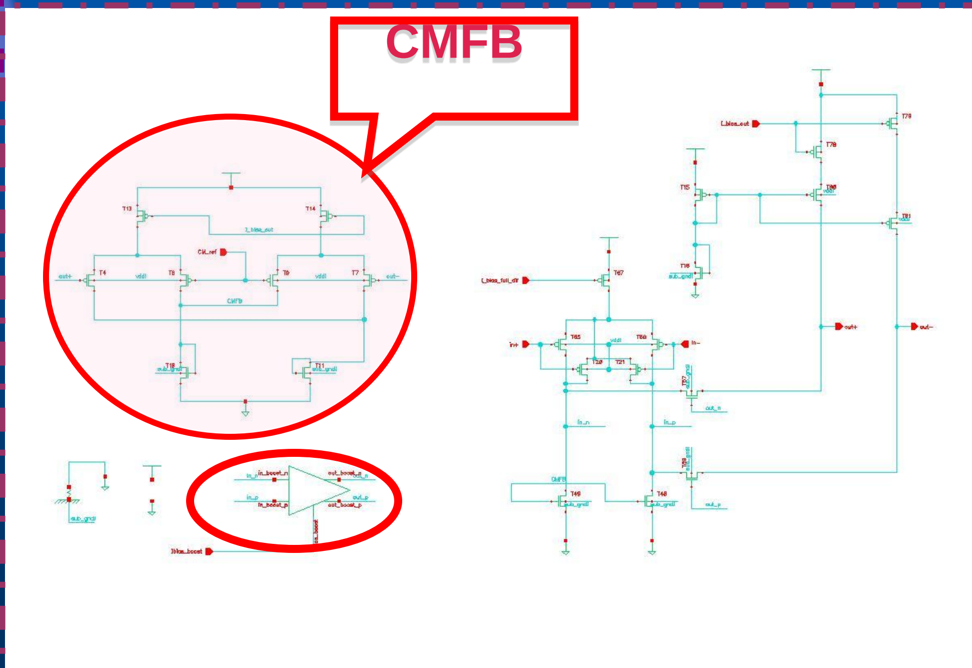
Gain : 20 mV/MIP

Sh _Time: 700 ns – 1 us

Bruit @ 1 us : ~ 698 + 17.7 e/pF

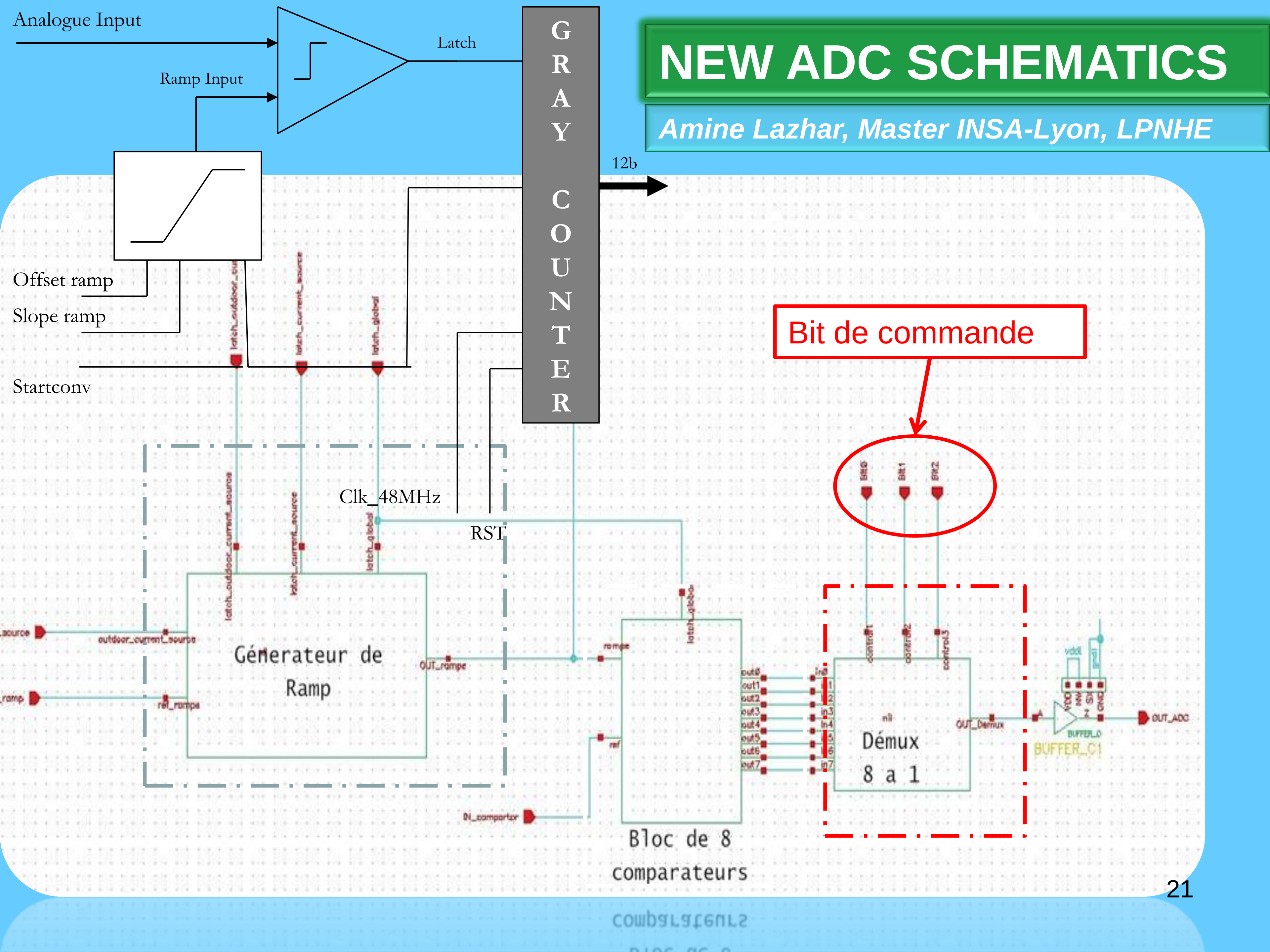
Linéarité < 1% (15 MIP)

Consommation : 540 uW



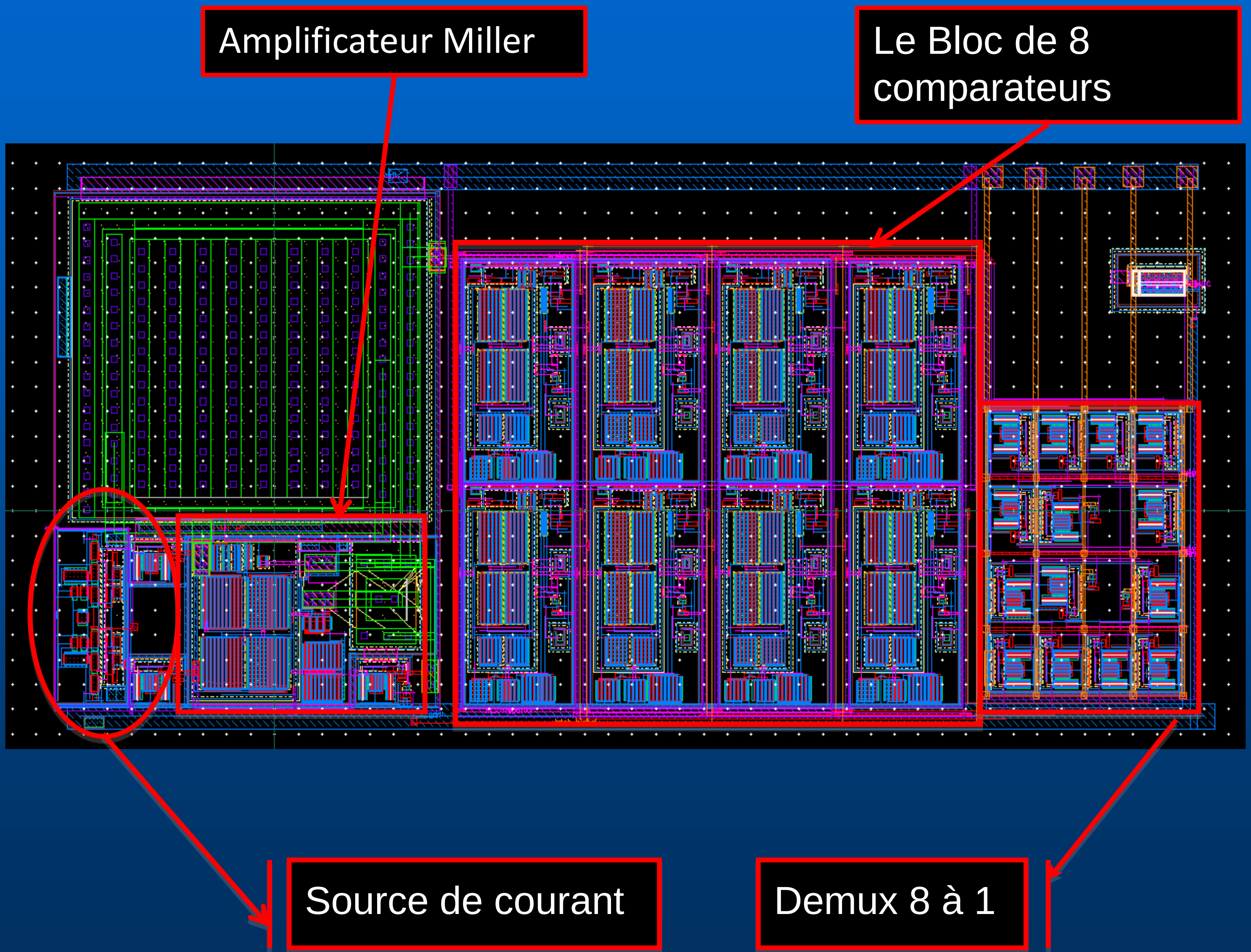
NEW ADC SCHEMATICS

Amine Lazhar, Master INSA-Lyon, LPNHE



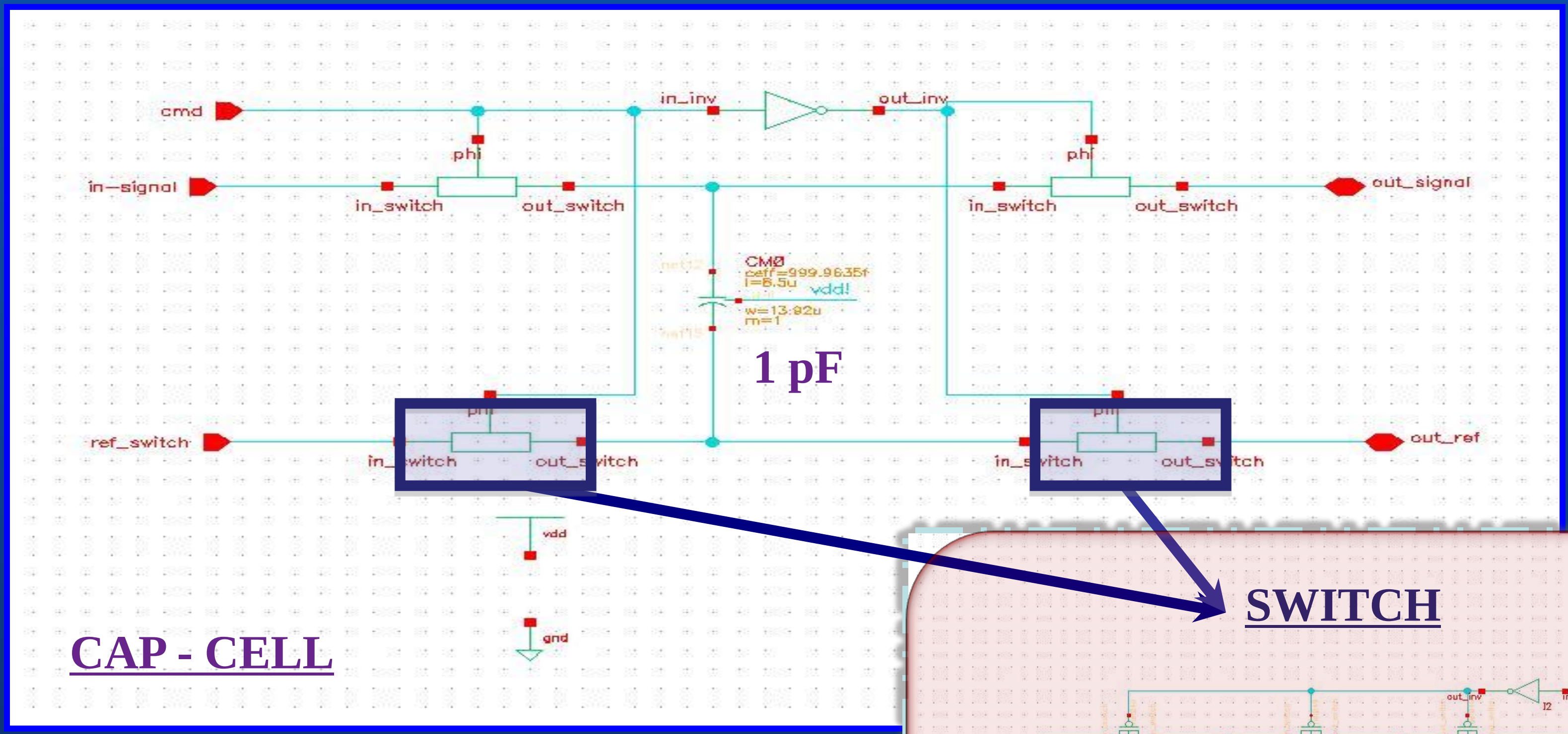
New ADC Layout

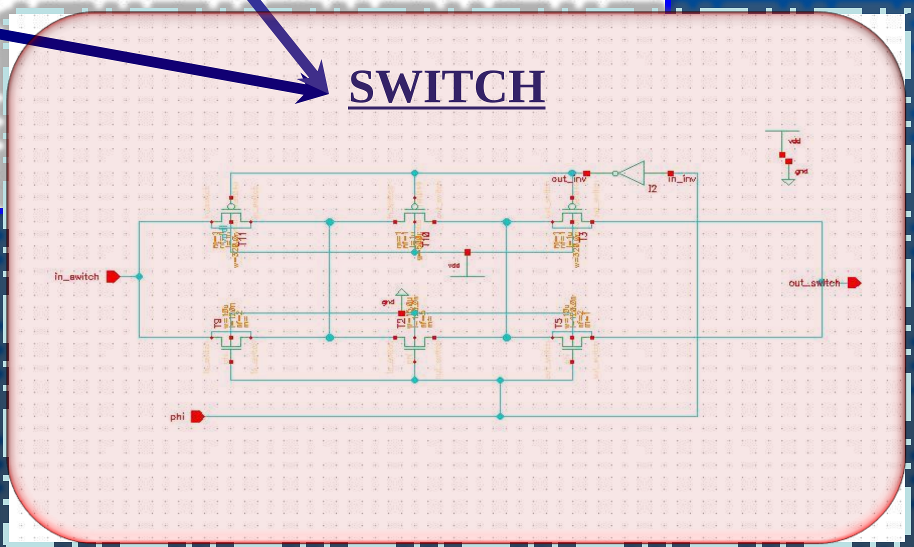
Amine Lazhar, Master INSA-Lyon, LPNHE



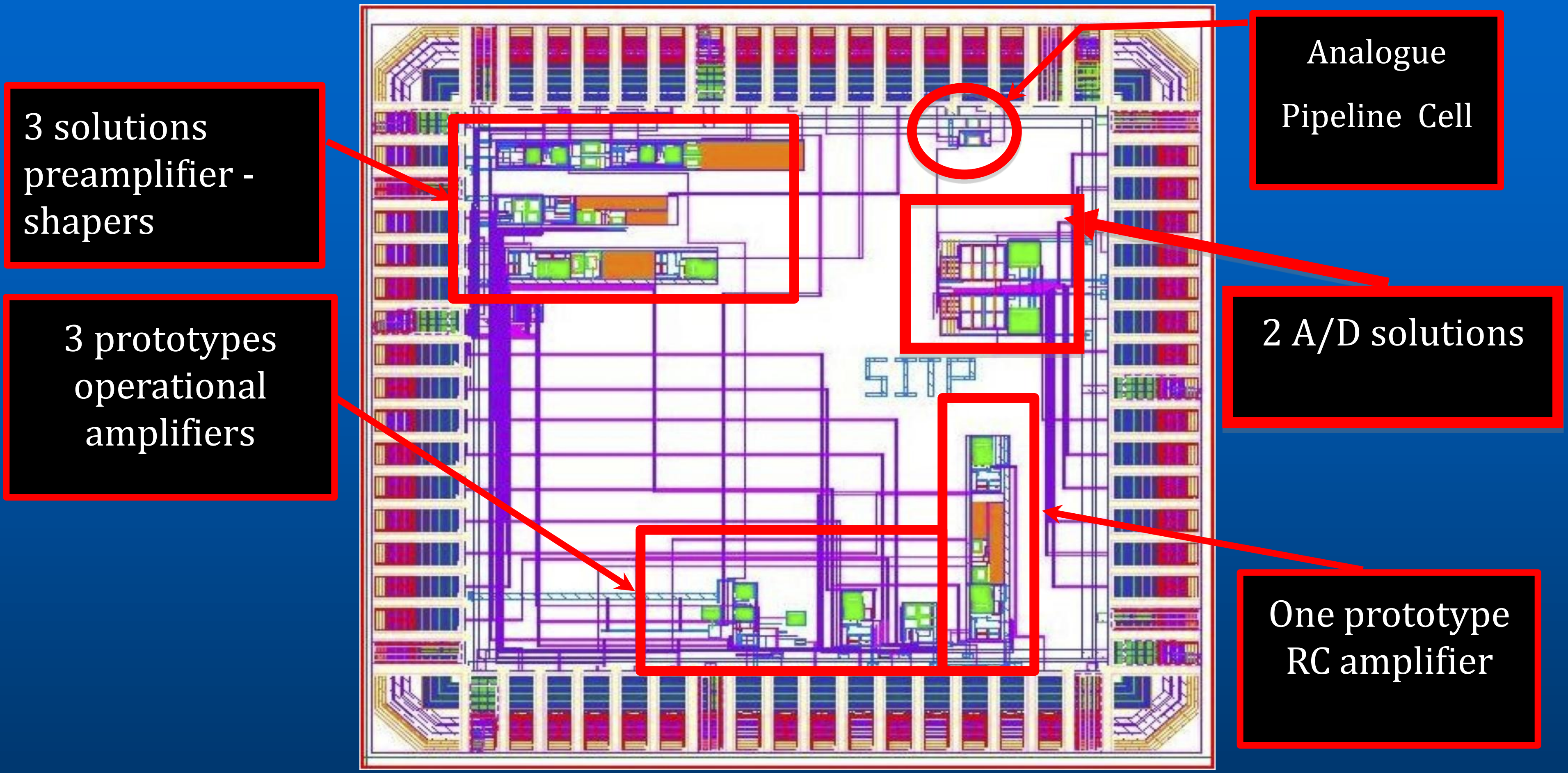
Analogue Memory cell

Rachid Sefri

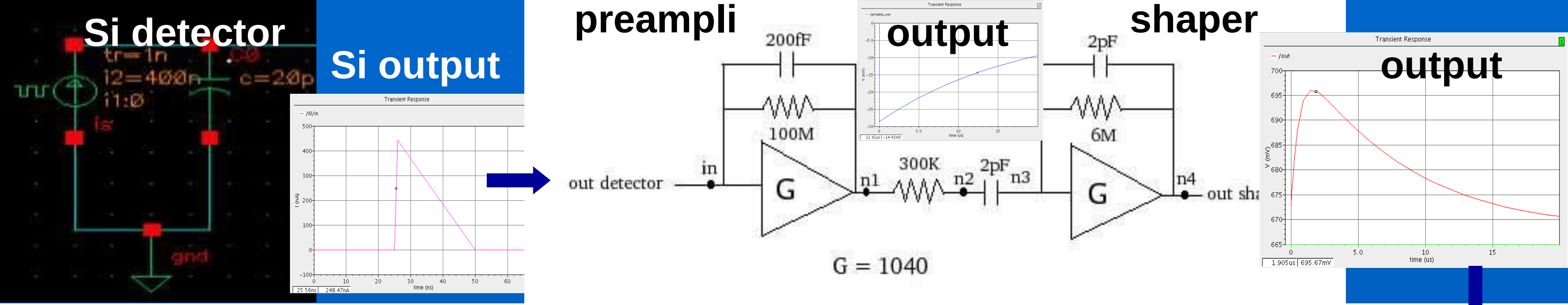


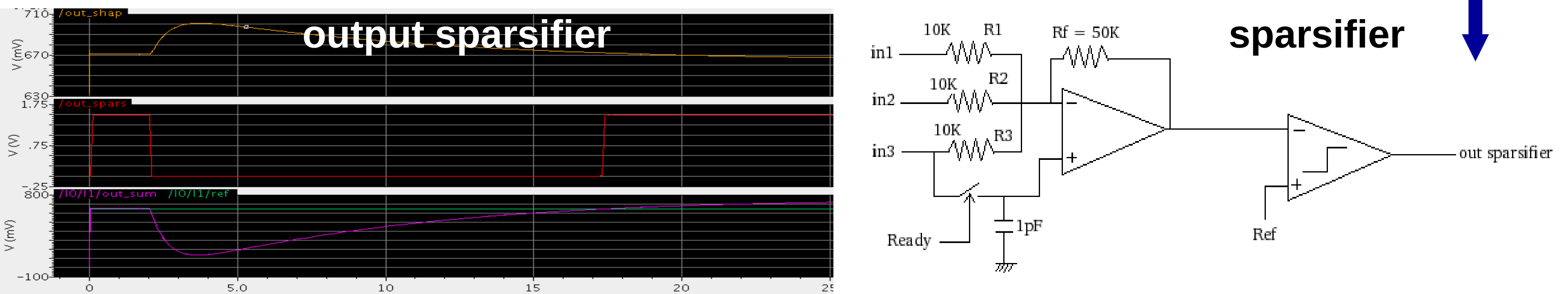


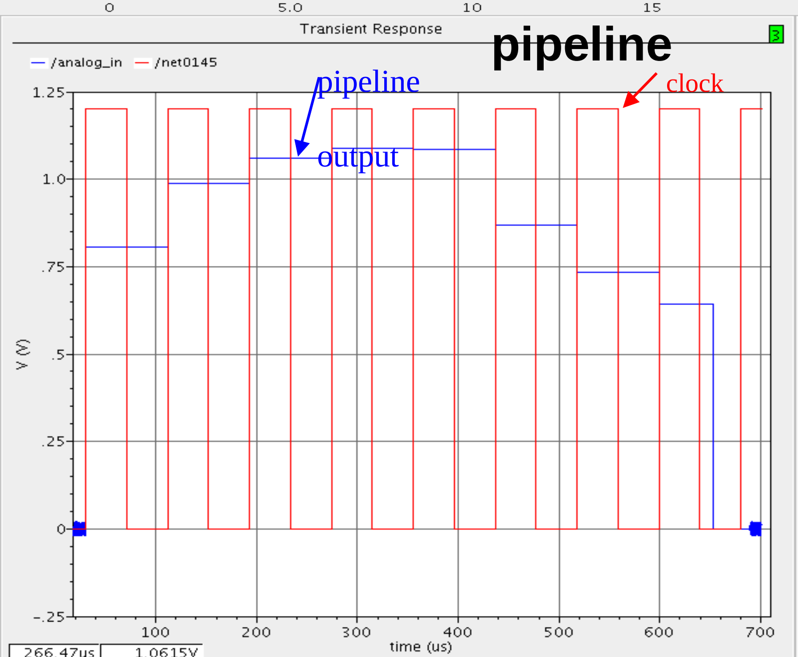
SiTR_Blocs Layout

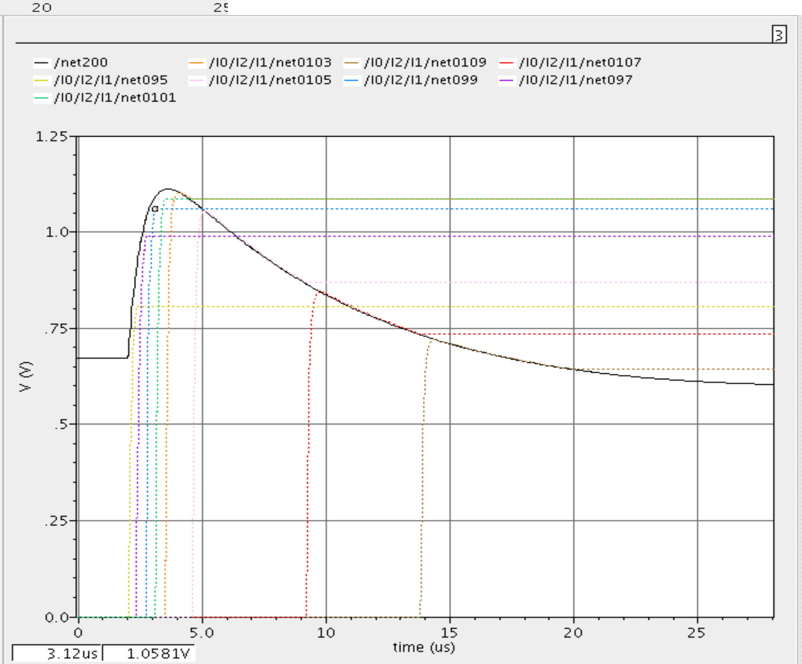


- Area= $4mm^2$
- 68 Pads (17 pads*4).
- ***Submitted to IBM Foundry June 30, 2010***



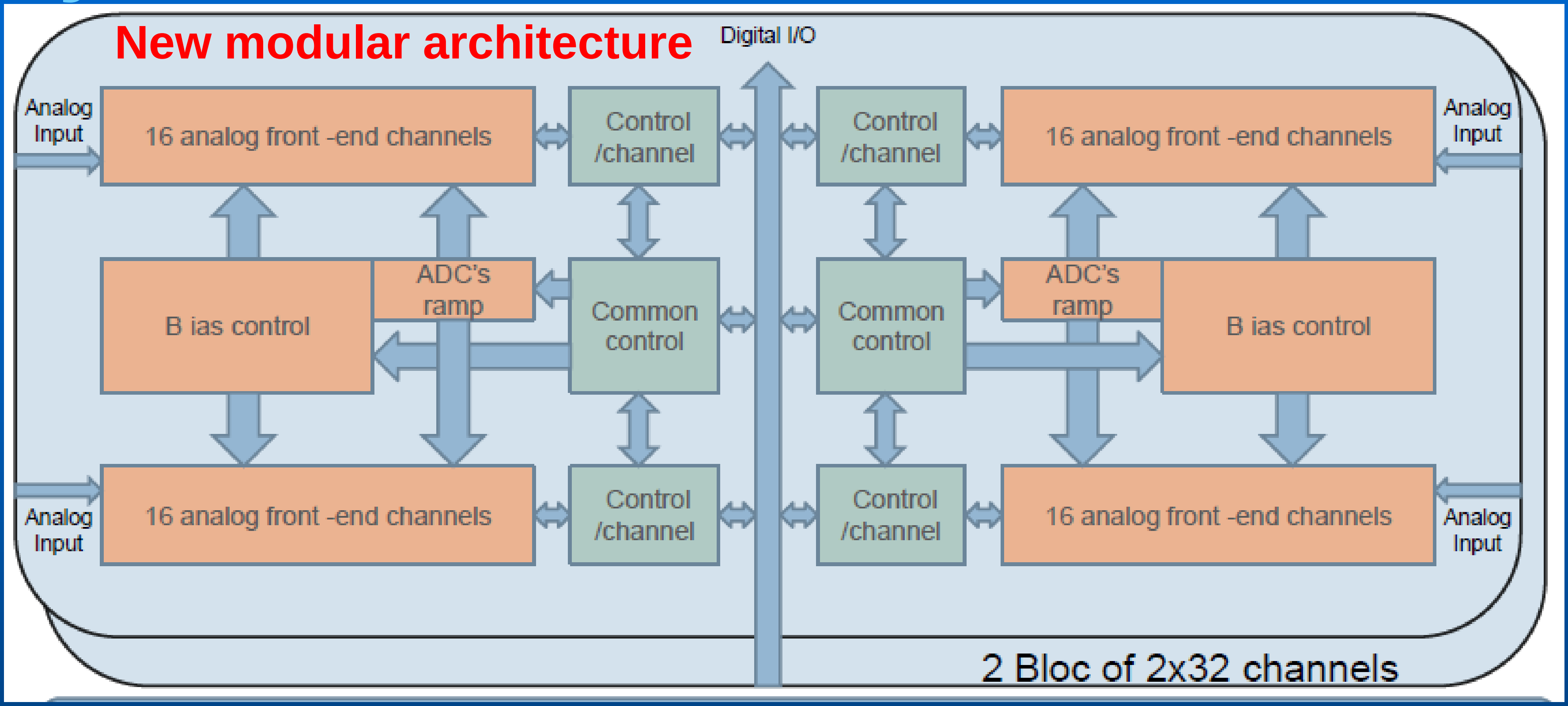






Mixed Analogue/ Digital => SiTR Chain Modeling

Beyond baseline: the 128 ch Si-FE ASIC

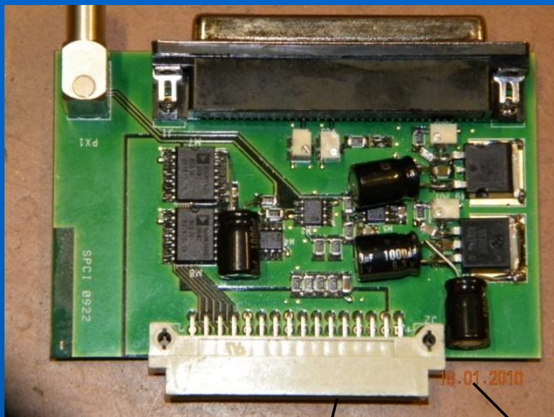


Beyond the SiTR_130-UMC deliverable achieved in 2008 with test beam on Si prototype, a new version is developed in two steps and aims to a full mix mode Analogue/Digital chip

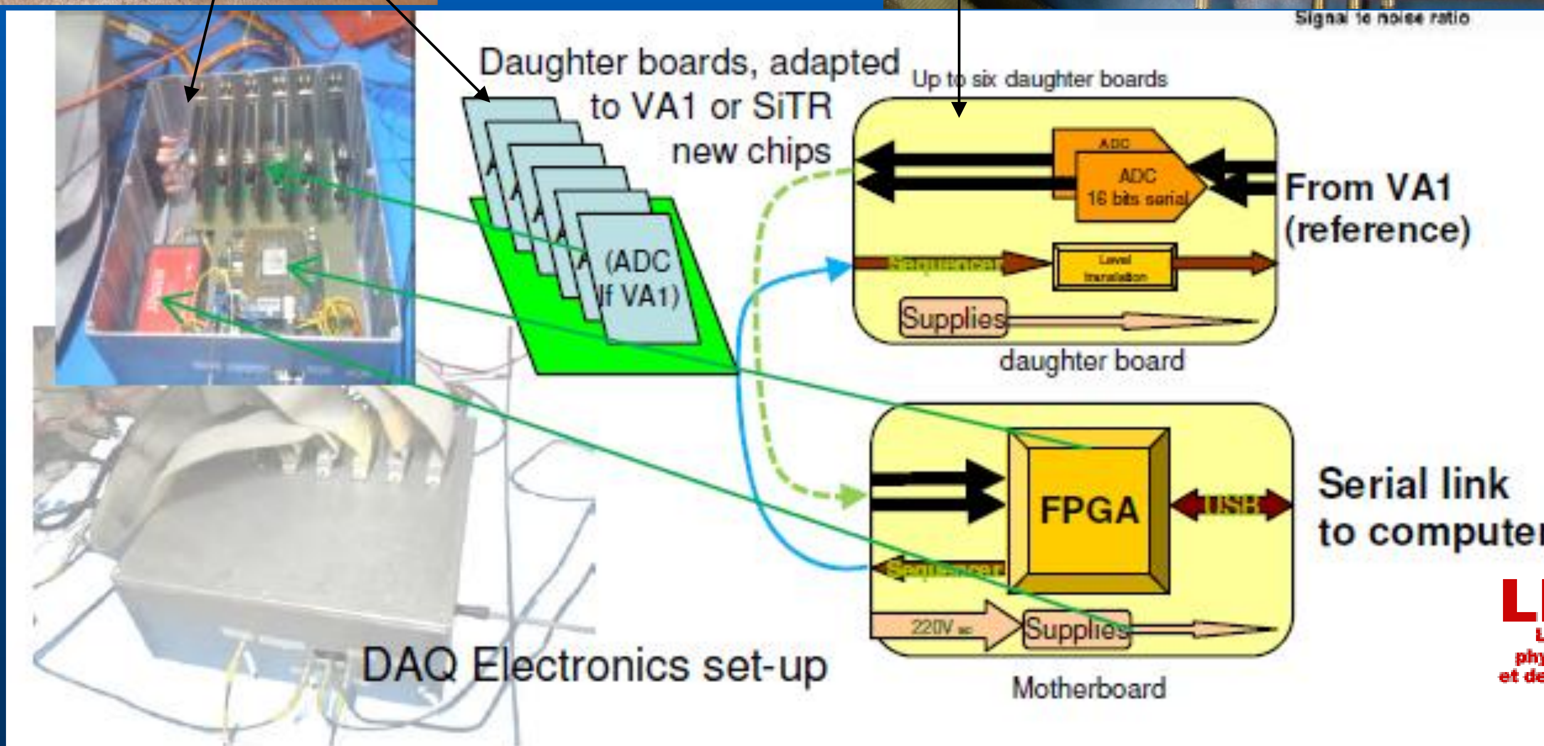
- The first step was keeping the UMC technology -> SiTR_130-88
- The second step now underway, with IBM-130 technology and upgraded analogue FE & digital parts will give the 128 ch ASIC. This chip will then be able to equip larger size Si prototypes, these coming years.

It is also requested for other applications (see section on outcomes)

DAQ Electronics

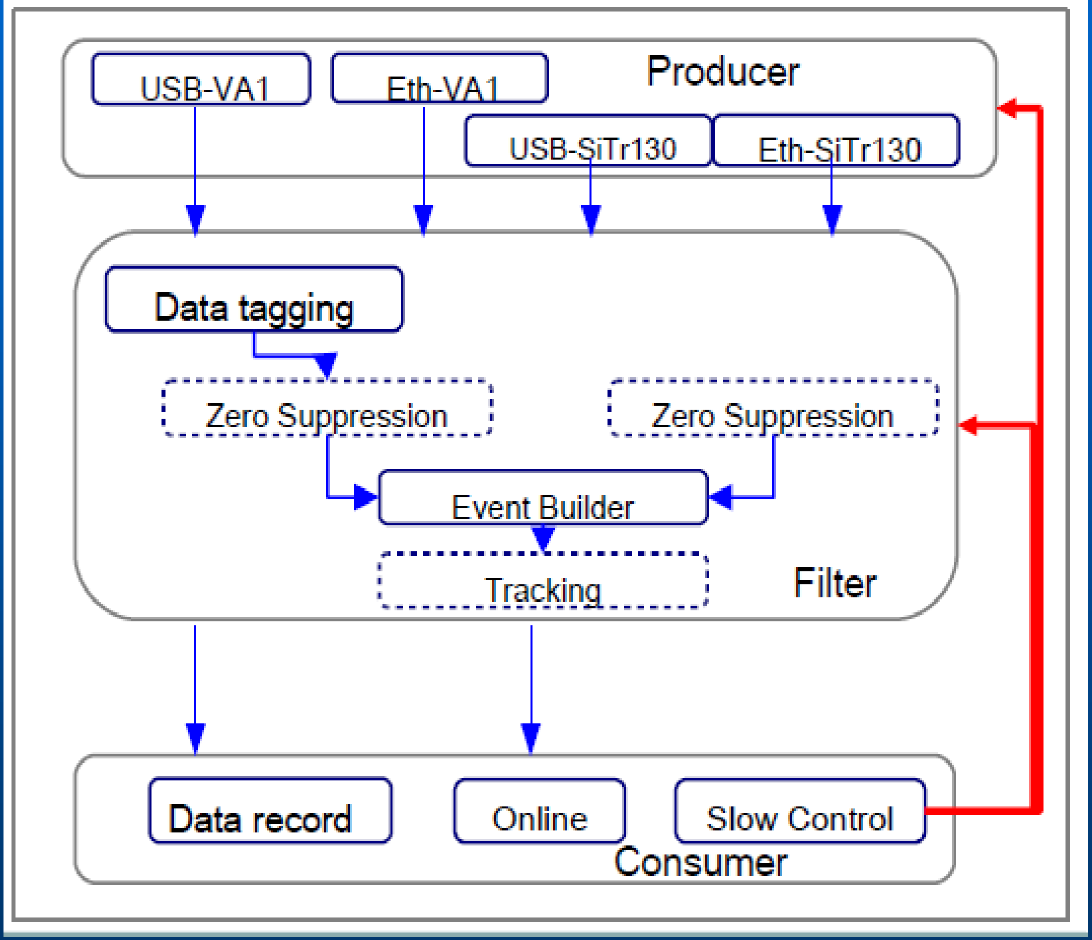


VA1' ASIC used as reference devices



LPNHE
Laboratoire de physique nucléaire et des hautes énergies

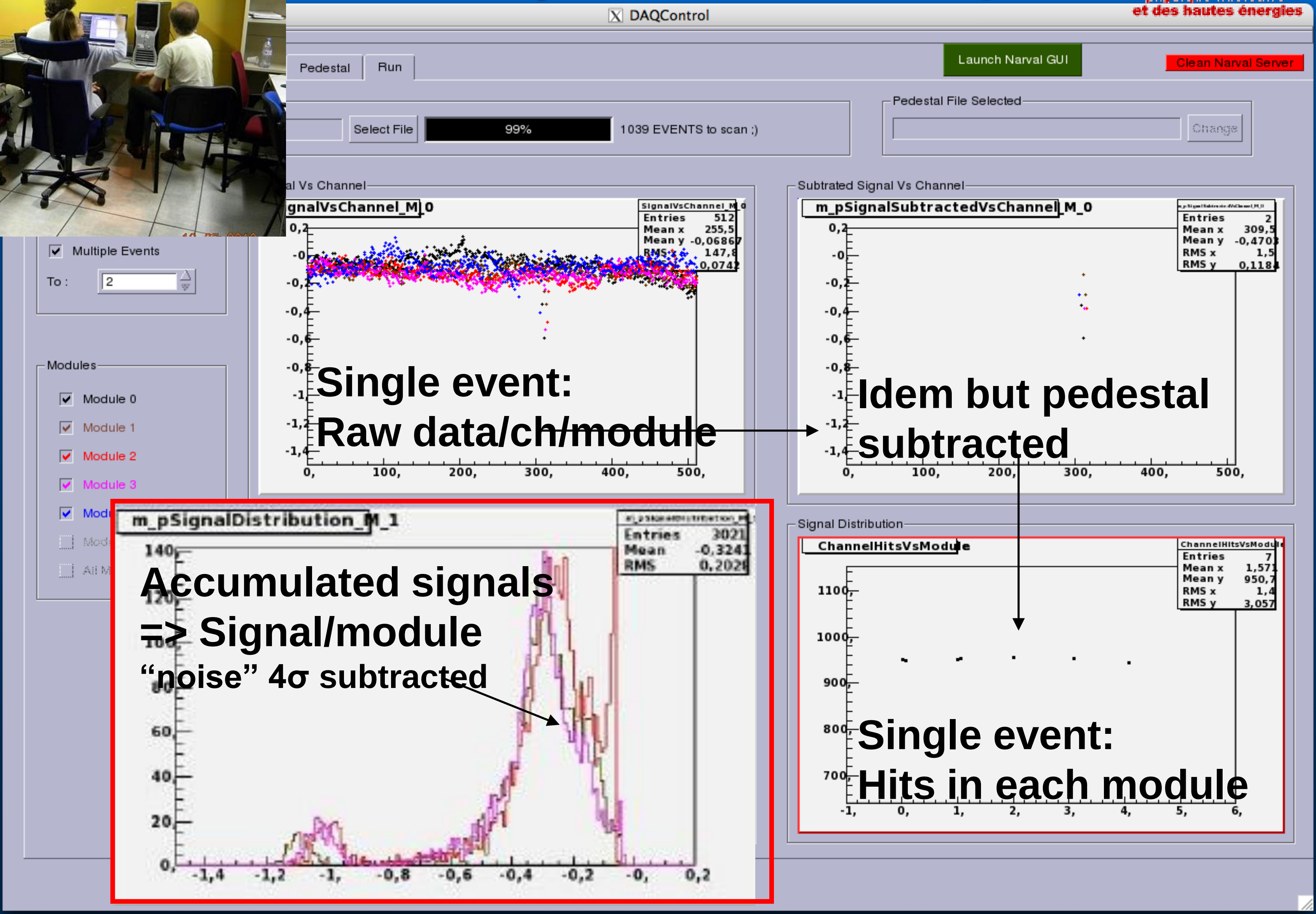
DAQ software



NARVAL:

- Distributed DAQ written in ADA language
- Divide the acquisition into activities called actors (ADA)
- 3 basic actors:
  - Producers
  - Filters
  - Consumers
- Dedicated Libraries in C/C++/ADA
- High Flexibility with very simple scripts & xml files

SPS May 2010 T.B.:Online plots



Testbeam Analysis

CU Prague

- **In a testbeam, we study prototype modules (reliability, S/N, charge sharing, resolutions etc.). Therefore,**
  - Geometry of testbeam setups is intentionally made simple
  - Tracking is used for alignment and calculation of resolutions. Simple tracking is used to obtain simple statistics of residuals for resolution estimates
- **So testbeam analysis is different from analysis in big experiments, BUT**
  - Studies of resolutions and detector response statistics can help to correctly define the parameters of tracking engines.
  - Studies of cluster parameters and charge sharing can contribute to better hit reconstruction

Analysis workflow

- “BLACK” correction: Pedestal and common noise subtraction
- Hit reconstruction 1: Centre-of-gravity
  - „WHITE“ correction 1: gain equalization
  - Rough alignment of detectors and tracking
  - Hit reconstruction 2: Eta correction
  - “WHITE” correction 2: Large scale response correction to eliminate edge effects
  - Final alignment, calculation of resolutions

Error Analysis

- Bootstrap resampling error analysis of alignment and tracking parameters and resolutions

Simulations

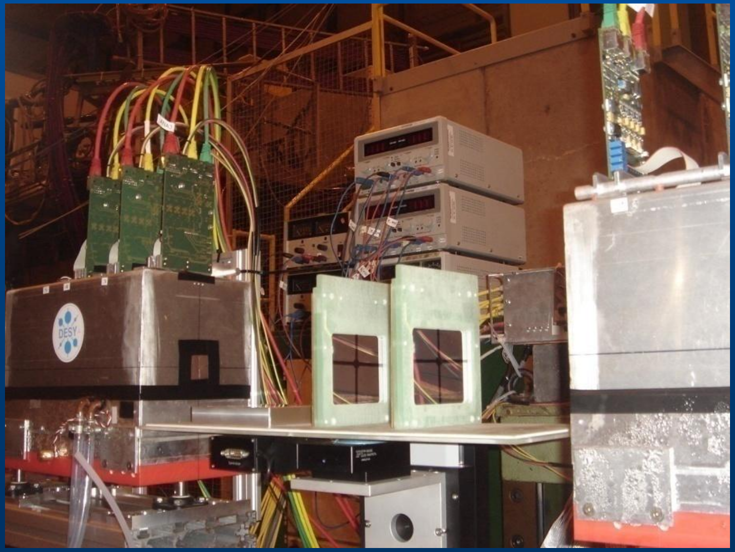
- GEANT 4 simulations of particle tracks
- Verification of analysis results and error analysis on simulated tracks
- Verification of specific simulations for individual analysis steps, such as gain equalization

The Prague Tracking Package

- **Hit alignment** (aka pattern recognition) – Scott and Longuet-Higgins iterative scheme
- **Detector alignmen**t based on Karimaki – looking for best alignment updates of residuals in local coordinates.
- **White correction algorithms** – gain equalization and large-scale response equalization
- **Tracking**: Straight line fits for alignment and resolutions
- **Detector resolutions**– estimates all resolutions based on covariance matrix of fit residuals
- **Bootstrap error analysis**
- **Validation by Geant 4 – based MC**

ALIGNMENT: Initial Proposal

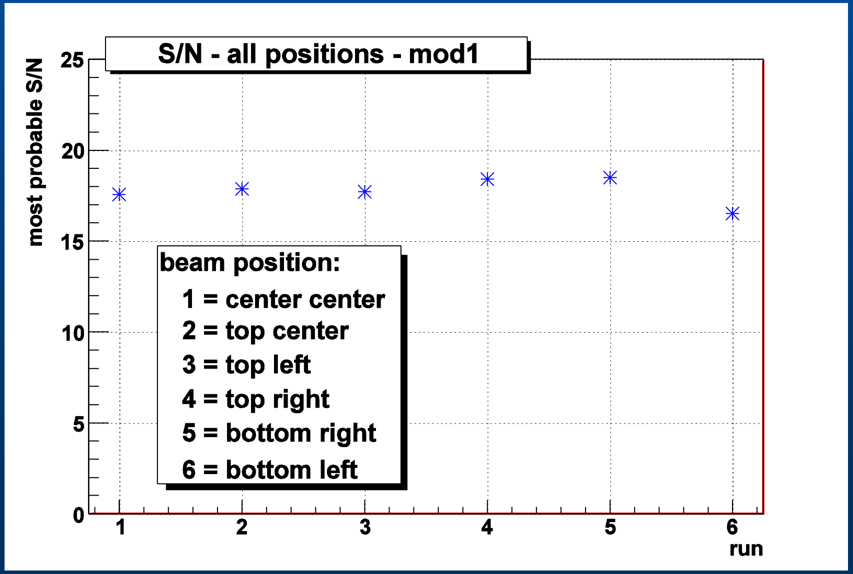
- Contribute to the SiTRA infrastructure by providing a laser-based alignment system.
- In brief: Usage of collimated laser beams (IR spectrum) going through silicon detector modules. The laser beams would be detected directly in the Si-modules. (AMS-I Idea)
  - CMS-Like sensors with optical windows as "baseline deliverable"



Part of the EUDET FP6 tracking prototype AIM:

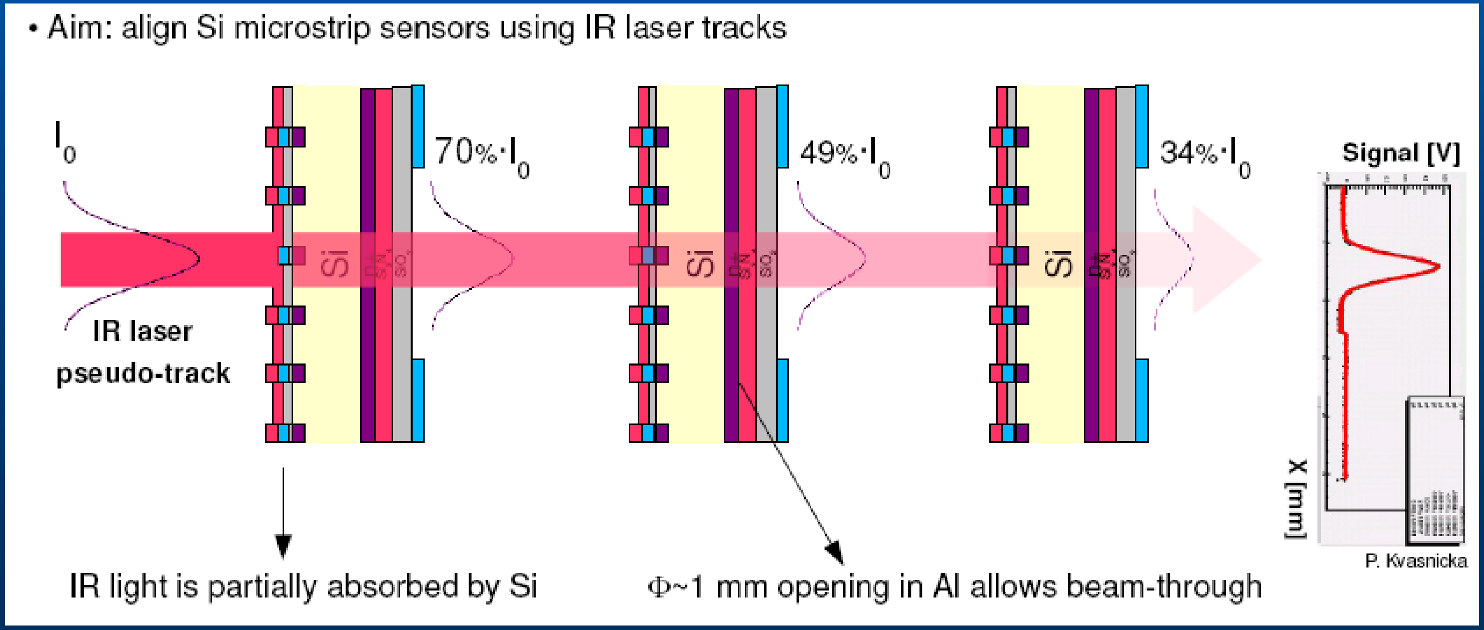
Assessment of SNR for backside removed metallization.

Comparison between track-based and laser alignment.



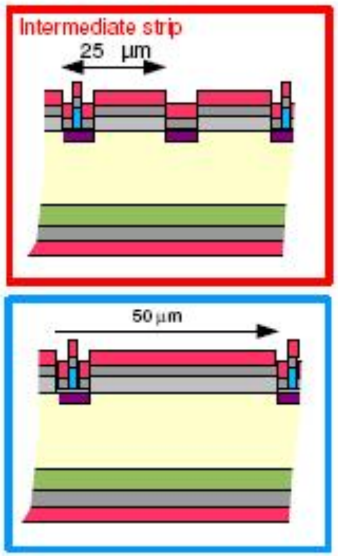
Beyond the EUDET baseline

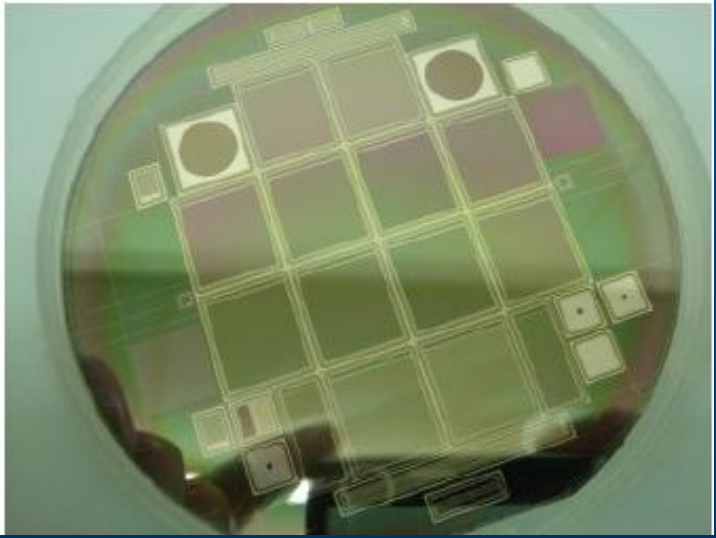
- **Transparent sensors for Si-tracker position monitoring.**
- **R&D line – Improve the photodetection characteristic of "conventional" microstrips sensors.**
- **Two handles:**
  - Replacing non-transparent Al electrodes by a Transparent Conductive Oxide (ITO, AZO, Poly,…)
  - Adjusting the layer thickness to reduce reflectance, including the AR coating in the default sensor design.



Beyond the EUDET baseline (2)

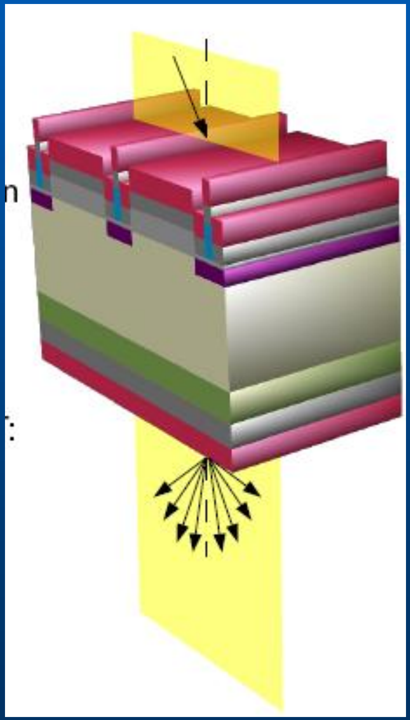
- 5+1 wafers
- 12 µstrip detectors per wafer (6 with intermediate strips, without metal contacts)
- 50 µm RO pitch (25 µm interm. strip)
- 256 RO strips
- 1.5 cm length varying strip width (3,5,10,15 µm)





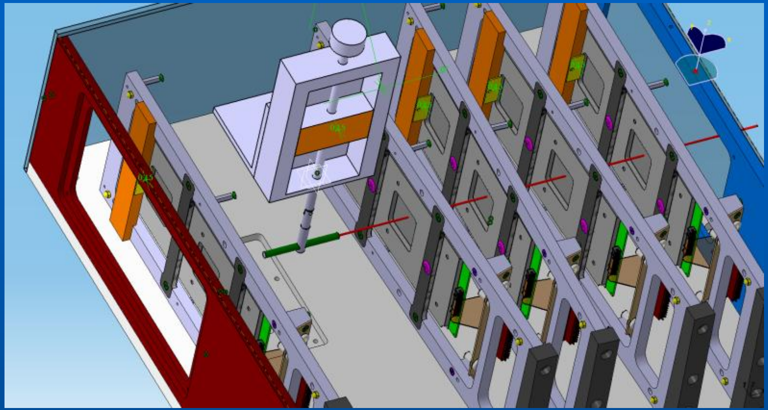
After last passivation layer
Tmax about 60% (7 layers)

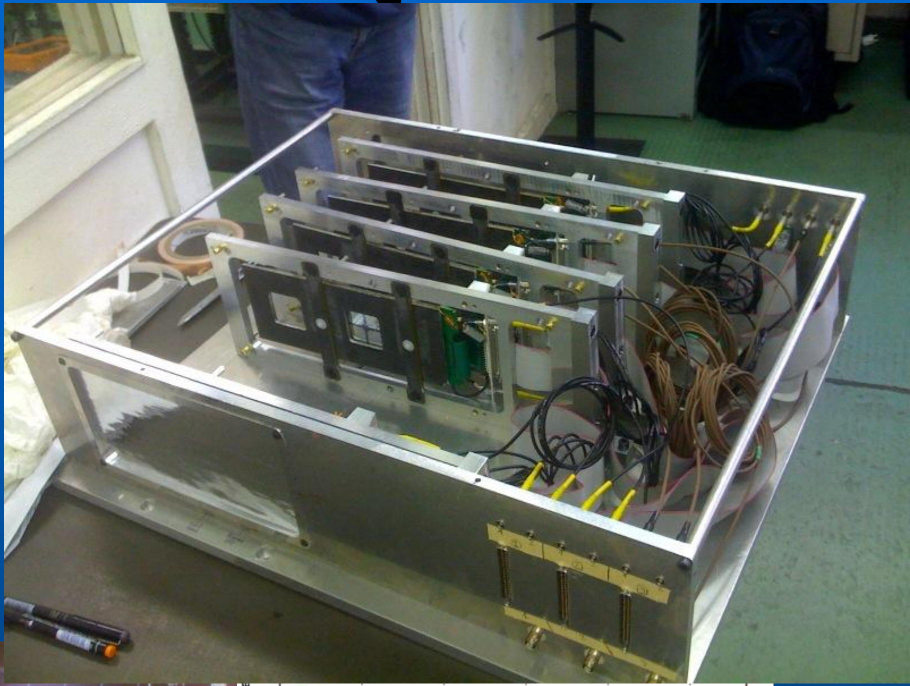
Compare with 20% @ CMS



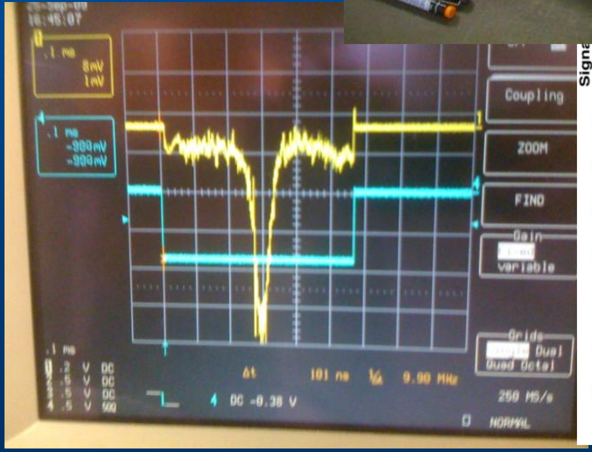
Banc de test autonome et portable a multiples applications + DAQ associe

Ex: test d'un systeme d'alignement:

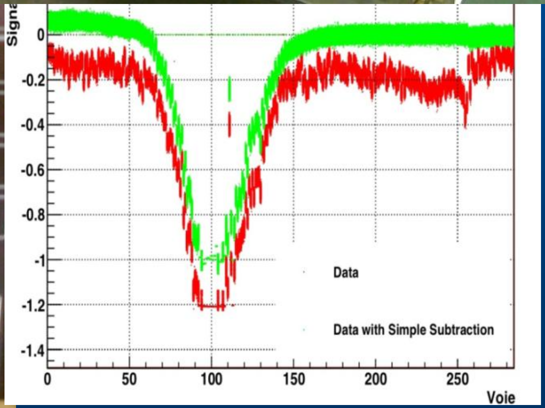




Tests of alignment system based on AF HPK sensors



Alignement test with IR laser



Signal reconstruit

Motorized 3D Table (Torino)

- suitable for testing Silicon sensors, pixel and microstrips in a beam test,
- DUT can be moved and rotated with respect to the beam line.
- built in a modular way, so that it can arrange different types of DUT, with alignment telescopes or without.
- 5 motors are controlled remotely via RS232, to set positions and angles, via LabVieW application
- Eudet-Memo-2007-59

Torino U. And INFN

DUT support D,
move horizontally
across beam line and
rotate

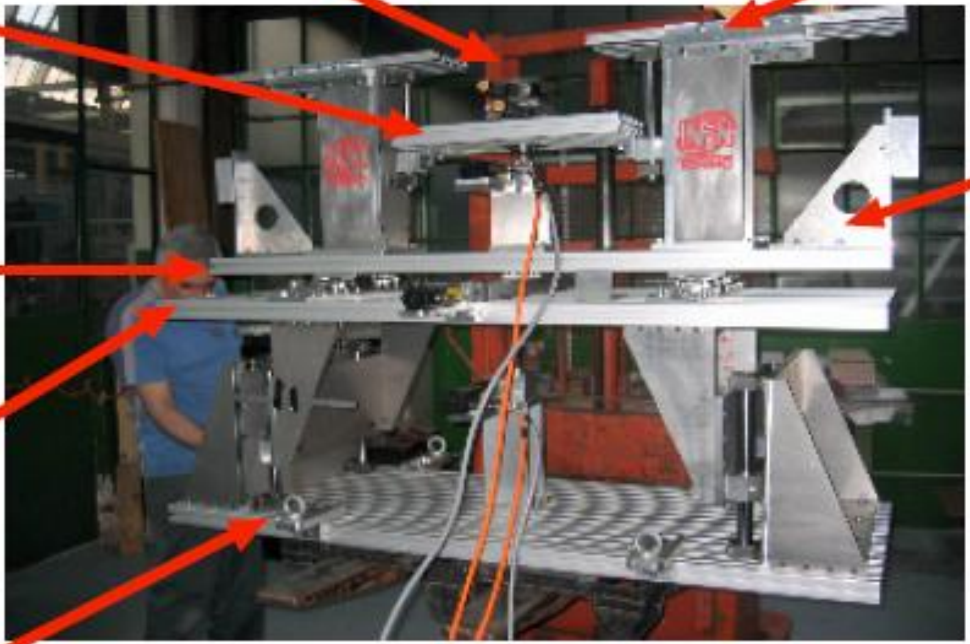
Telescope support

Base C for DUT

Beam scintillator
support

Base B with DUT
and telescope move
horizontally
across beam line

Base A
move
vertically



Ground fixed Base G

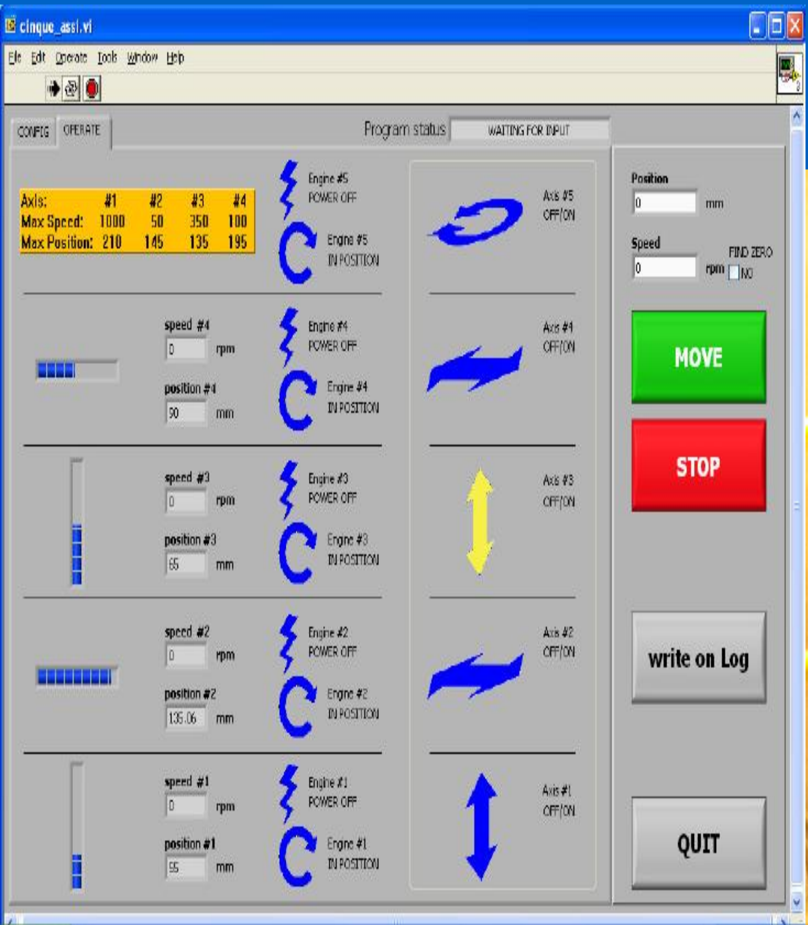
Movements:
Base A DZ=28 cm
Base B DY=20cm
Base C DZ=16cm
Support D, DY=5cm,Dphi=+-90^{O}

CERN PS: 2008

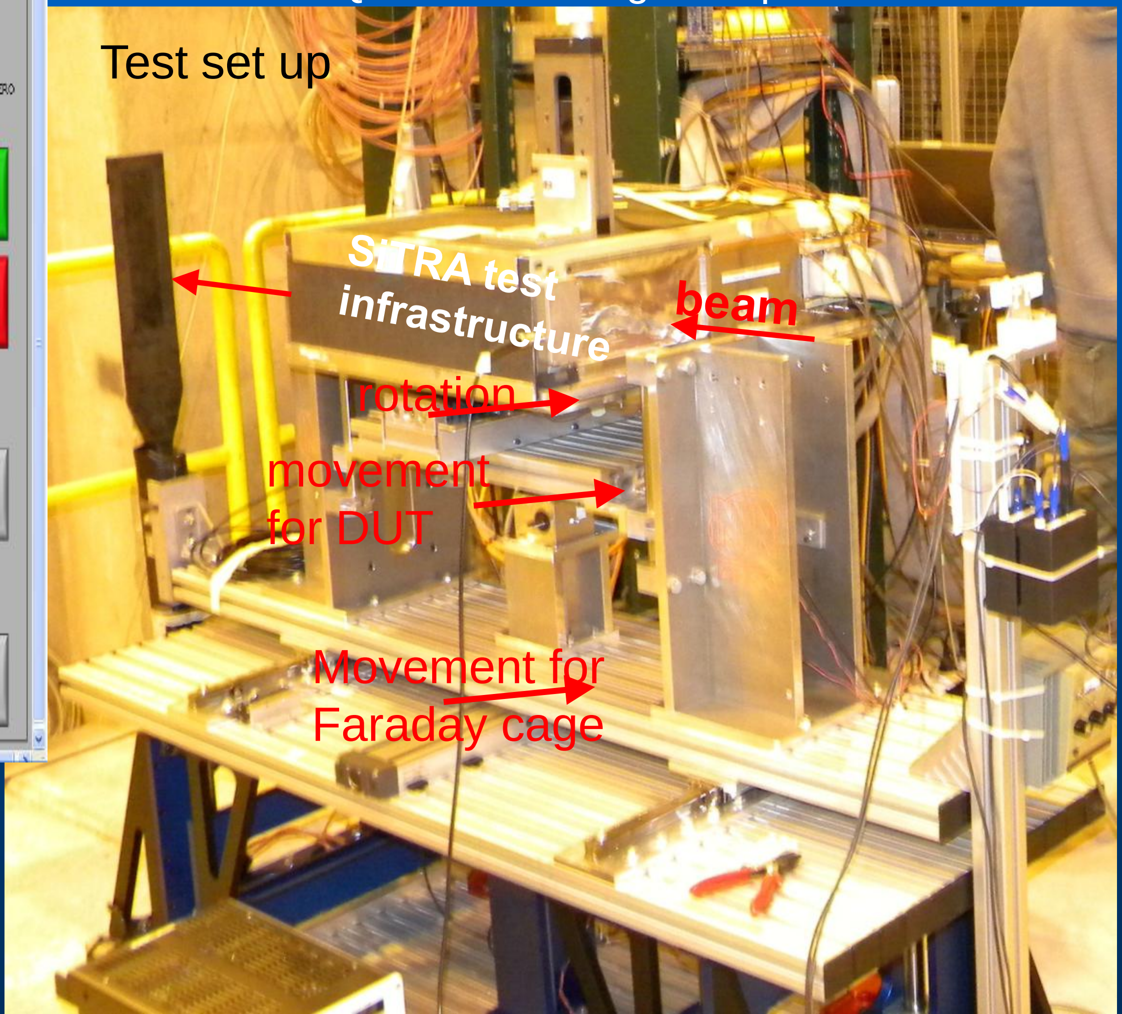
Torino U. and INFN

BEYOND EUDET: NEW 3D Table *(Torino)*

- 5 motorized & controlled movements:4 linear+1 rotation 2 movements for positioning test bench; 3 for a 3D scan of the DUT
- Main feature: highly precise position repeatability: with Linear mvt □ 0.1mm and rot □ 0.01 degree (tested by TB)
- Control & monitor via serial line by LabView and through Ethernet to DAQ thus recording DUT positions/each run.



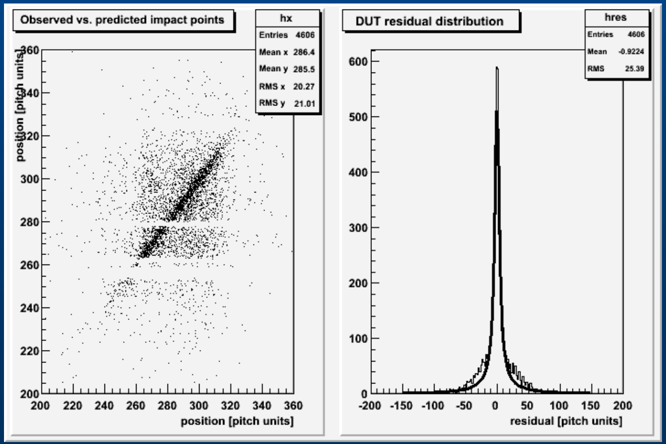
LabView based GUI allowing adjustement of 5 available movements



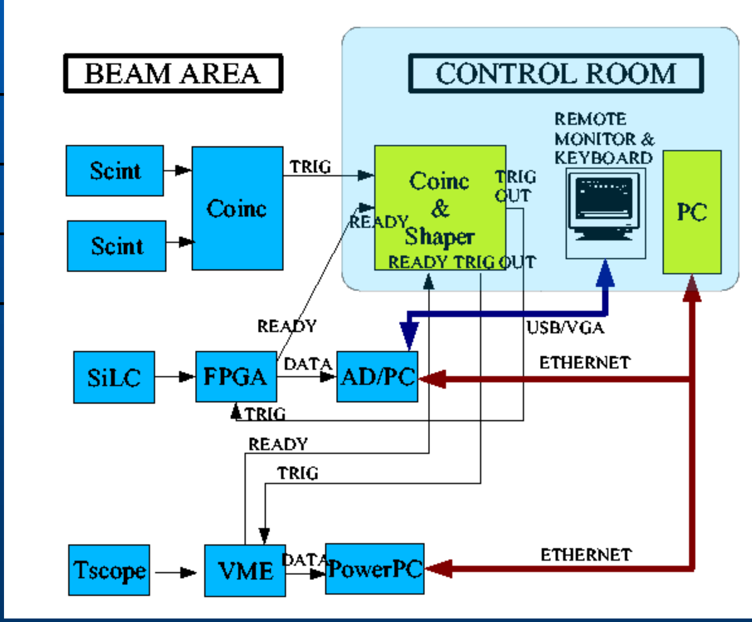
Test Beams since October 2006

During October and November 2006, the first SiLC test beam took place at DESY.
3 prototype modules were tested in a beam of 1-6 GeV electrons. DESY TB telescope

Notation	sensor	pitch [µm]	total length [mm]	FE electronics
A	GLAST	228	900	228 nm + VA1
B	CMS	183	283.5	180 nm + VA1
C	CMS	183	283.5	VA1 (reference)

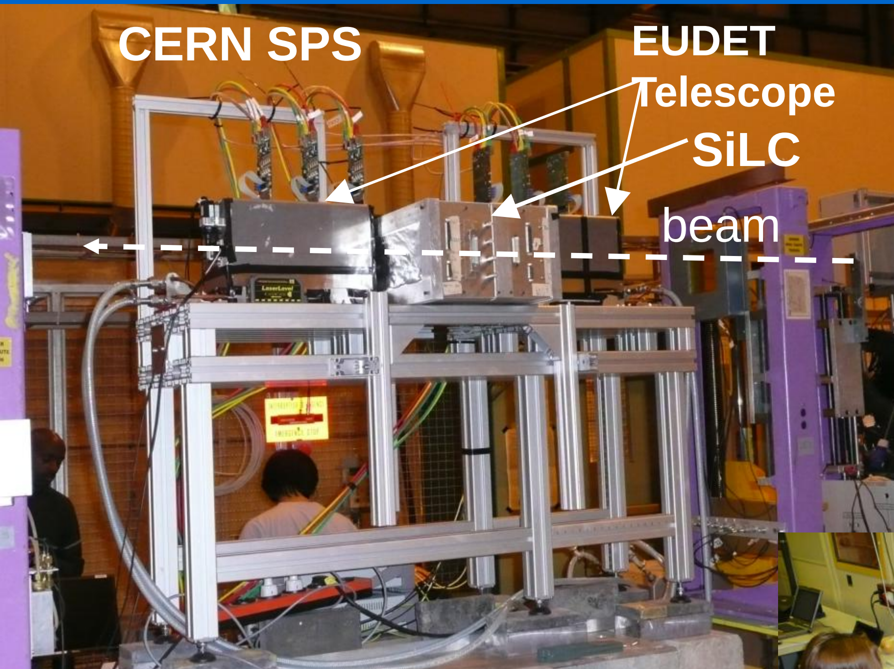


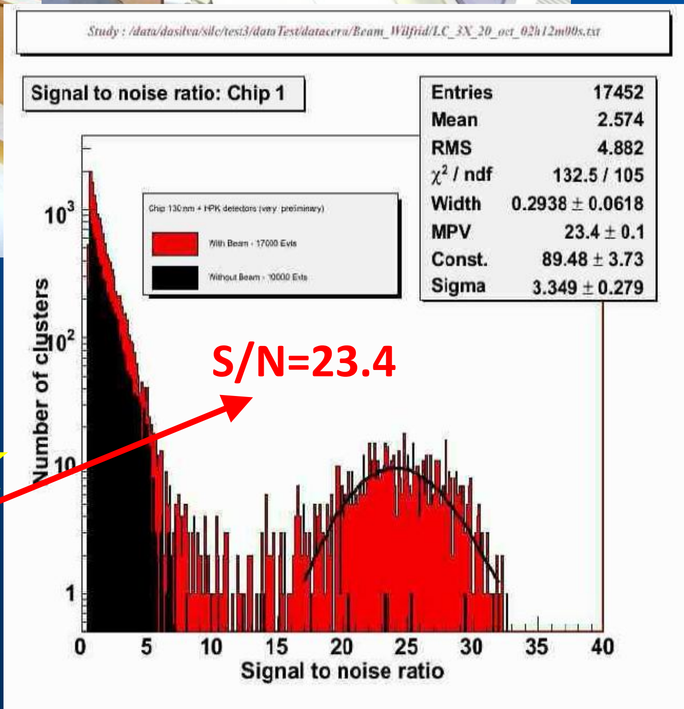
GOAL:
Test of SiTR_180
+ various Si protos
S/N=15



Test Beam DESY, oct.2006

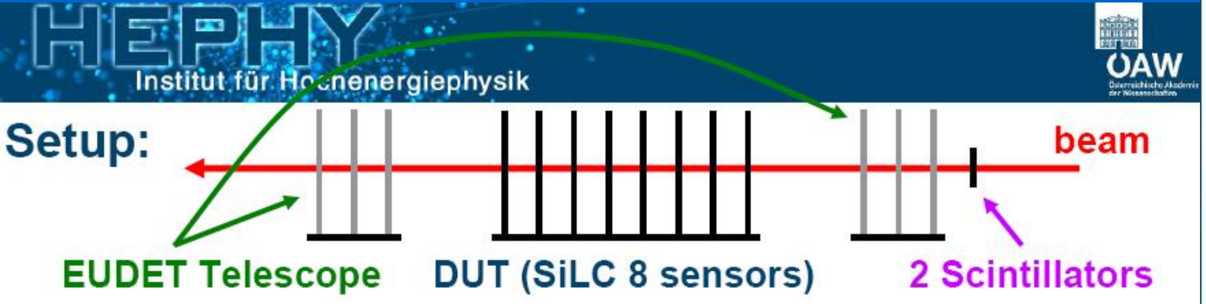
First Combined TB of 1st SiTRA infrastructure with EUDET telescope, Nov 2007

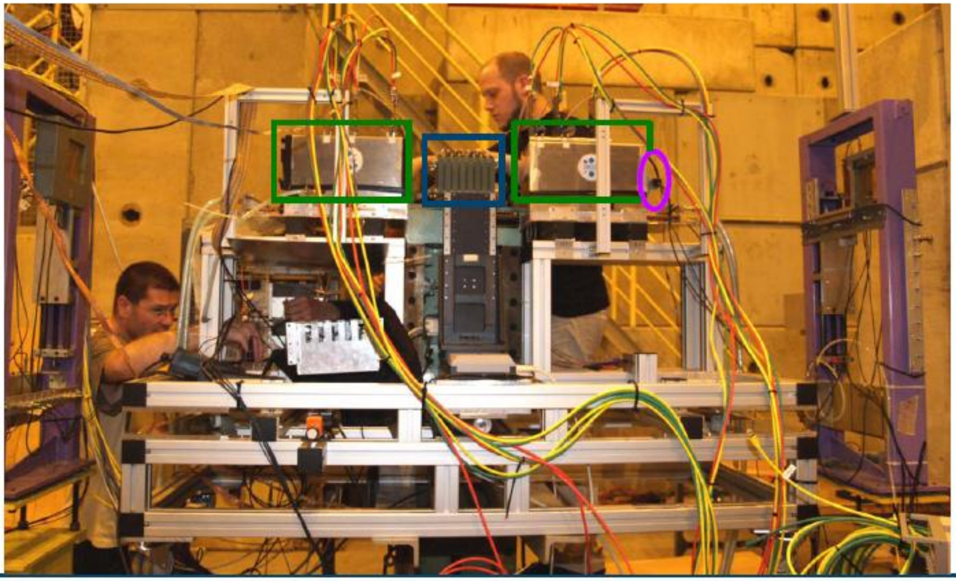


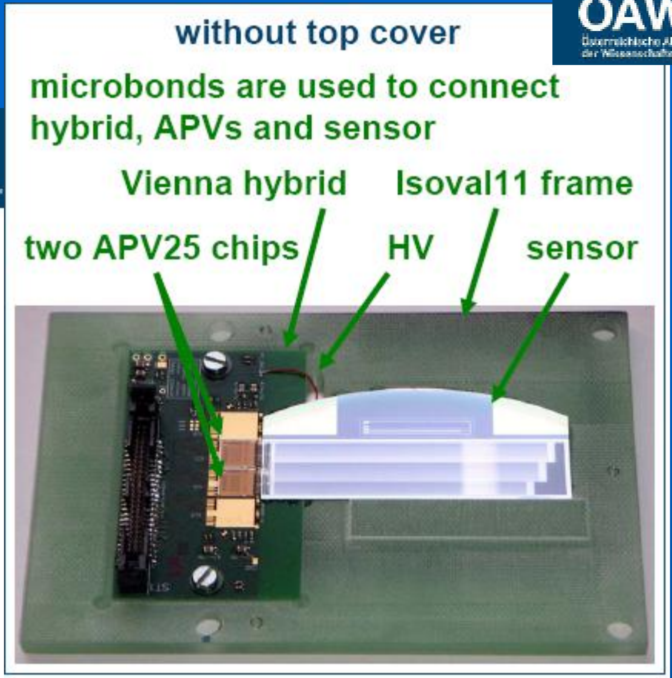


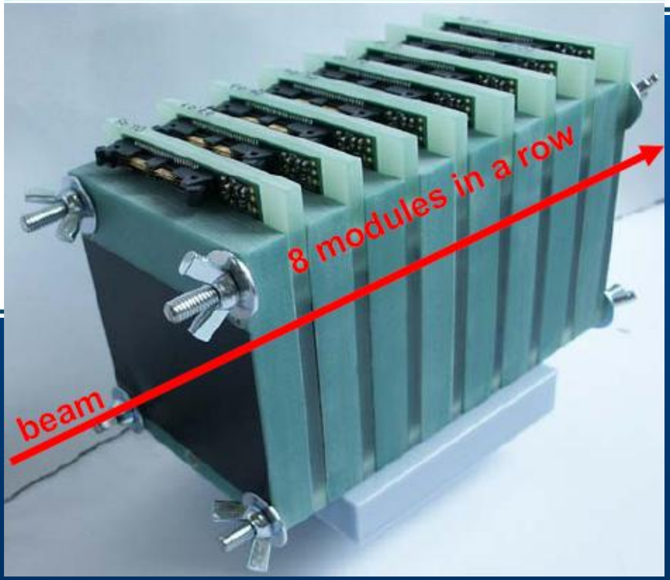
Goal: test the Prototype equipped with new HPK strip sensors and the new SiTR_130 FE chip

Test beam on HPK test strutures





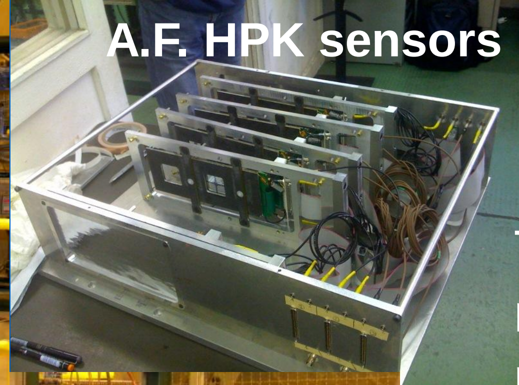


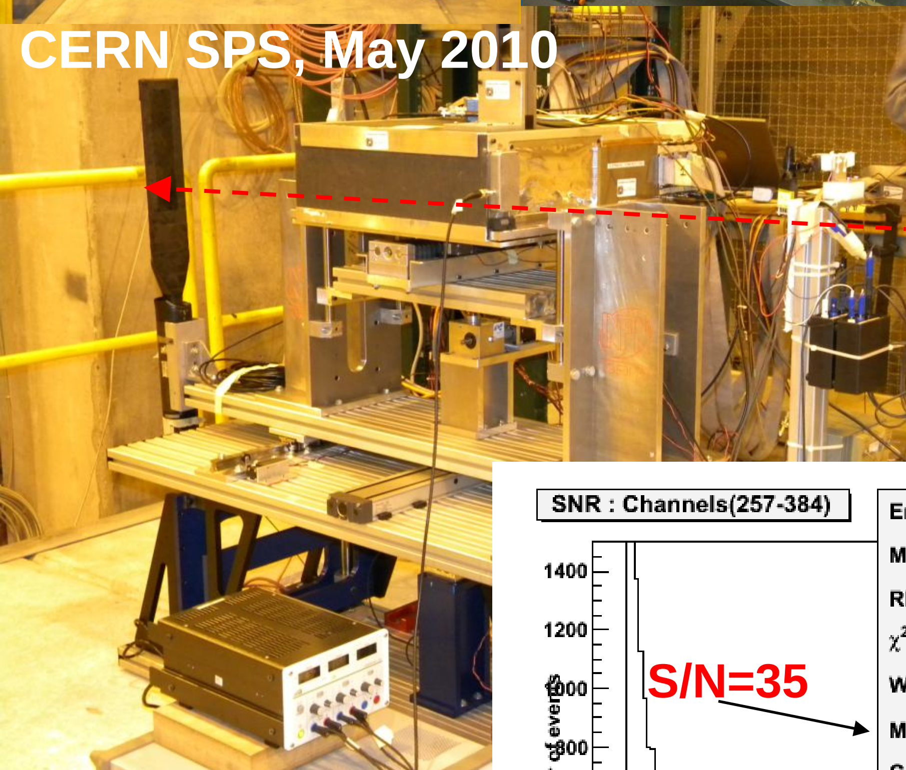


Performed on H6B SPS-CERN in August 2008.

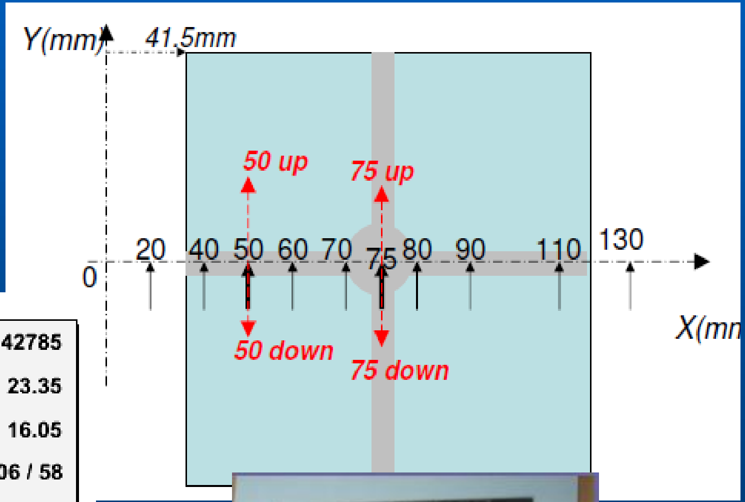
Goal: Characterization of the test structures in the HPK sensors

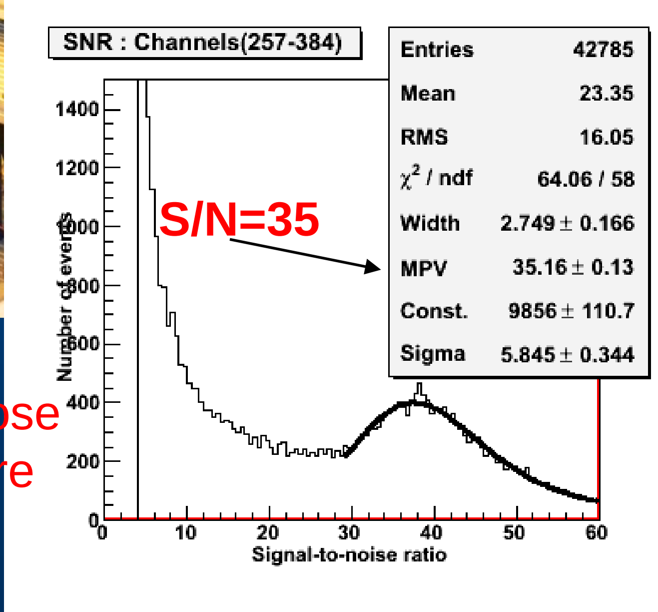
Standalone T.B. infrastructure





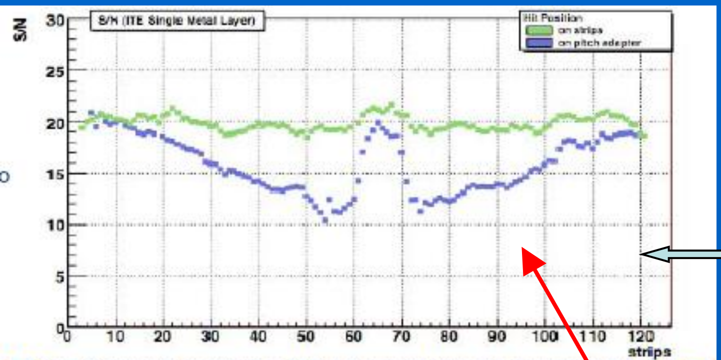
TB system for testing any new Si module with strips or pixels & any new FEE and/or DAQ Electronics. First & successful test in May 2010 at SPS-CERN (alignment sensors).





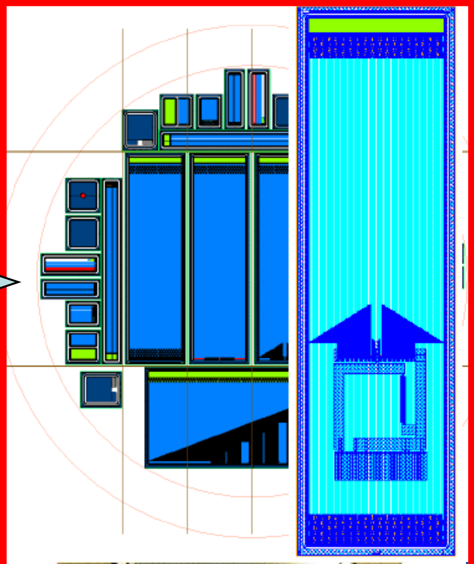
First TB with the new Standalone multipurpose TB SiTRA infrastructure

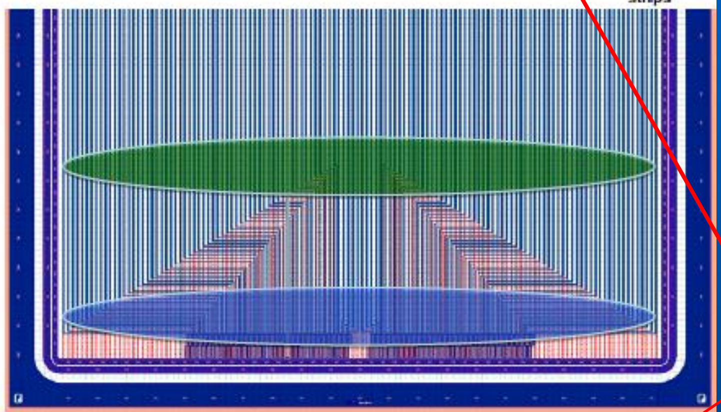
ONGOING NOW in 2010

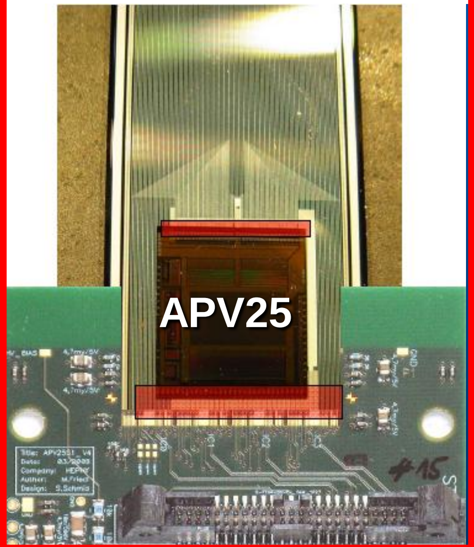


Test beam at SPS-beam 2009 → 2010

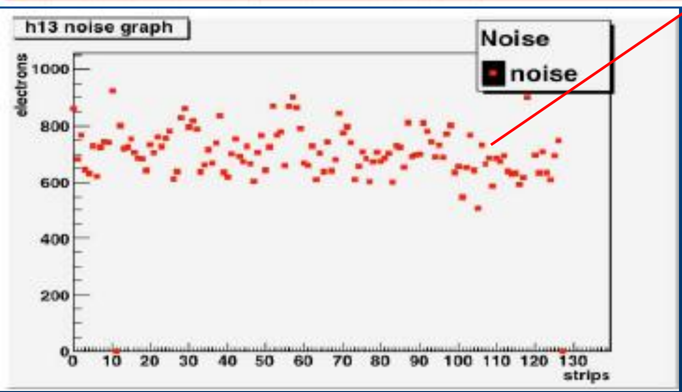
Combined with EUDET Telescope







Not due to noise increase but to signal loss



Results from 2009 test beam

Reason:

- capacitance of integrated coupling capacitor gets extremely low when metal strip moves away from implant in routing region
- Remedy: routing on dedicated, second, metal

Chip glued on sensor: wire or bump bonding

And test new DSSD-HPK

TA #2 in 2010 currently running At CERN SPS (th bergauer)

Activities in 2010: transnational activities

- ***Transnational Activity #1: Test beam at CERN led by D. Gamba (Torino)***

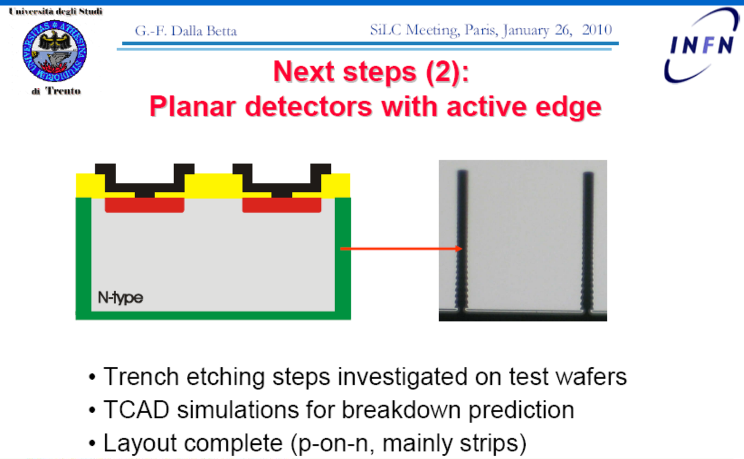
An upgraded version of the SiTRA test infrastructure was used by the Torino team to calibrate their new 3D motorized and fully automatized 3D Table with very high precision movements.
This Table after EUDET is a new general facility that will be used by Torino's teams.
(Torino is an important sezione of INFN and contributes to LHC-CMS and ALICE-, as well as a number of other experiments in particle, nuclear and astroparticle physics, with important participation to detector R&D and construction.)
At the same time it allowed testing the performances of new HPK microstrip sensors especially treated for the alignment.
(more on the early slide on the new 3D automatized Table)

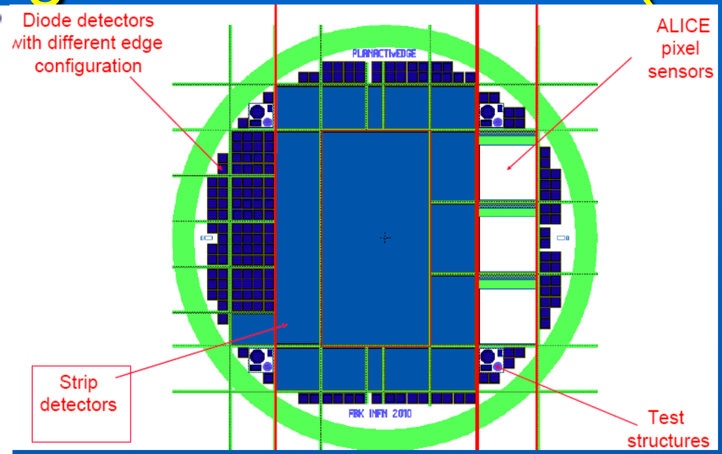
Participants to this test beam:
D. Gamba, G. Alampi, G. Cotto, P Mereu (Torino INFN and University)
A. Charpy, J. David, M. Dhellot, P. Ghislain, F. Kapusta,A. Savoy-Navarro (LPNHE)
M. Fernandez-Garcia (IFCA)
Contribution from Z. Dolezal for the Telescope PMs.

Test beam at SPS CERN: May 10-17 with proton beam of 120 GeV.

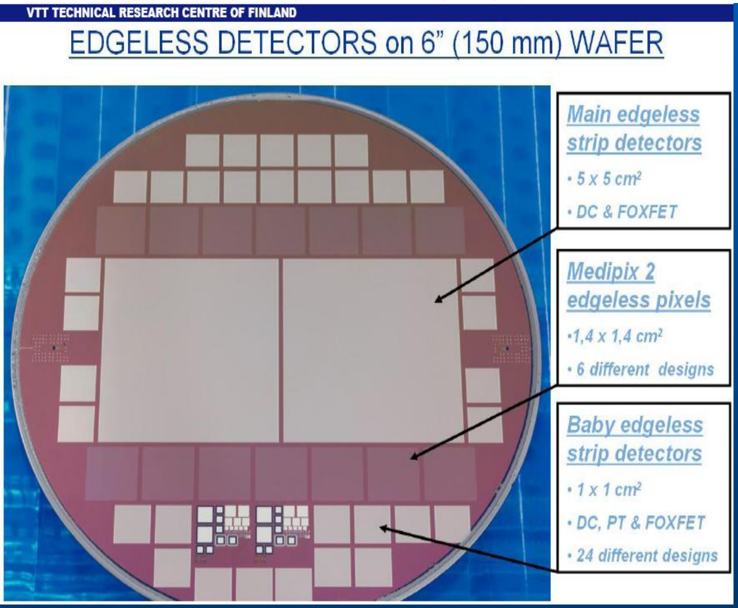
EUDET-memo in preparation

TN#3: Test of new edgeless Si sensors (IRST+VTT)

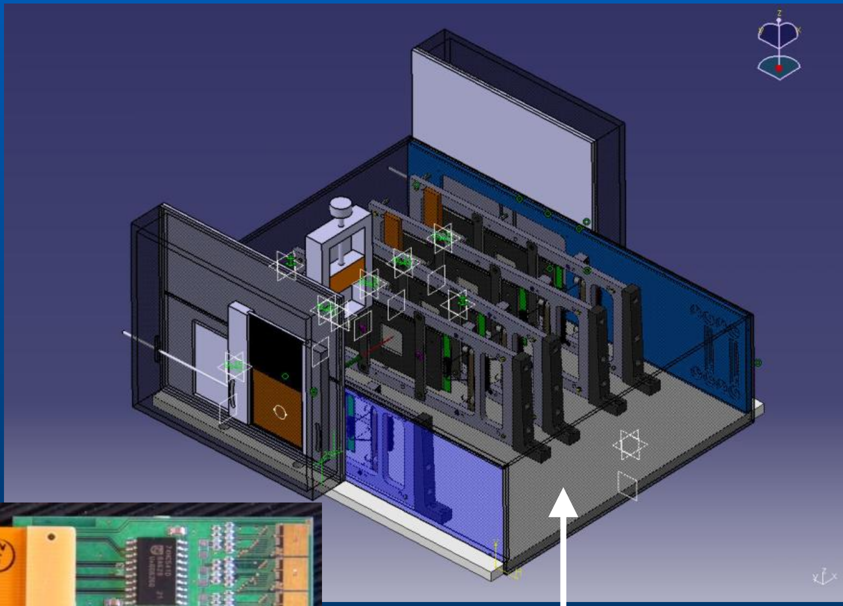




Nov TB at CERN Using standalone EUDET Infrastructure to Test new Si strip technologies

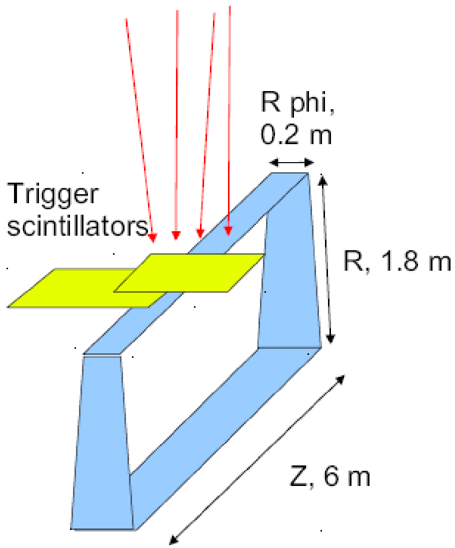


And eventually even more



Some updates on the infrastructure are prepared

TA-EUDET: Cosmic test with ATLAS tile starting 2010



Interest:

- Measure z coordinate of the impact point and phi
- Precision:
  - z: < 1 mm
  - Phi: < 2 mrad
- Area:
  - ~100 mm z
  - ~200 mm R x phi
- Rate: 0.01 /cm^2 /s

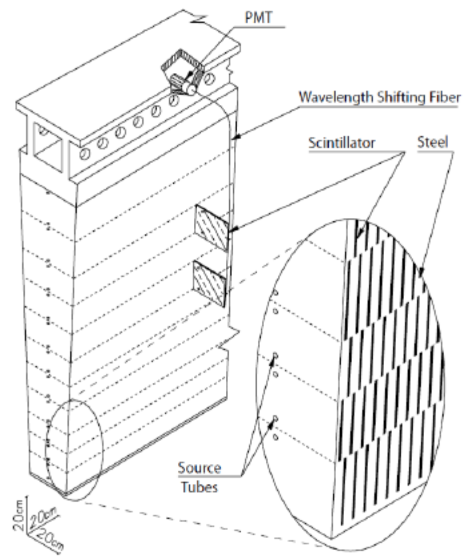
Proposal for the usage of EUDET TA2/SI_STRIP infrastructure at CERN in November 2010

ATLAS Tilecal collaboration (part)

Institute of Physics, Academy of Sciences, Prague, Charles University in Prague, Institut de Fisica de L,Universitat de Valencia-CSIC, CERN

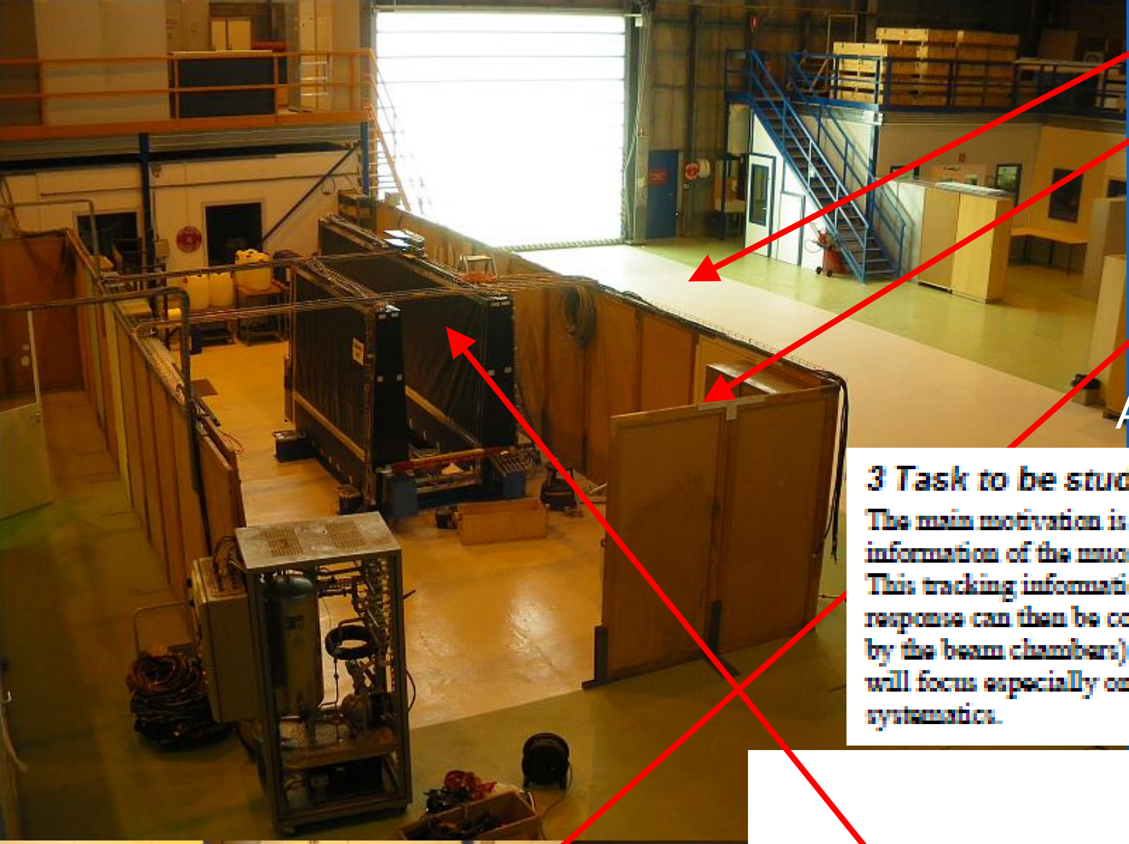
Team leader: Stanislav Nemecek, Institute of Physics, Academy of Sciences, Prague

- ATLAS Hadronic Calorimeter Tilecal
- Sandwich of iron and scintillator
- Segmentation period
  - Iron: 5+4+5 mm
  - Scintillator 3 mm



Silicon test infrastructure

- ➢ 2 Silicon modules
- ➢ Modules currently used as XY-Telescope
- ➢ RO pitch: 100 µm
- ➢ FEE & DAQ of test infrastructure Easy to associat to the ATLAS Tile cosmic ray test set-up
- ➢ DAQ synchronized with common trigger busy signals (at rate ~ 1 Hz/wafer)

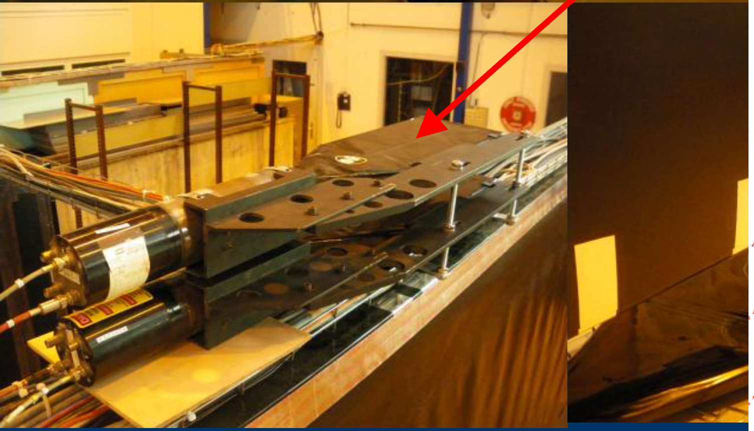


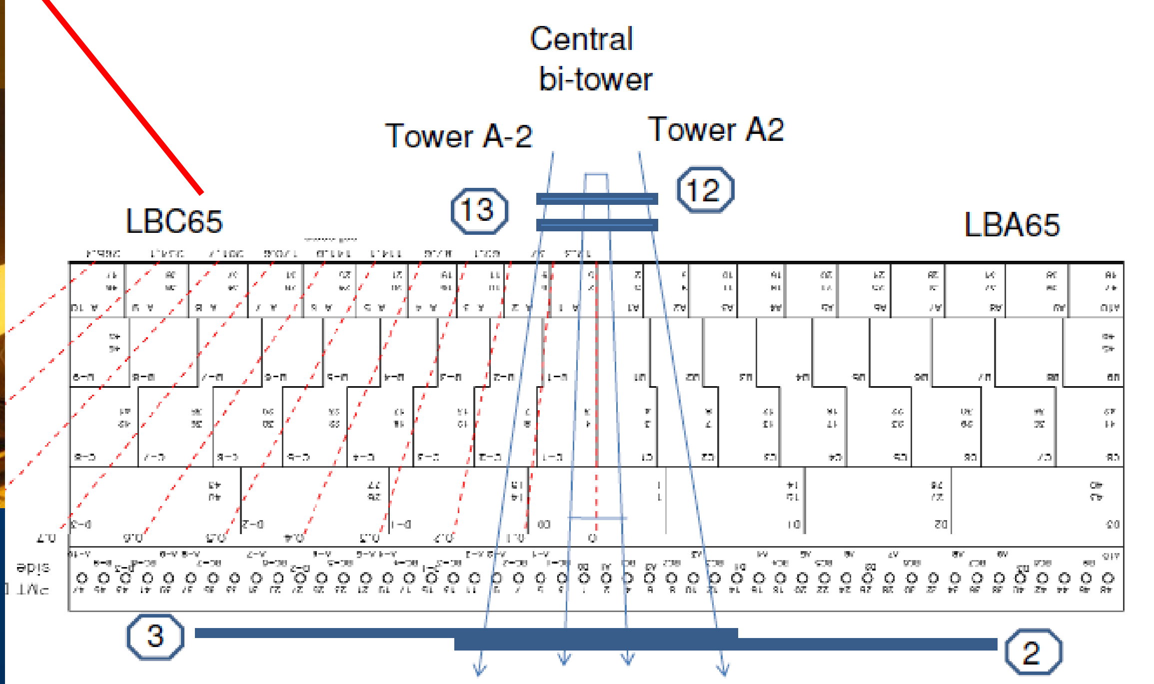
- Floors painted
- Cesium zone enlargement is in progress
- Cosmic ray trigger
  - Installed top/bottom scintillator pairs for long barrel module

ATLAS-TILE test set-up at CERN

3 Task to be studied

The main motivation is to study the cosmic muon response using rather precise information of the muon track passing through the calorimeter.
This tracking information is expected to be delivered by the Si-strip detector. The response can then be compared to the testbeam results (where tracking info was provided by the beam chambers) and to that of cosmic muons in the full ATLAS setup. Studies will focus especially on the intercalibration of the Tilecal radial layers and associated systematics.





This test set-up be pursued these next coming years

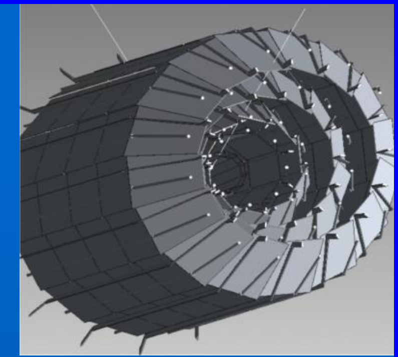
Outcomes and perspectives

Beside the obvious **synergy with the *upgrades of the large area Si tracker at LHC (ATLAS & CMS)*** already underway at the start of this E.U. programme, EUDET developed a strong collaborative effort on T.B. with important outcomes and perspectives:

- Opening to CLIC (FEE, time stamping, sensors etc…
- ATLAS TileCal
- ***Interest by short term future experiments***
  - BELLE II
  - g-2/EDM JPARC experiment

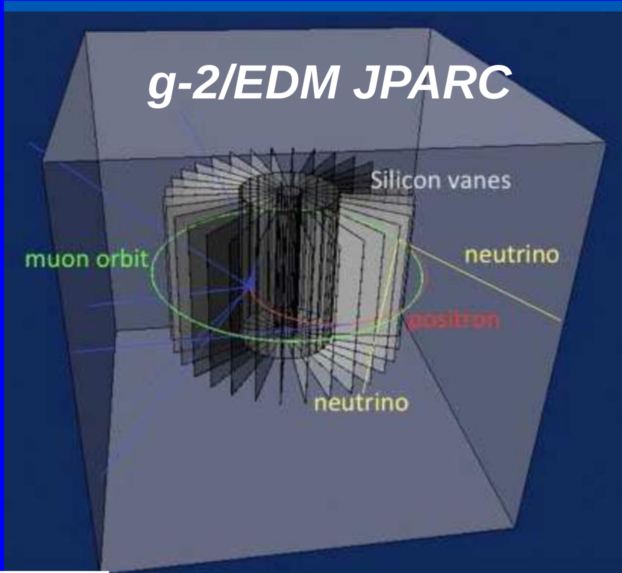
EUDET Programme was a tremendous asset for the SiTRA and the whole SiLC R&D collaboration.
In counterpart, all what was developed within EUDET will be instrumental for near/far future Si tracking applications

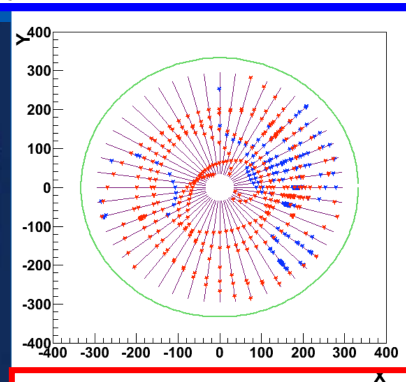
BELLE II	Belle SVD	Belle upgrade SVD
Vertex detector (radius, cm)	4 layer DSSD (2.0<R<10.0)	2 layer DEPFET (1.8<R<2.2) 4 layer DSSD (4<R<14)
Readout / shaping time	VA1TA / 0.8 μsec	APV25 / 0.05 μsec
Silicon area (m^2)	0.6	1.2

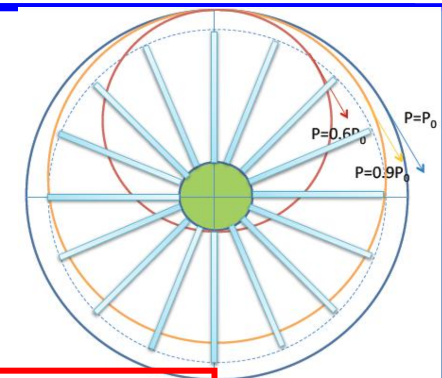


EUDET-memo in preparation

2009/8: HPK starts 6” DSSD production line
2009/9: 6” design submitted to HPK
2010/3: Prototype sensors from pilot batch by KEK
Tested @SPS-CERN







Collaboration:
- ❖Test beam infrastructure
  => tests
- ❖ FEE
- ❖ Alignment system
- ❖ Direct connect FEE/strips

EUDET-memo in preparation

Will be pursued these next years