

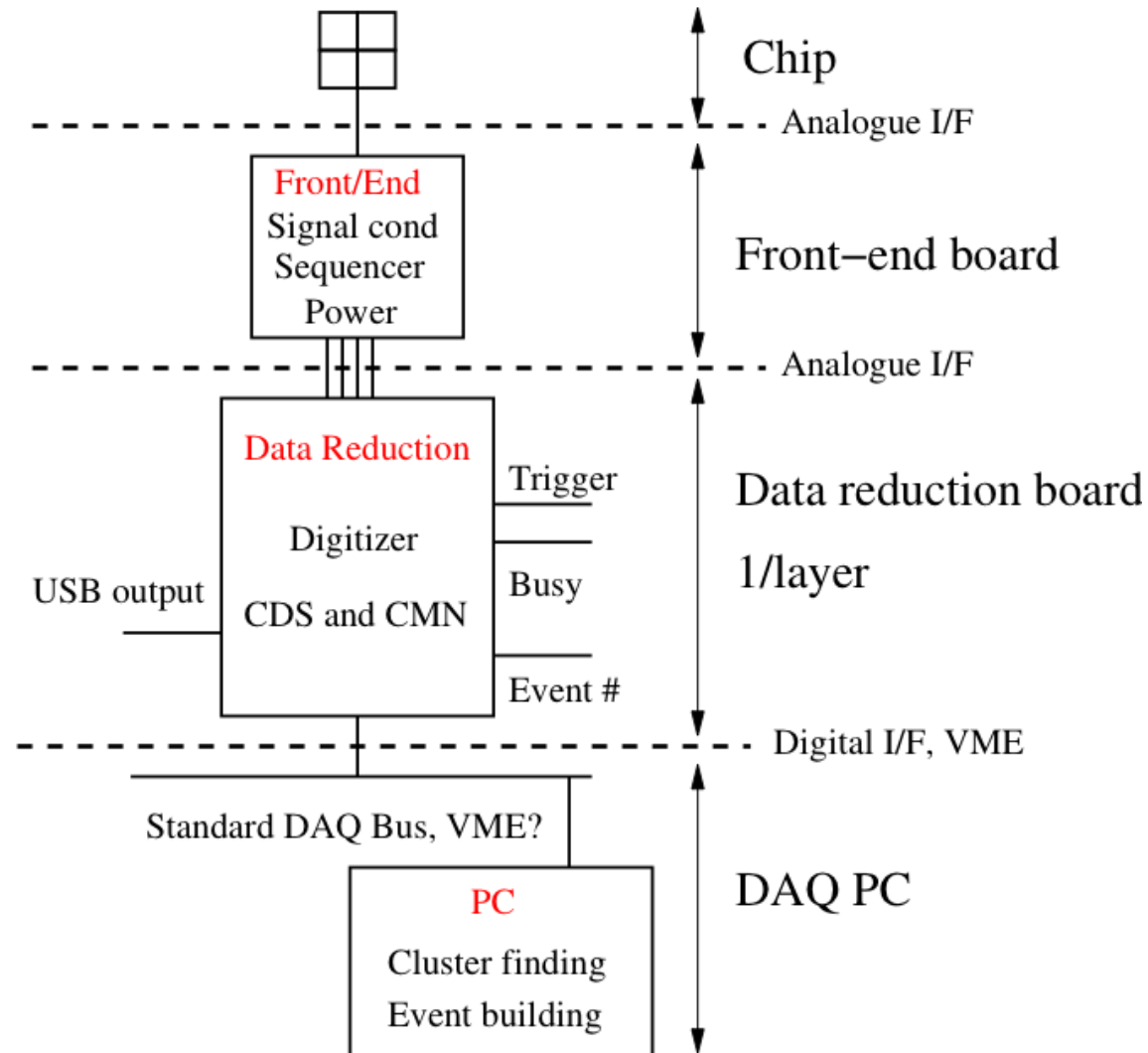
JRA1 Data Acquisition Past – Present - Future

Daniel Haas
Hamburg, Sep 2010

- The initial concept
- Main Ingredients:
 - EUDRB + TLU (Hardware)
 - EUDAQ (Acquisition Software)
 - EUTelescope (Analysis Framework) -> Ingrid
- Past & Present
- Some numbers
- Outlook to AIDA

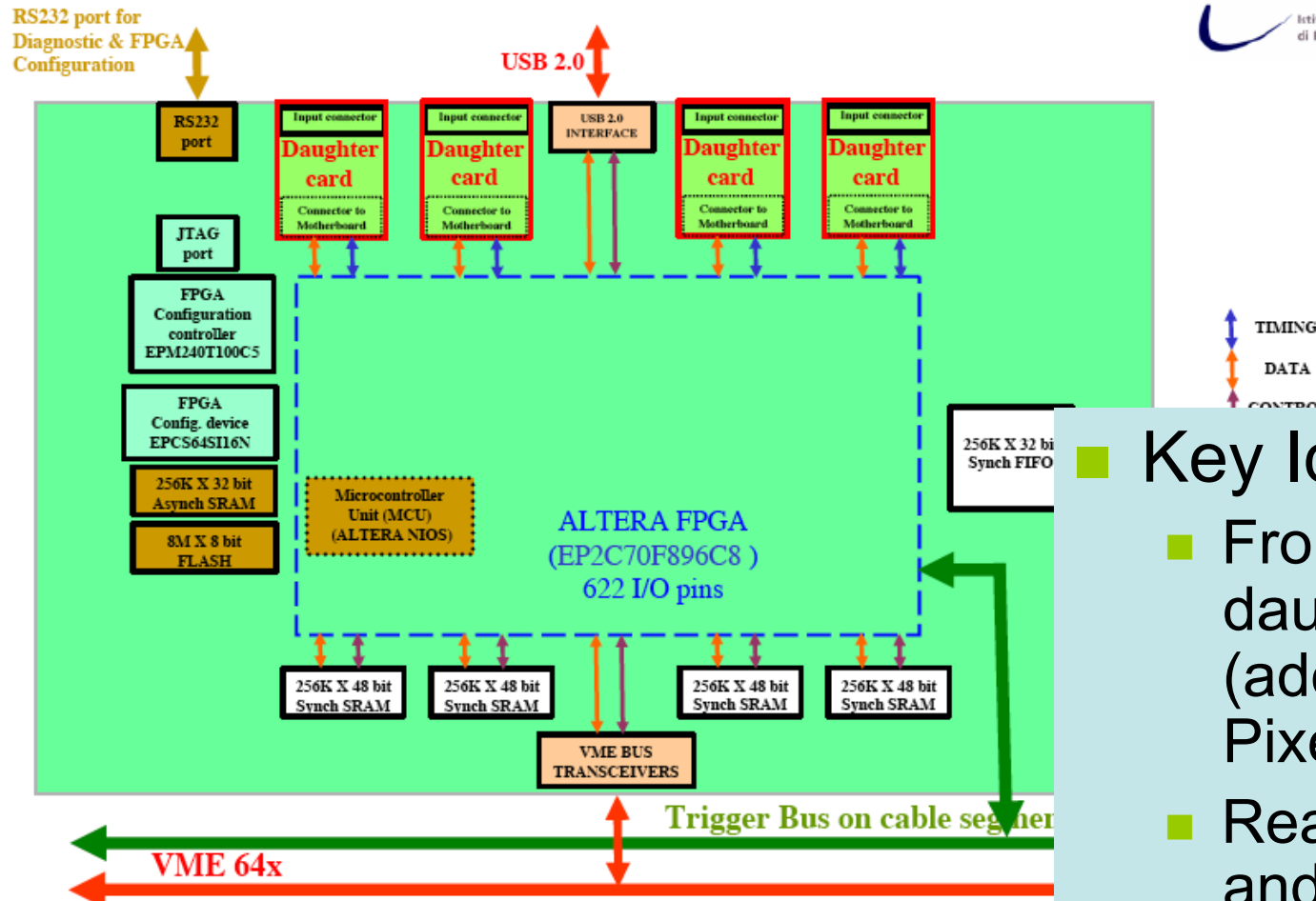


The initial concept...



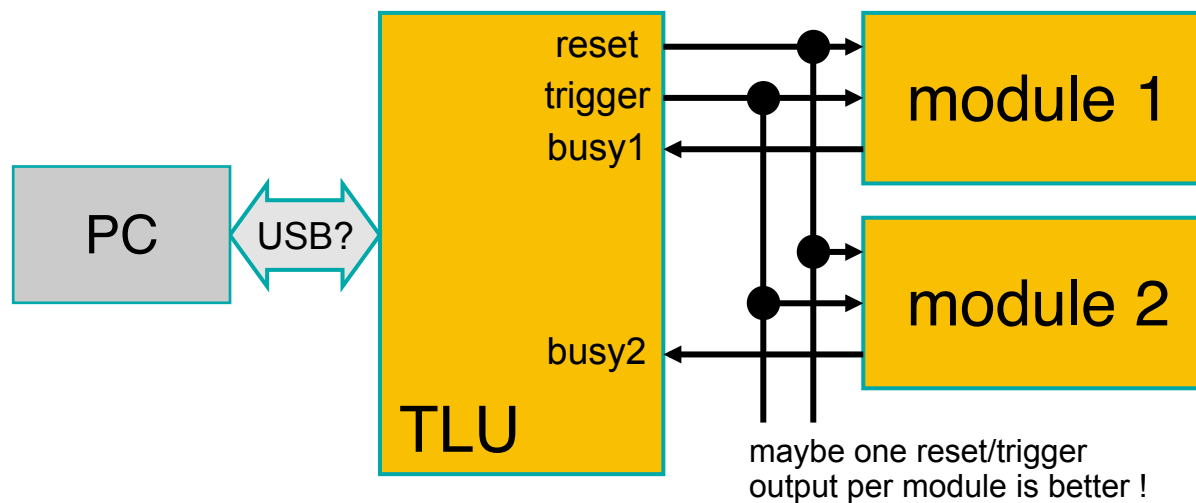
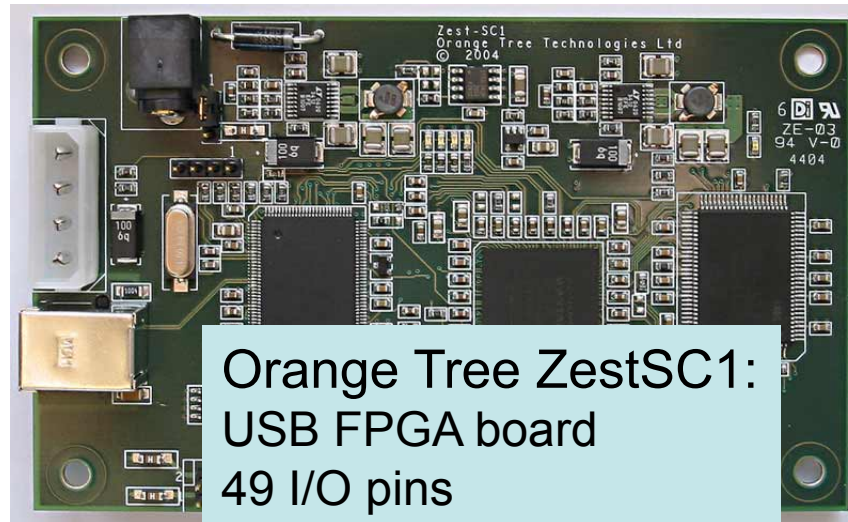
...The initial concept...

A proposal for the baseline features of a VME based DAQ card for MIMOSA-V sensors to be used on test beam experiments



- Key Ideas:
 - Frontend on daughter cards (adoptable to Pixel-DUTs)
 - Readout by VME and/or USB

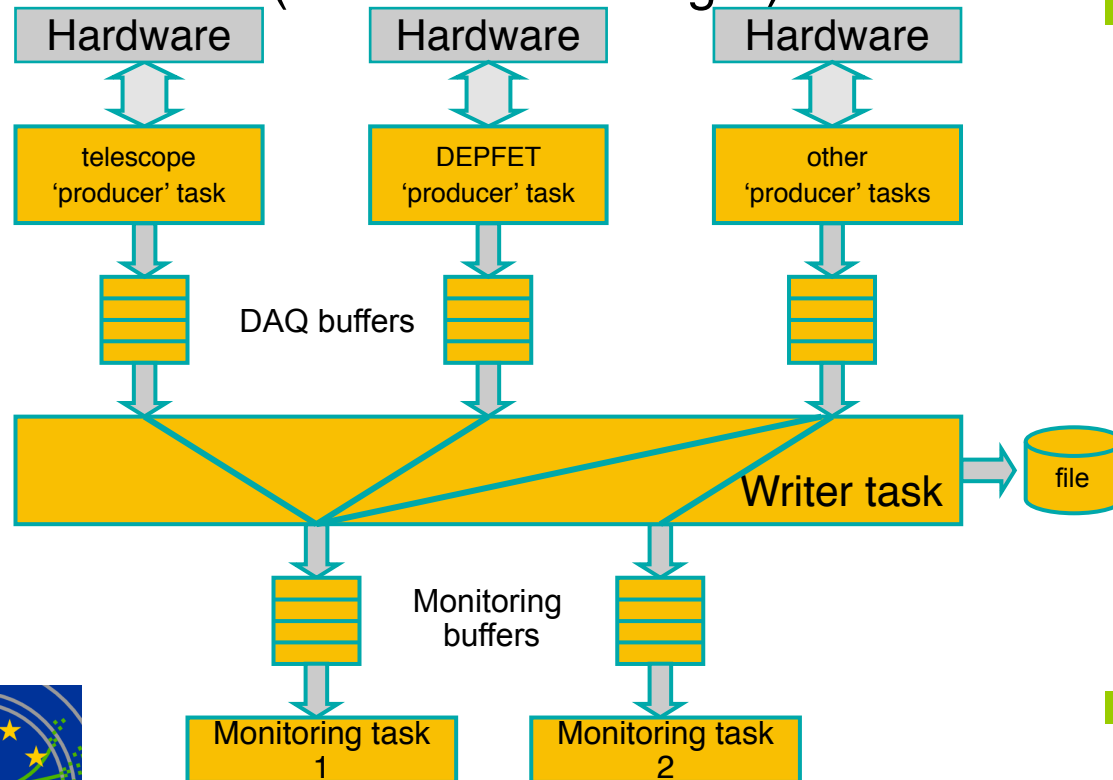
...The initial concept...



...The initial concept...

Based on DEPFET 'Mini-DAQ'

(P. Fischer/H. Krüger)

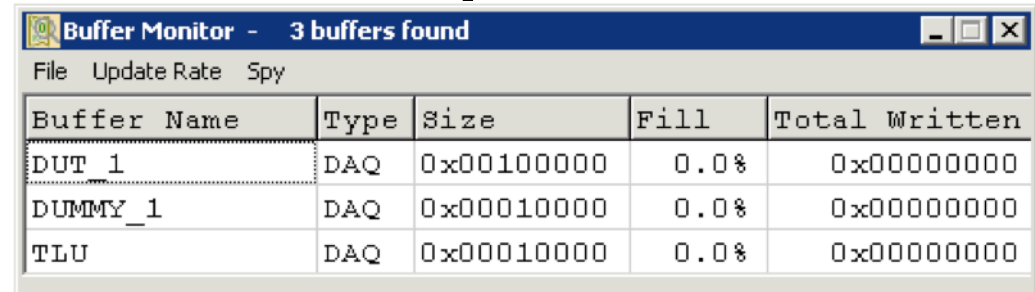


- Baseline: Depfet Bonn solution
- Missing:
 - Overall control task (flush buffers, start/stop run,...)
 - TCP/IP communication
 - Detector configuration
- Modular, flexible, OS-independent



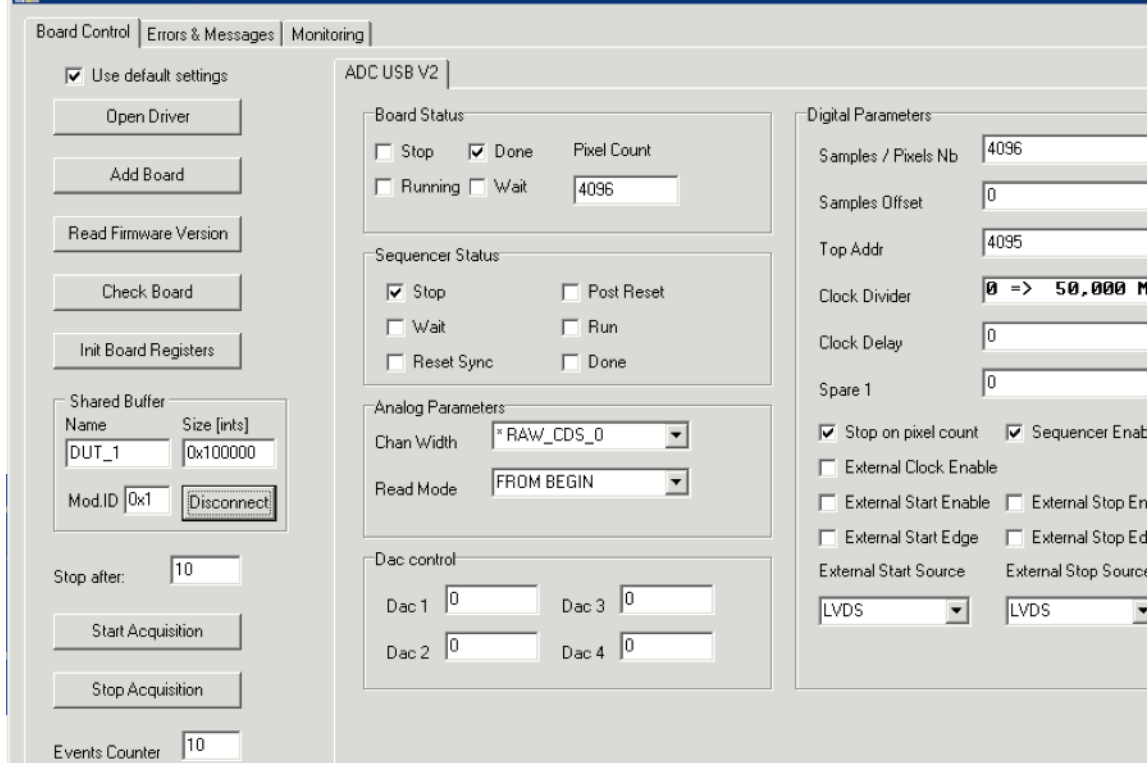
...The initial concept...

Proof of principle: Hacked
DEPFET DAQ
running on multiple
machines



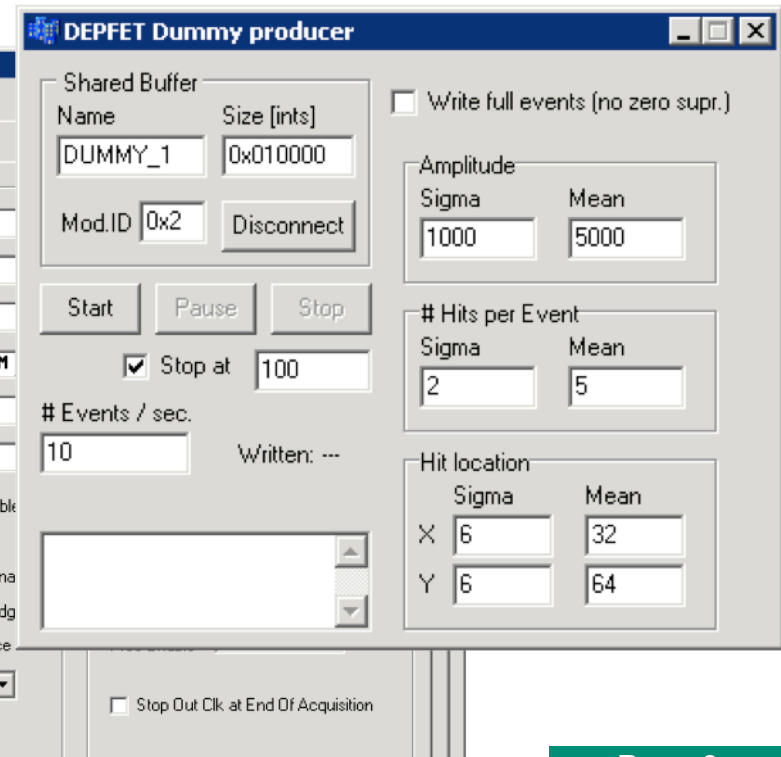
Buffer Name	Type	Size	Fill	Total Written
DUT_1	DAQ	0x00100000	0.0%	0x00000000
DUMMY_1	DAQ	0x00010000	0.0%	0x00000000
TLU	DAQ	0x00010000	0.0%	0x00000000

EUDET - Strasbourg Producer v1.0



The main interface is divided into several sections:

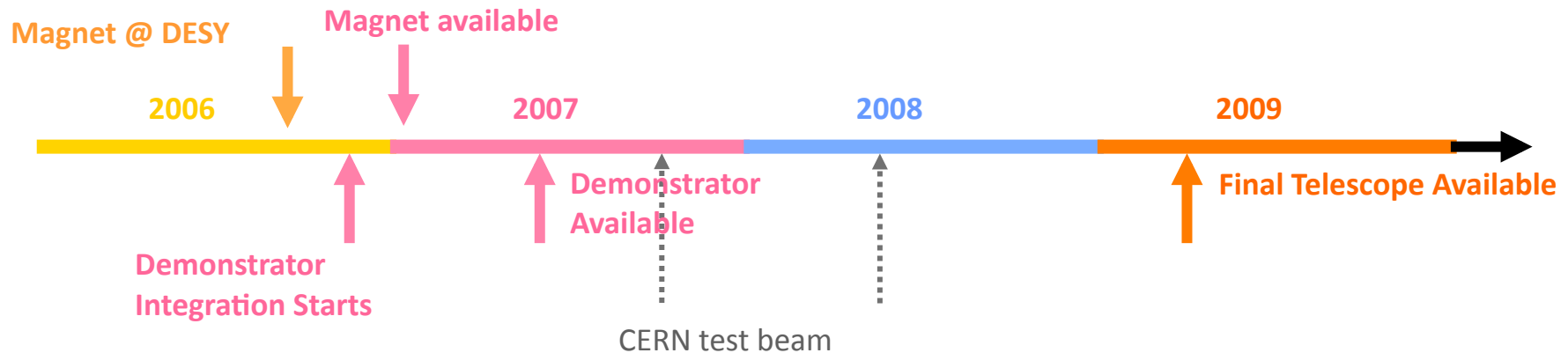
- Board Control:** Includes buttons for 'Open Driver', 'Add Board', 'Read Firmware Version', 'Check Board', and 'Init Board Registers'. A checkbox for 'Use default settings' is checked.
- ADC USB V2:** Contains 'Board Status' (Stop, Done, Running, Wait), 'Sequencer Status' (Stop, Post Reset, Wait, Run, Reset Sync, Done), and 'Analog Parameters' (Chan Width, Read Mode).
- Digital Parameters:** Includes 'Samples / Pixels Nb' (4096), 'Samples Offset' (0), 'Top Addr' (4095), 'Clock Divider' (0 => 50,000 M), 'Clock Delay' (0), and 'Spare 1' (0).
- Dac control:** Features four DAC value inputs (Dac 1-4) all set to 0.



The 'DEPFET Dummy producer' window is configured as follows:

- Shared Buffer:** Name 'DUMMY_1', Size [ints] '0x010000', Mod.ID '0x2', Disconnect button.
- Write full events (no zero supr.):** Unchecked.
- Amplitude:** Sigma '1000', Mean '5000'.
- # Hits per Event:** Sigma '2', Mean '5'.
- Hit location:** Sigma X '6', Mean X '32', Sigma Y '6', Mean Y '64'.
- Control:** Start, Pause, Stop buttons. 'Stop at' '100' (checked). '# Events / sec.' '10'. 'Written: ...'.
- Advanced Settings:** 'Stop on pixel count' (checked), 'Sequencer Enable' (checked), 'External Clock Enable' (unchecked), 'External Start Enable' (unchecked), 'External Start Edge' (unchecked), 'External Stop Enable' (unchecked), 'External Stop Edge' (unchecked), 'External Start Source' 'LVDS', 'External Stop Source' 'LVDS', 'Stop Out Clk at End Of Acquisition' (unchecked).

...The initial concept



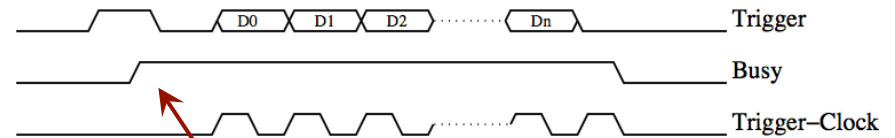
Aggressive initial timeline and Milestones have been respected and maintained over the full time



Main Ingredients - TLU

Trigger Logic Unit

- Two handshake modes
 - Simple handshake (Trigger/Busy/Reset)
 - Trigger data handshake incl. event number
- Timestamp and event-number via USB
- LVDS via RJ45, NIM and TTL via Lemo (Software-Selectable)
- Inputs for four trigger signals (ANDed, ORed, VETOed)
- Internal trigger mode and scalers for testing
- Low voltage power supply for PMTs
- Special needs for special demands:
 - Low Jitter mode (for TPCs etc.)
 - 'LHC'-users: increased timestamp resolution, central clocking



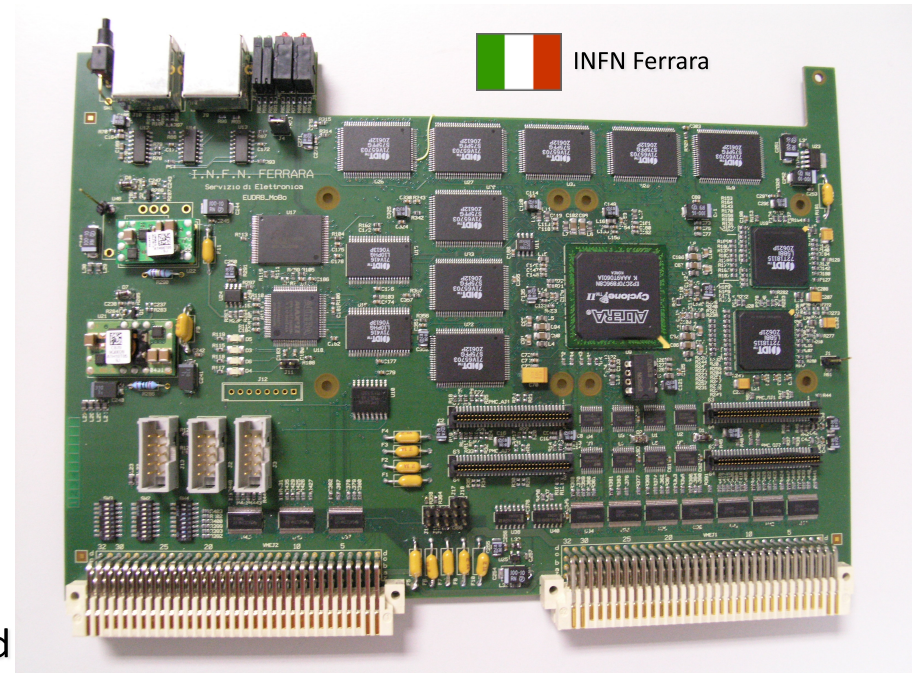
Busy acknowledges the Trigger



Main Ingredients - EUDRB

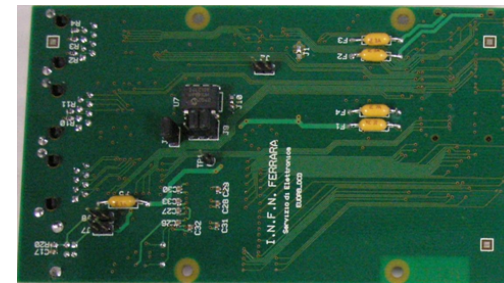
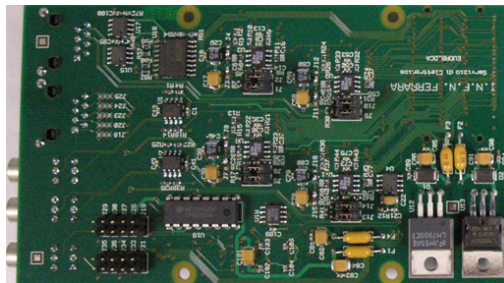
EUDET Data Reduction Board:

- Mother board with ALTERA CycloneII FPGA (clock: 80MHz) hosts core resources and Interfaces (VME64X slave, USB2.0, EUDET trigger bus)
- 2 Daughter cards (analog + digital)
- NIOS II, 32 bit “soft” microcontr. (40Mz) for diagnostics, pedestal+noise calculation and remote configuration
- Two readout modes: **Zero Suppressed** for normal data taking, **raw readout** of multiple frames for debugging or off-line pedestal and noise calculations



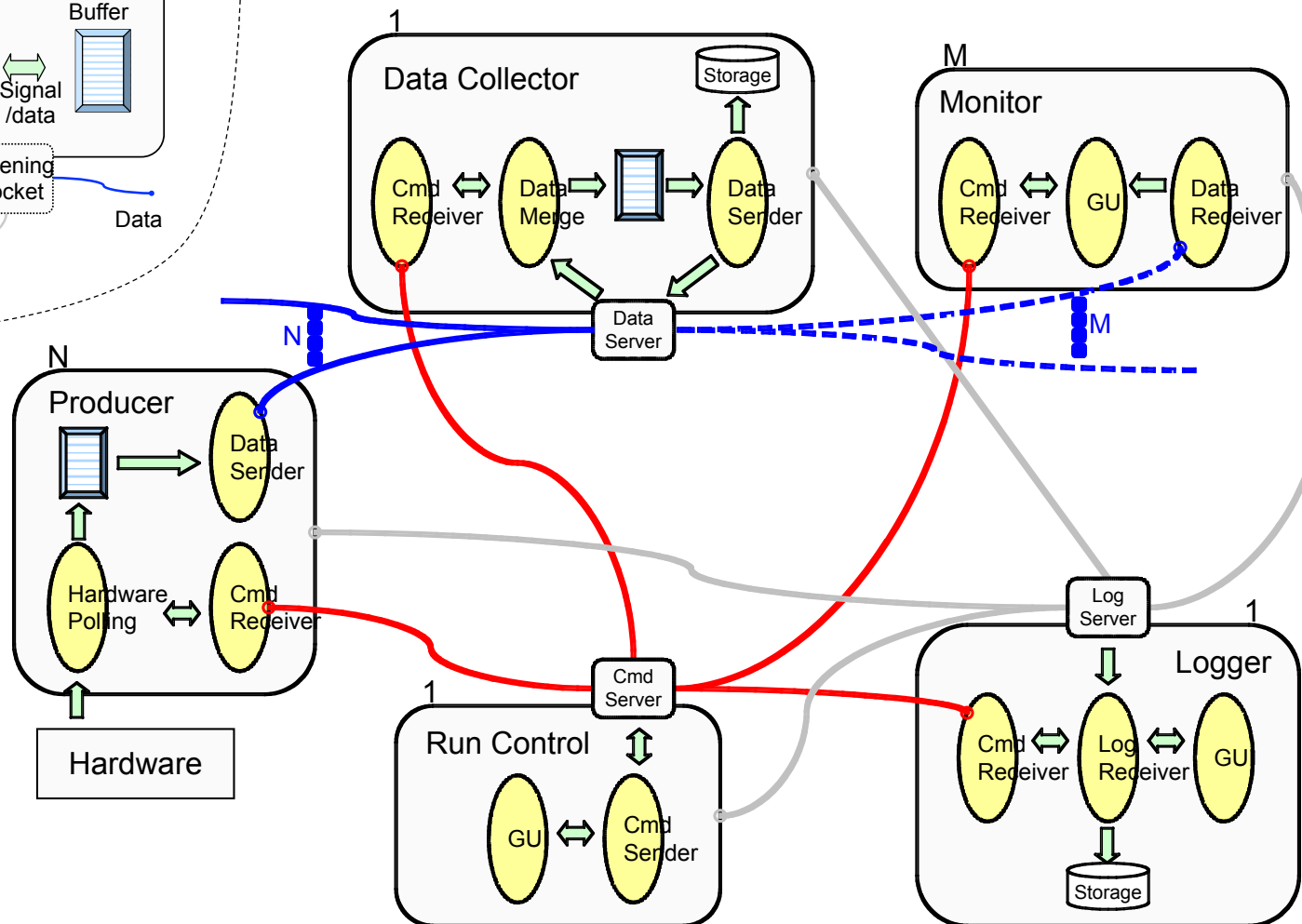
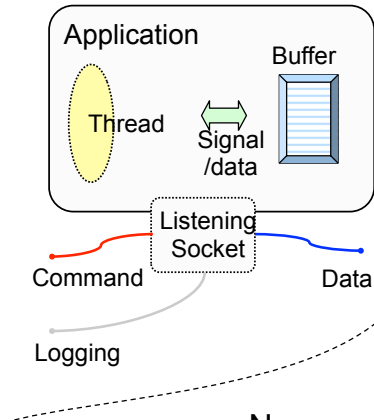
Analog Daughter card based on the successful LEPSI and SUCIMA designs clock rate up to 20 MHz

Digital daughter card drives/receives control signals for the detectors and features a USB 2.0 link



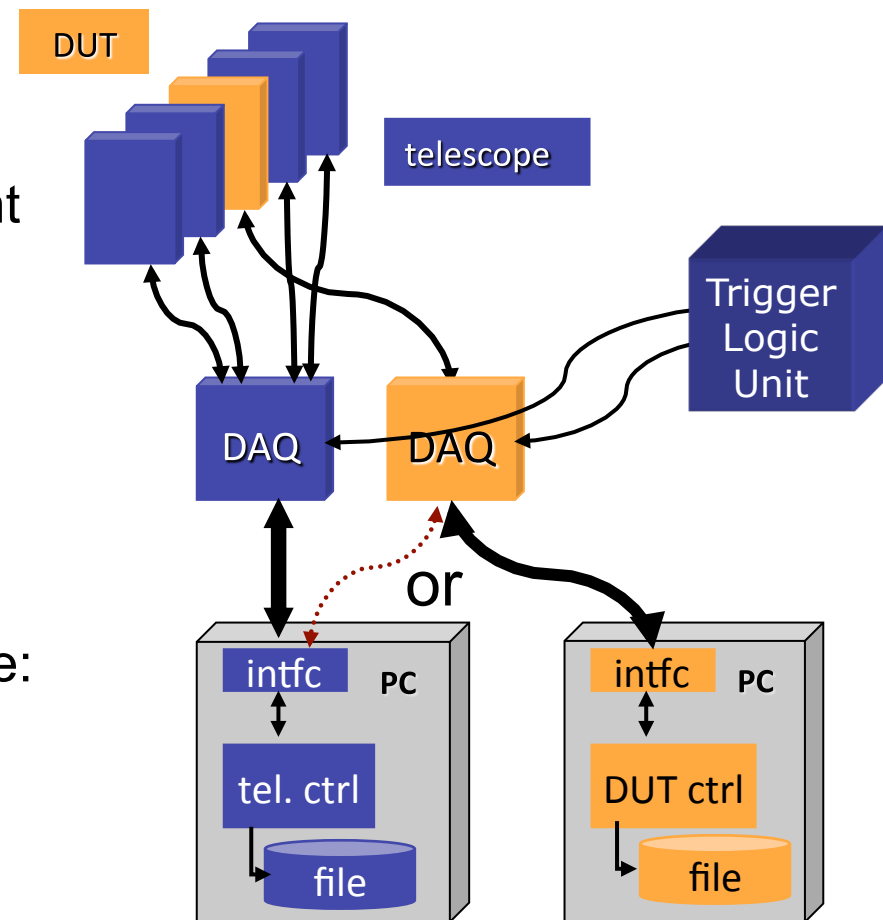
Main Ingredients – Acquisition SW

Key:



Main Ingredients – DUT Integration

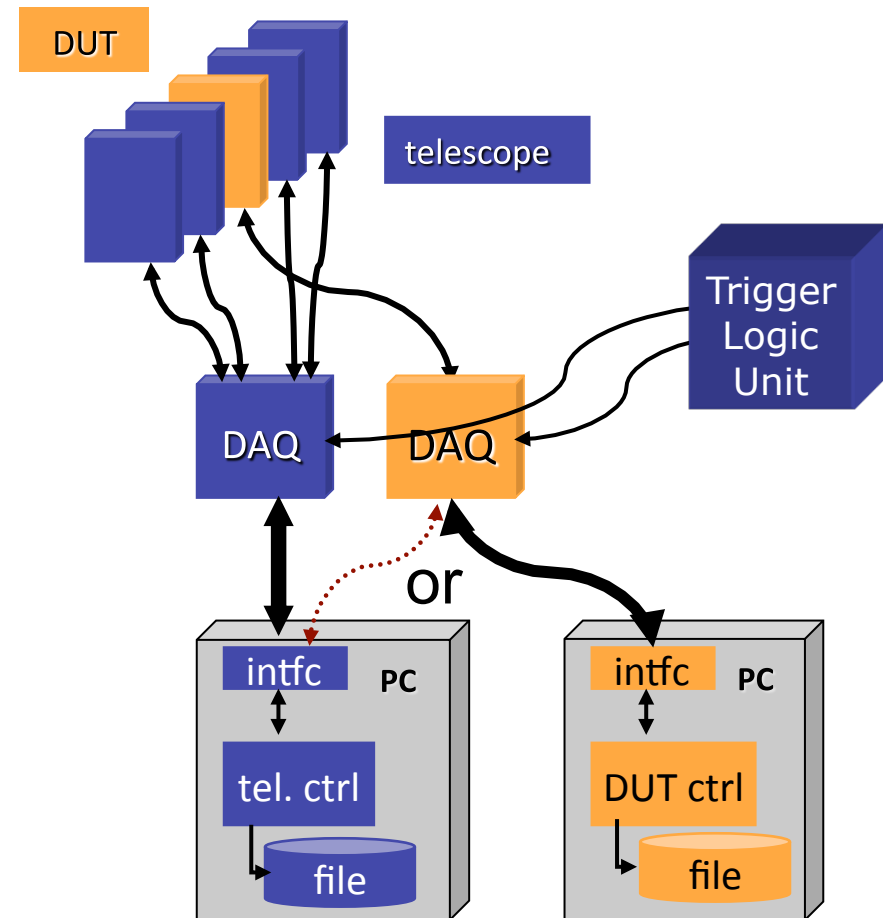
- How to integrate the DUT hardware with the EUDET beam telescope?
 - different groups with different detector technologies and different, pre-existing DAQ systems
- Use completely different hardware and DAQ for the DUT and the telescope
- Two levels of integration possible:
 - “easy” solution: at trigger level
 - full integration on DAQ software level



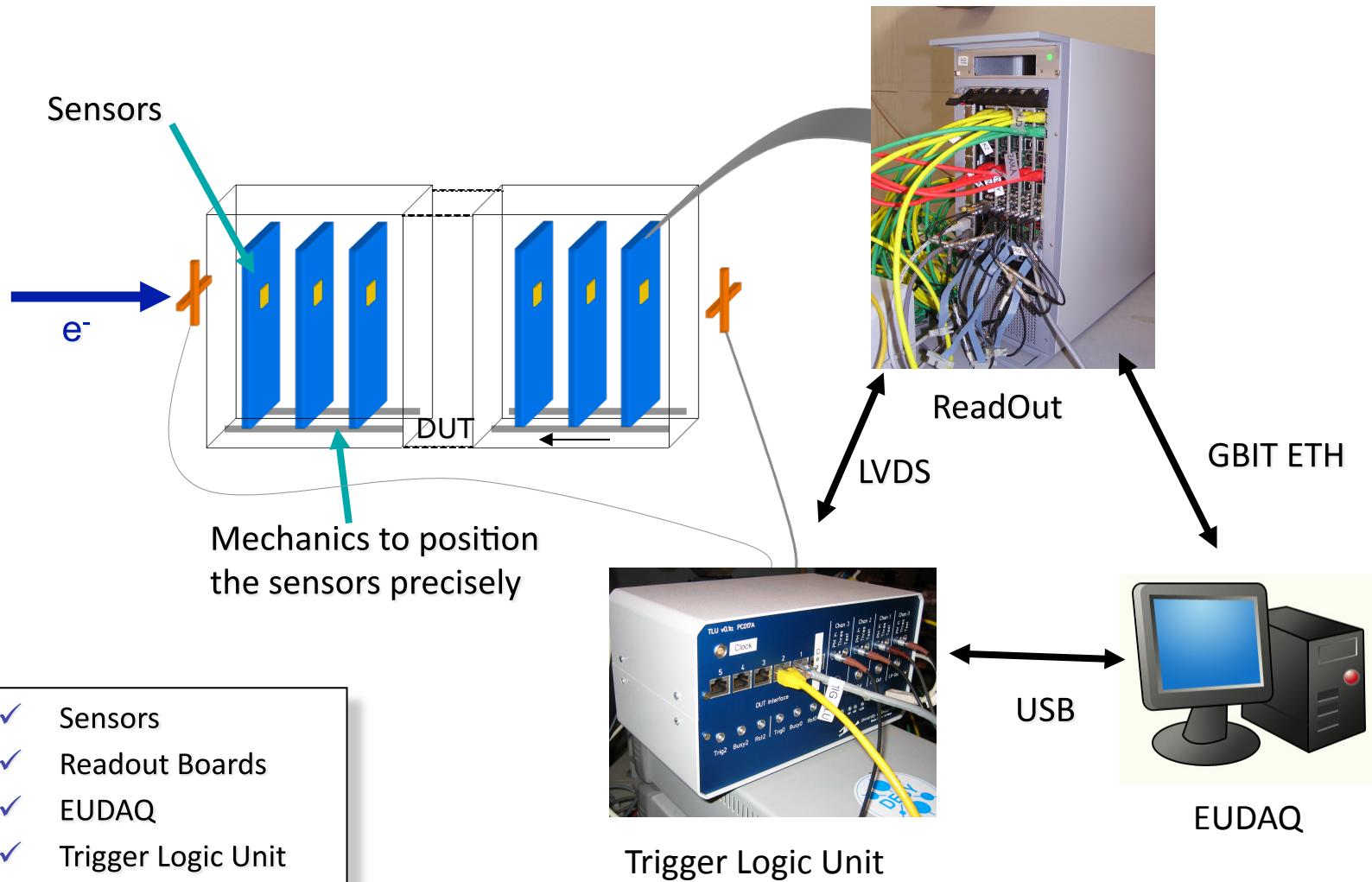
Main Ingredients – DUT Integration

Usage of EUDAQ

- Altro - Bonn (Martin Killenberg)
- APIX - Atlas Pixels (Georg Troska)
- DEPFET - Bonn (Julia Fourletova)
- FORTIS/SPIDER - Bristol (David Cussans)
- MimoRoma - INFN (Toto)
- MVD - DESY (Silvia Bonfanti)
- PixelMan - Freiburg (Uwe Renz)
- SITRA - Santander (Javier Gonzalez Sanchez)
- Taki - Mannheim (Christian Takacs / Ivan Peric)
- Timepix - Bonn (Martin Killenberg)
- Atlas TRT (Ilja Slepnev)
- 2010: NA62, Alfa, etc.



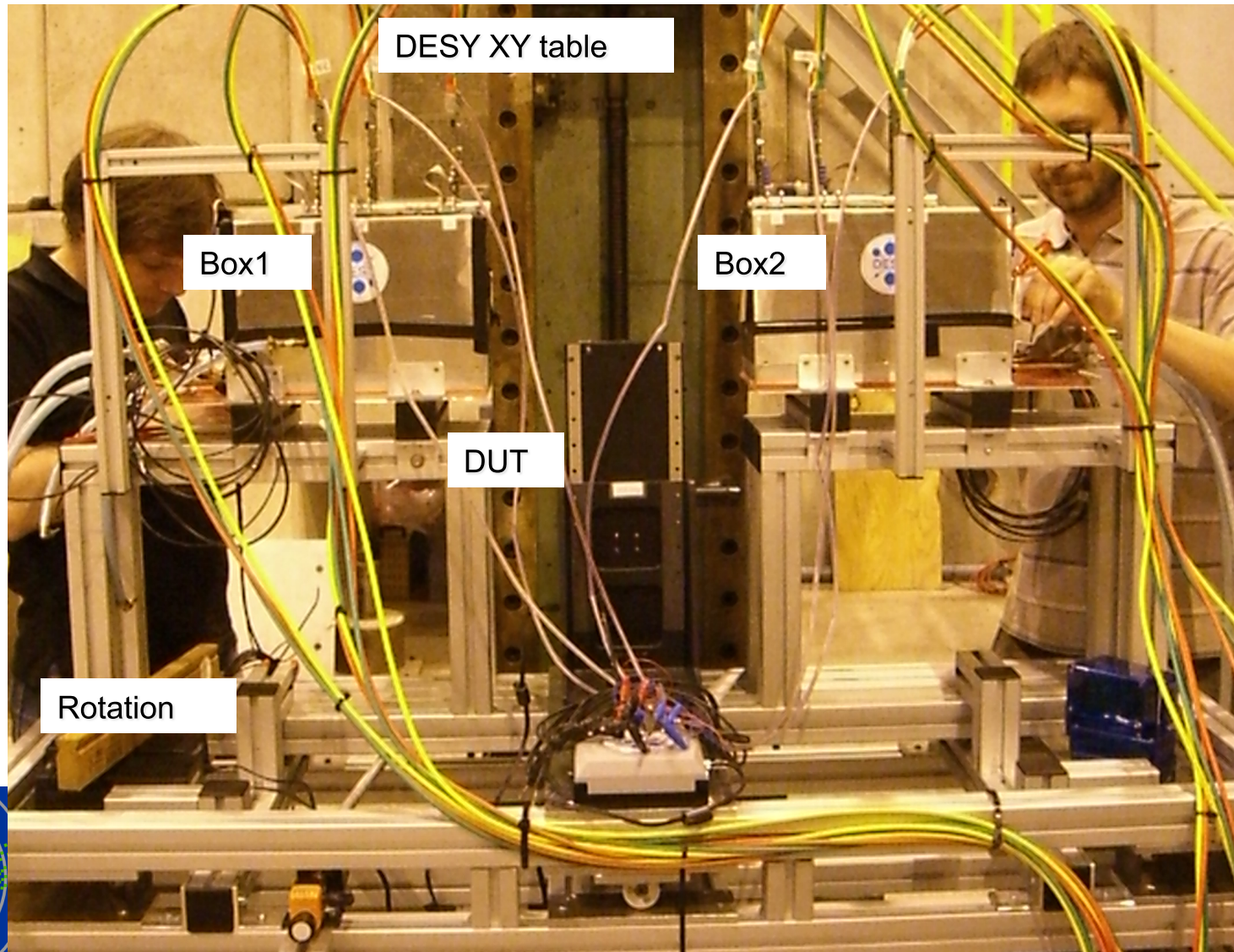
The Real Thing in the Past



- ✓ Sensors
- ✓ Readout Boards
- ✓ EUDAQ
- ✓ Trigger Logic Unit
- ✓ Mechanics



The Real Thing in the Past

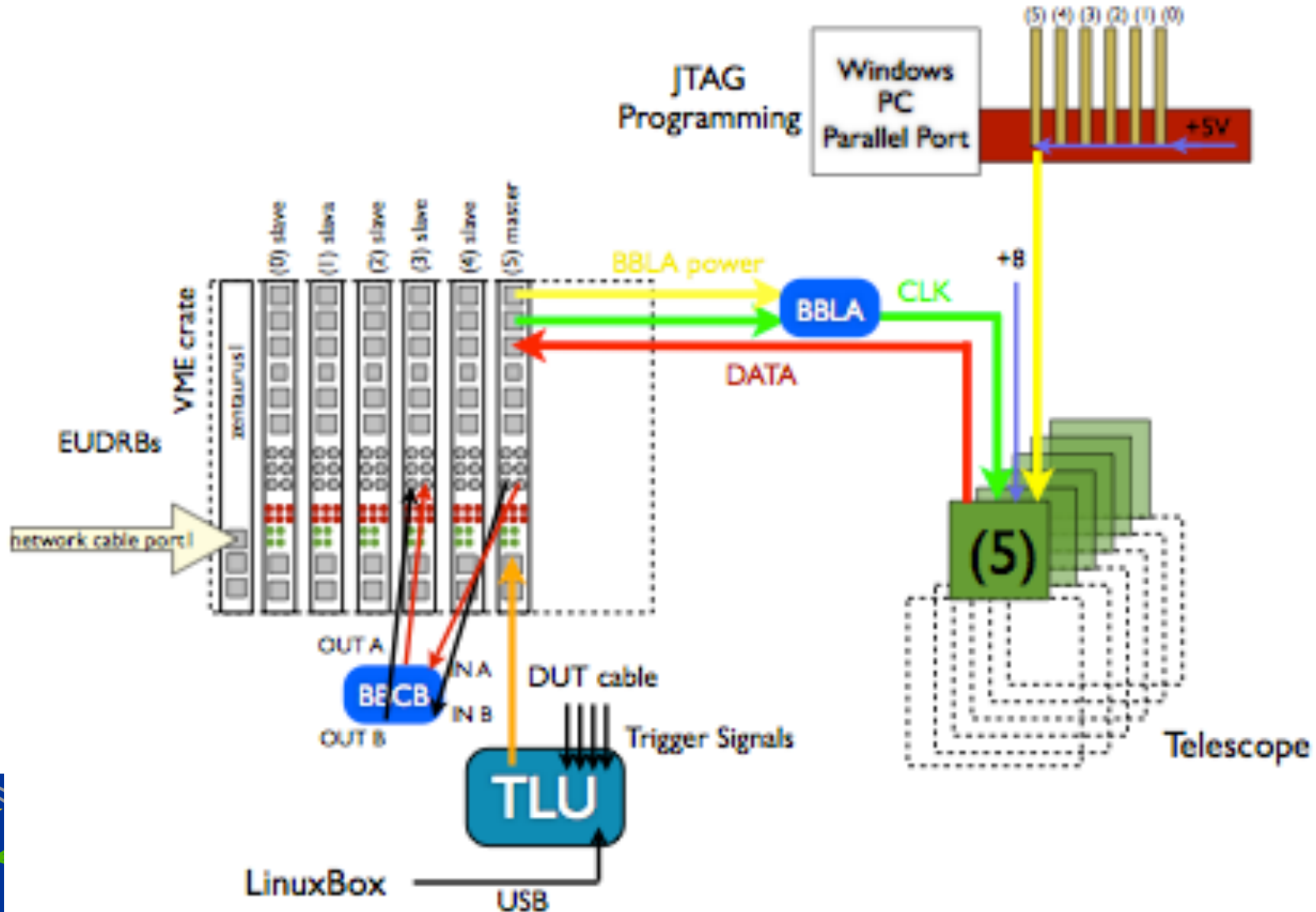


The Real Thing in the Present

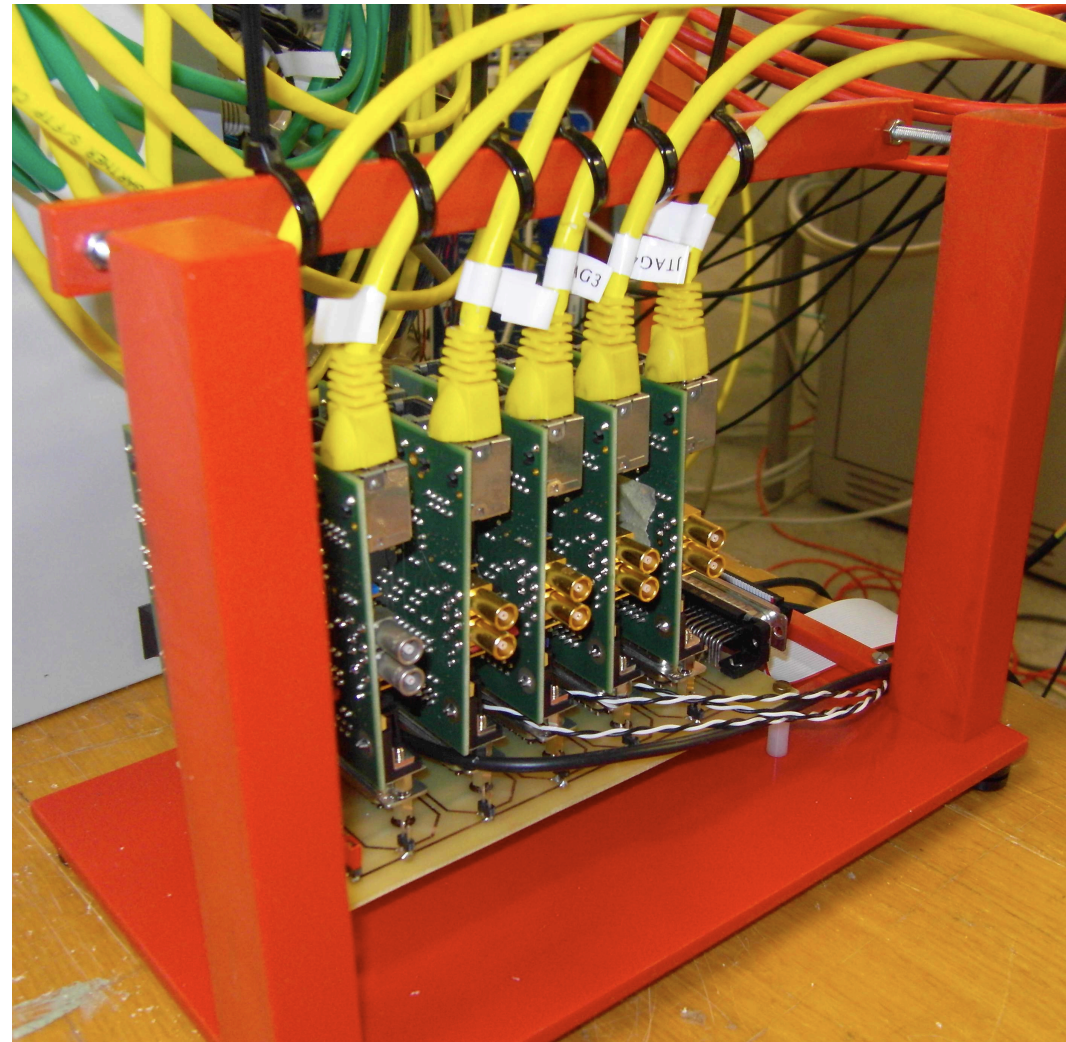
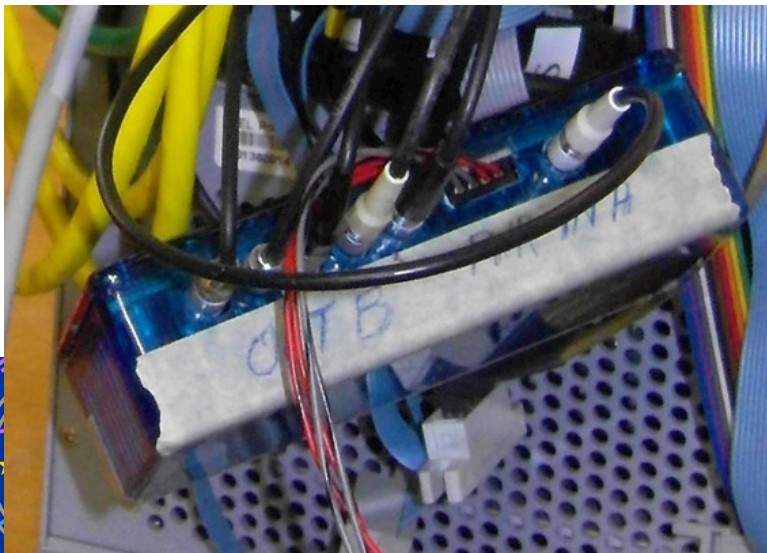
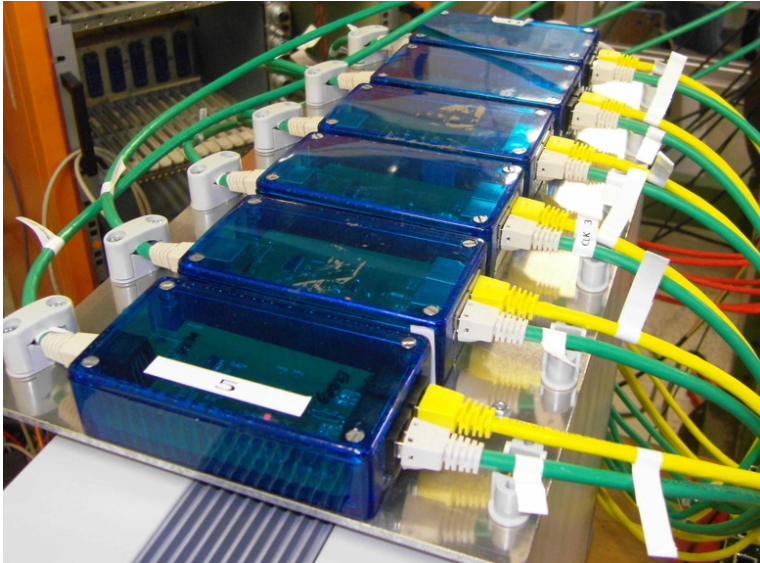
- Upgrade of pixel sensor lead to:
 - Major upgrade of EUDRBs
(also needed additional hardware)
 - Upgrade of DAQ Software and Analysis chain
- TLU got firmware upgrades etc.



The Real Thing in the Present



The Real Thing in the Present



Some numbers

Code Statistics:

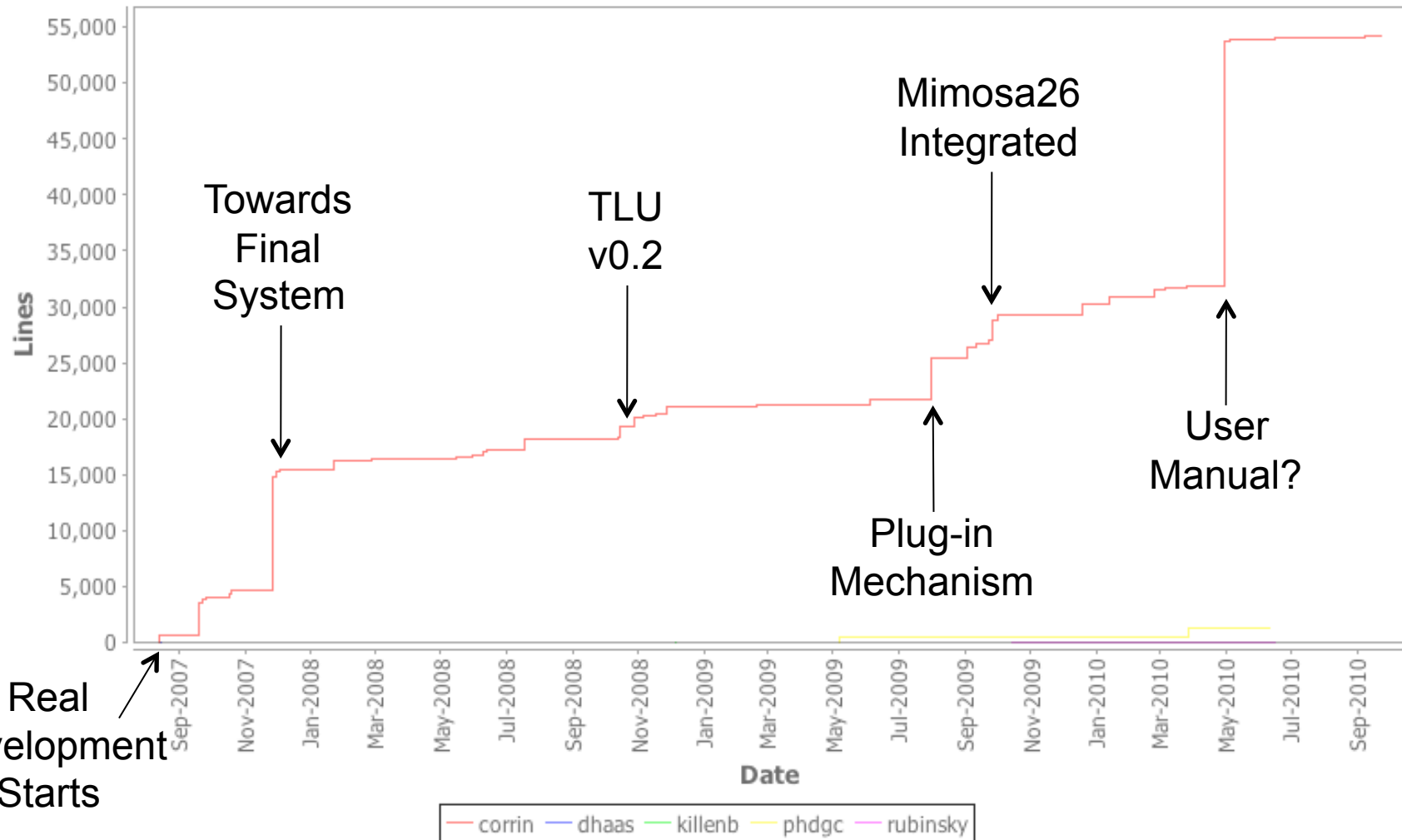
- First checked in to subversion repository in Feb 2007 (~30 source files)
- Now more than 350 source files in trunk (containing > 30 kloc)
- More than 1000 revisions
- 6 Developers registered (+ more changes by email)

Author	Commits	LOC
corrin	775	45263
killenb	82	3933
phdgc	50	1448
renz	43	2132
dhaas	39	449
rubinsky	12	119



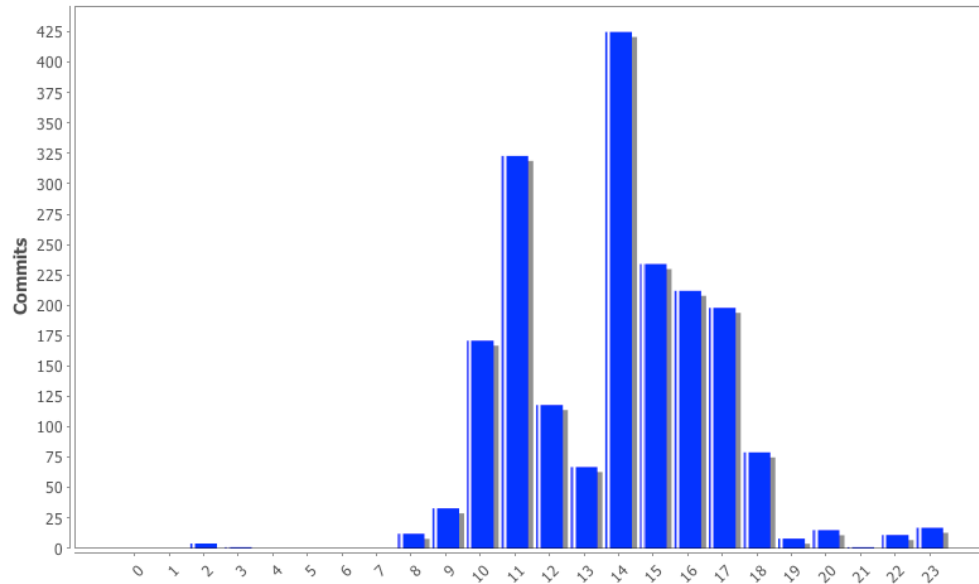
Some numbers

/trunk: Contributed Lines of Code

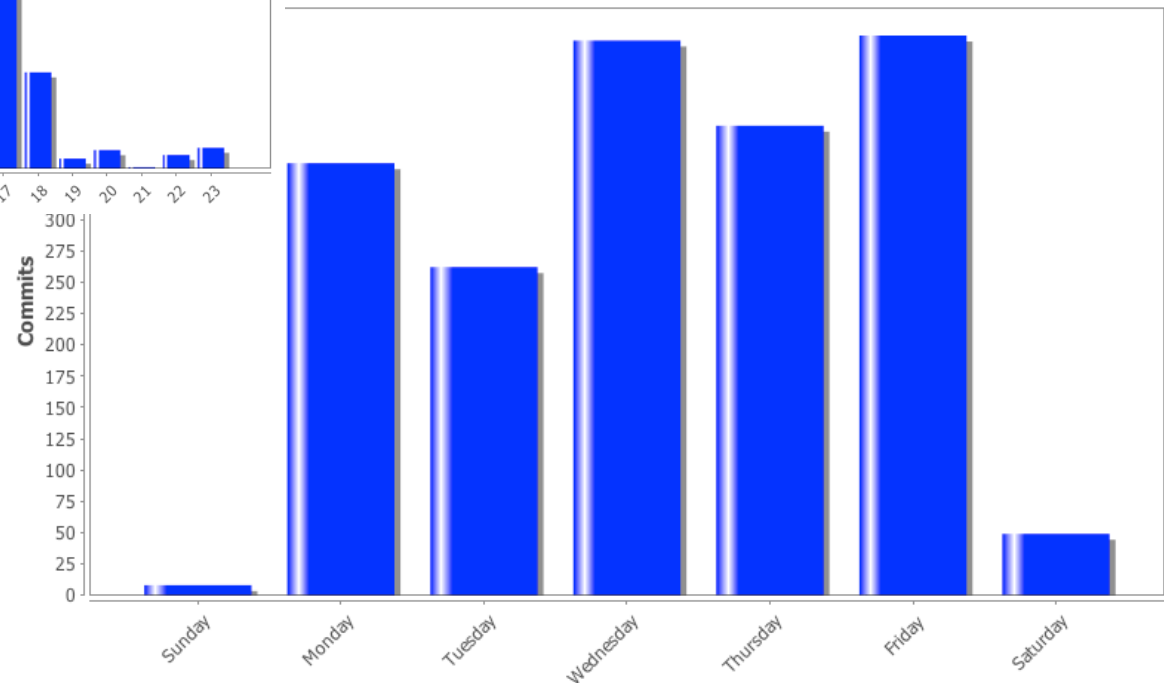


Some numbers

/trunk: Activity by Hour of Day



/trunk: Activity by Day of Week



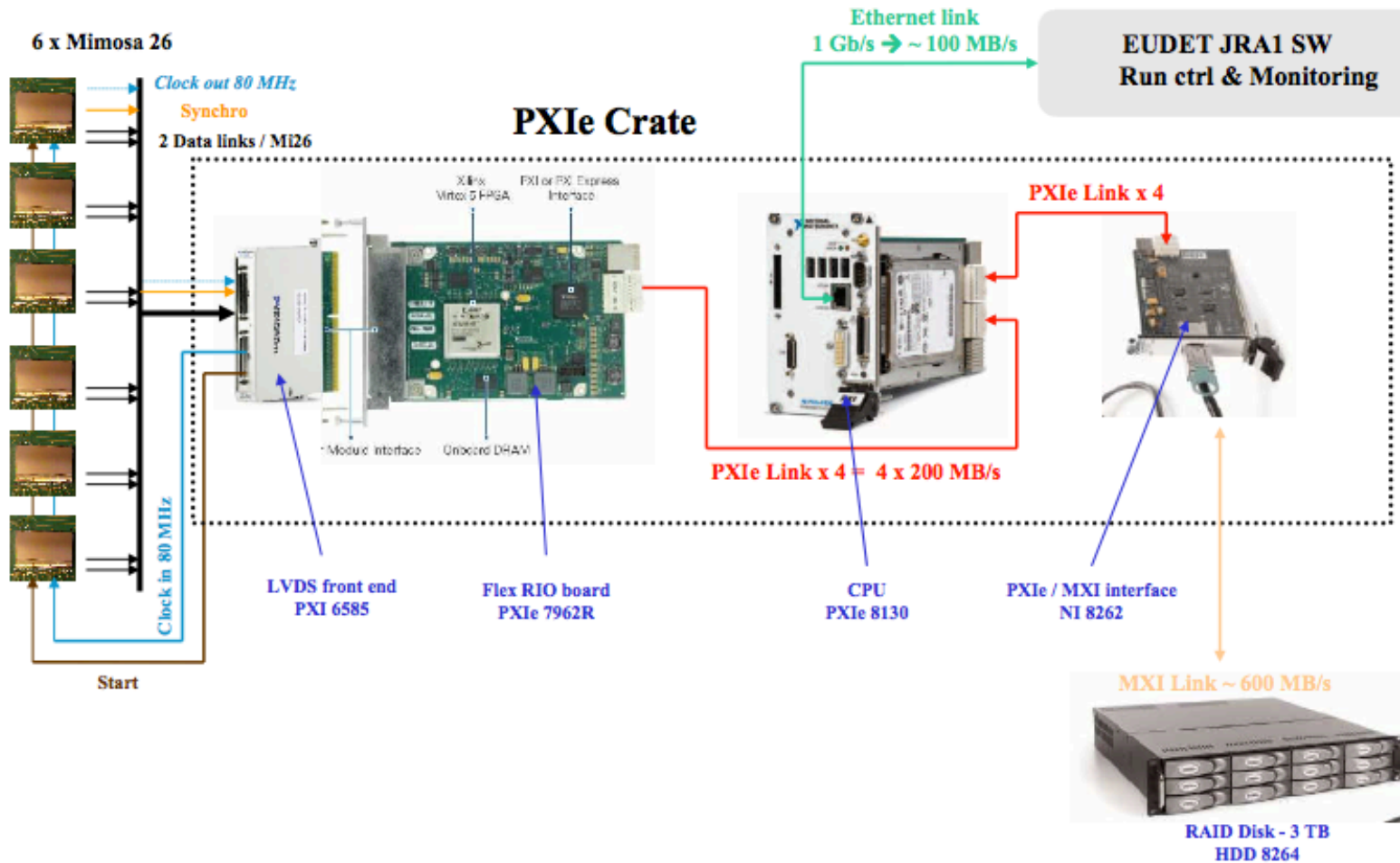
Outlook to AIDA

- One order of magnitude bigger!
- Implications on HW and SW:
 - EUDRBs cannot scale to that level, will use ‘commercial’ readout based on NI boards (already under development)
 - EUDAQ can still scale, but is now in competition with the ‘big beasts’ like XDAQ
 - Common effort to streamline things should be done now!



Outlook to AIDA

DAQ : Proposal of DAQ based on Flex RIO



Conclusions

- FAQ (2005-2010): Why do you want to build a beam telescope, everybody can do this/has done this!
- Answer (2010): Yes, true, but ours has been integrated and used 84 weeks by ~30 different users in 3.5 years (>300 MEvents in 2010 alone) and basically running non-stop at CERN and DESY in the last 3-4 testbeam seasons



Conclusions

- TLU is a real ‘seller’: Common starting point of integration
- EUDAQ was extremely successful: Up to 8 DUTs, sometimes 2 different DUTs from different communities – Integration to the DAQ framework was standard in the last 2-3 years
- Copies of the telescope will be prepared, ‘old’ MVD-telescope runs with EUDAQ



Conclusions

- Activities in JRA1 have been a lot of fun and (even) a lot (more) of work
- Community building/transnational access has been eyed suspiciously in the beginning, but proven very productive for JRA1
- AIDA will continue the efforts of EUDET and can hopefully profit from the achieved results

