

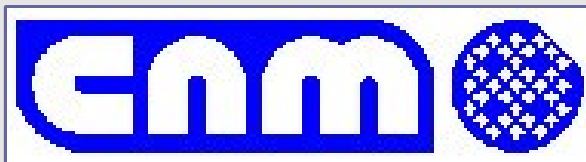
IR Transparent Si microstrips

(alignment optimized Si sensors)



IFCA SiLC (a.o.):

Marcos Fernández, Javier González,
Richard Jaramillo, Amparo López,
David Moya, Celso Martínez Rivero,
Francisca Munoz, Alberto Ruiz, Iván Vila



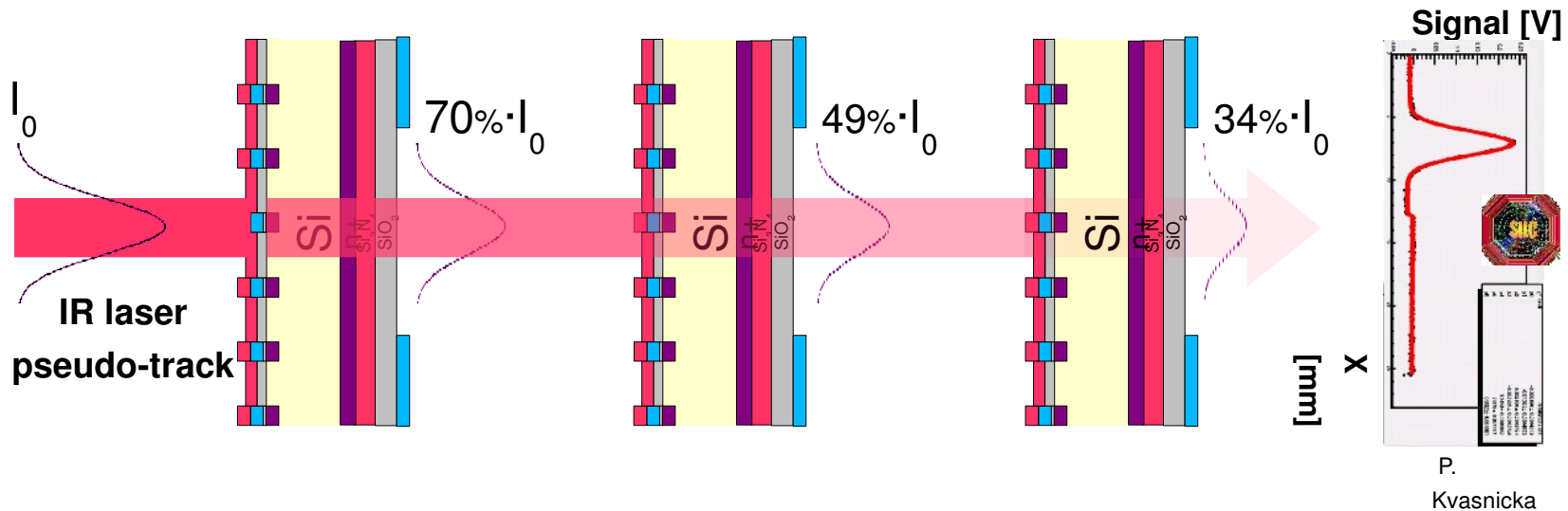
CNM SiLC (a.o.):

Daniela Bassignana, Manuel Lozano,
Giullio Pellegrini, Enric Cabruja,
David Quirion



Microstrips as semitransparent light detectors

Laser tracks can be used by a hardware system to align the tracker



Goal of this project is to improve transmittance to infrared light of microstrip detectors. Main constraint is not to alter the standard production process, and not to include alien materials

Once pitch is fixed, the key to increase transmittance is the thickness of top&bottom passivation layers. Note: The passivation consists of a double layer of Si_3N_4 on SiO_2 . The sensors are passivated from the top and from the bottom.

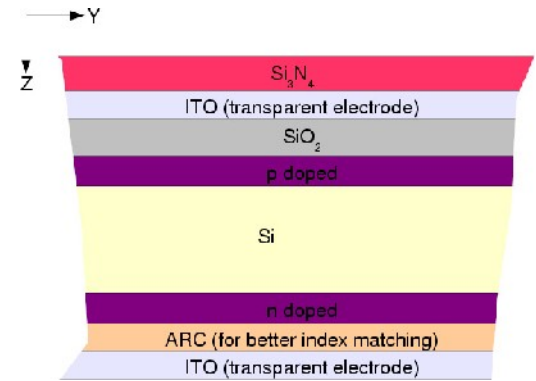
Highlights of this project within EUDET framework

1st year: conceptual design, proposals and perspectives

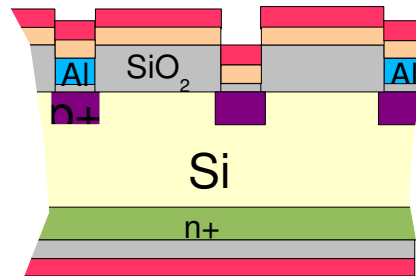
2nd year: Simplified simulation of μ strips as plane-parallel layers.

Validation of plane parallel simulation

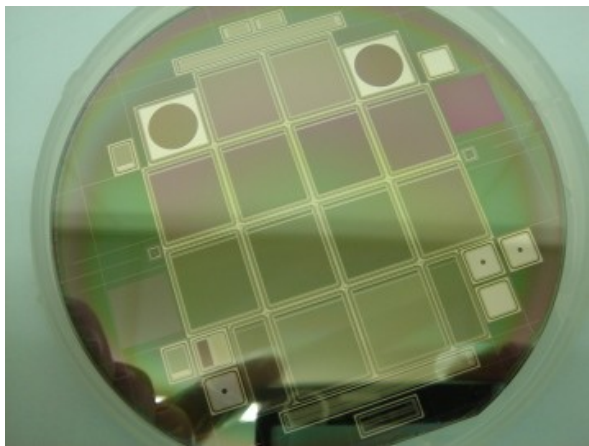
Beginning of realistic study (segmented strips)



3rd year: Full simulation of μ strips (interference and diffraction)



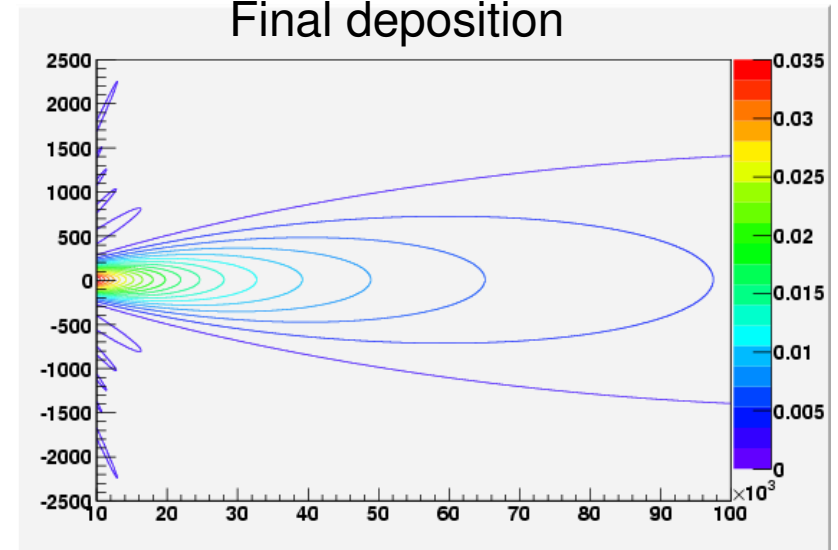
4th year: Production of prototype transparent microstrip detectors



5th year: Validation of realistic simulation:

Far field calculations

Final deposition



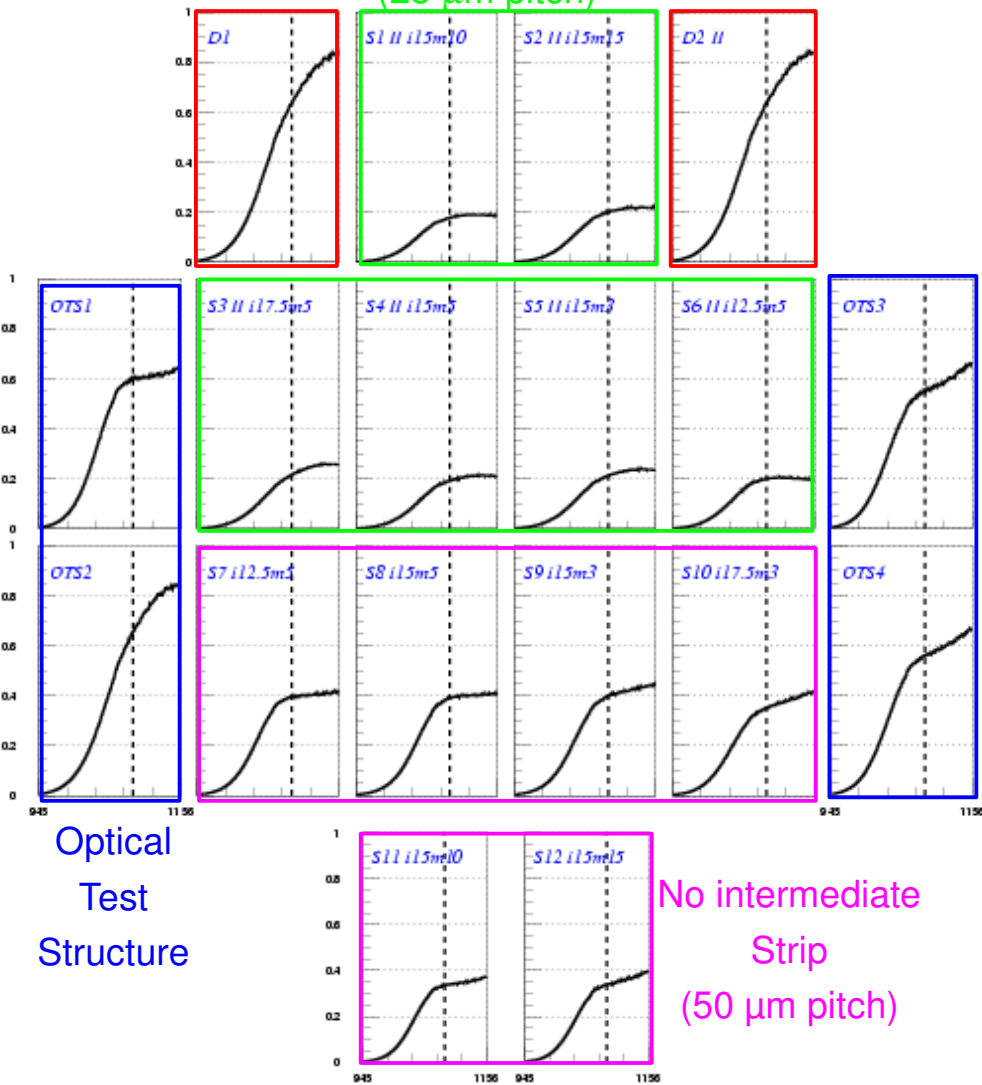
Main results achieved

- Strips (having metal or not) behave as a diffraction grating. Sensors with intermediate are more “efficient” gratings.
- Pitch reduction (=closer strips) decreases transmittance (1st order effect) and increases reflectance (2nd order).
- Strip width increases reflectance (1st order), and reduces transmittance (2nd order).
- Top and bottom passivation layers behave as an AntiReflection Coating (ARC)
Top passivation thickness more critical than bottom.

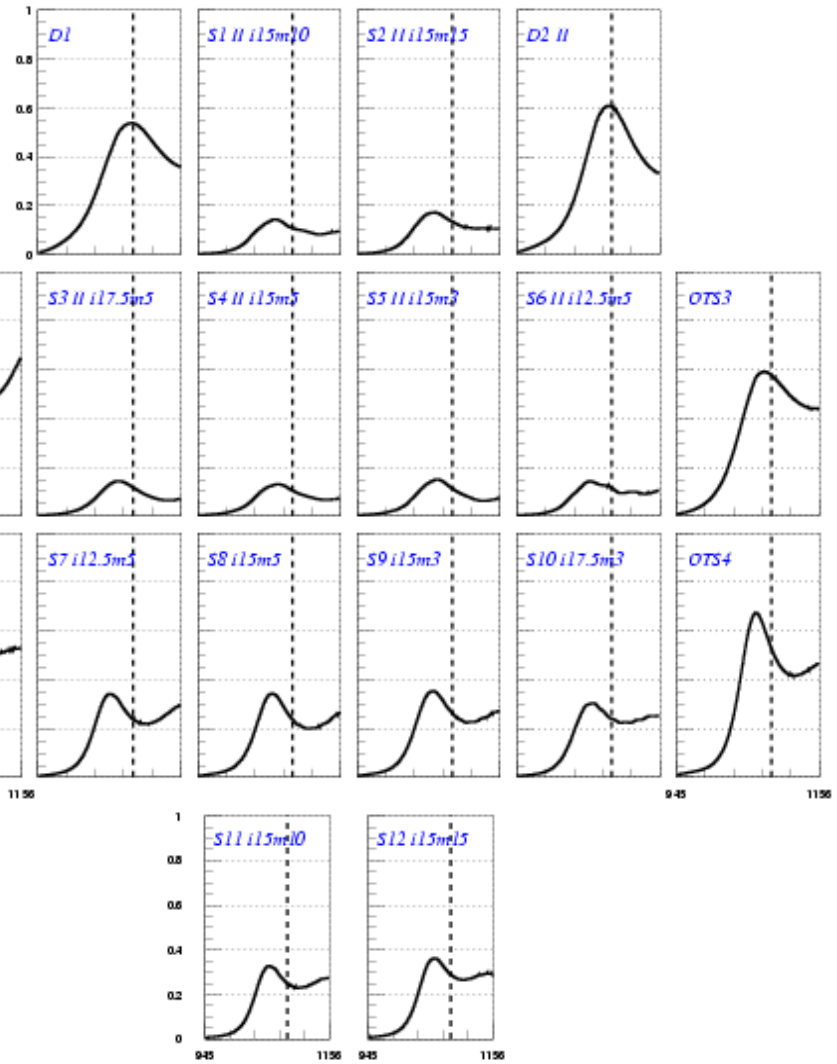
Wafer 1, measured

1 intermediate
strip
(25 μm pitch)

Diode



Incomplete top&bottom passivation
Transmittance~40%

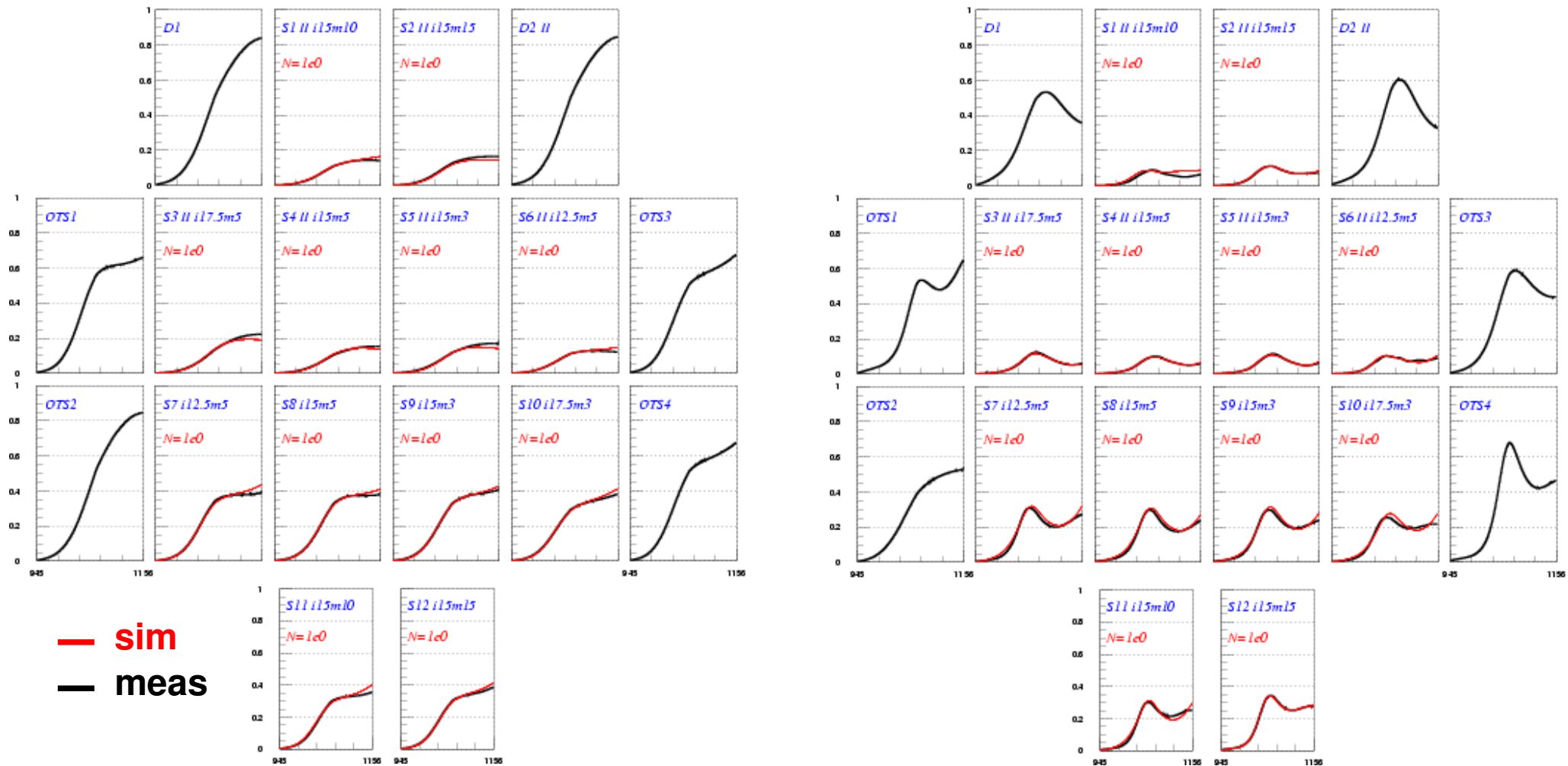


Complete top&bottom passivation
Transmittance~20%

Wafer 1&2, finished

- First 2 wafers were finalized in 2 steps.
- First step was the deposition of SiO₂ (top and bottom)
 - Good news: transmittance of selected sensors ~40%
 - Measurement differs from simulation by a constant scale factor
 - The scale factor is different from sensor to sensor
- Deposition of Si₃N₄ (2nd step) had to be done before end of year 2009
 - Finalized wafers had lowered transmittance
 - We realized that transmittance depends on measurement distance.
 - We need to propagate the calculated fields to far distance

Wafer 1, far field fits



Simulation is validated !!

Final step for the last 3 remaining wafers

- Three wafers left

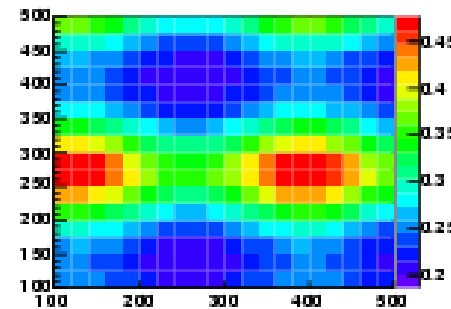
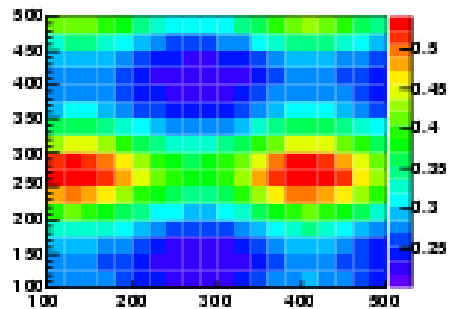
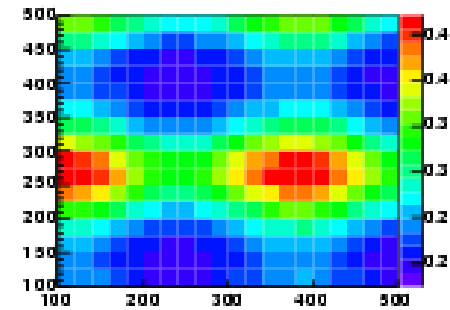
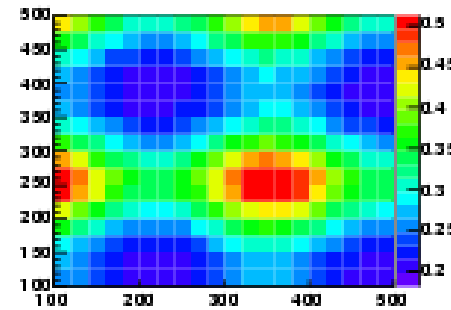
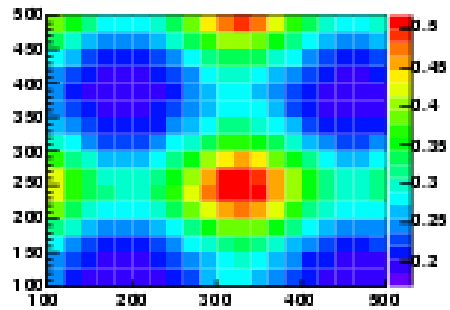
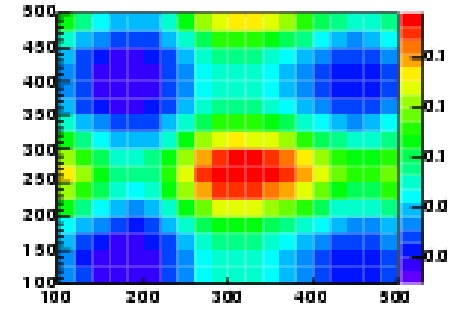
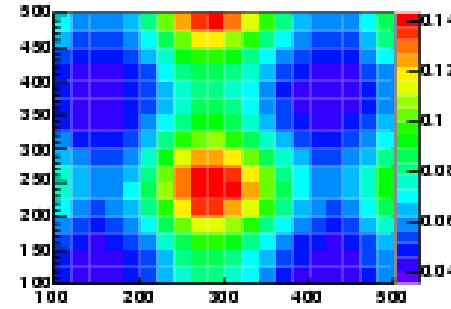
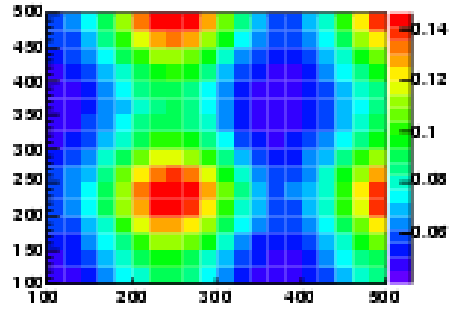
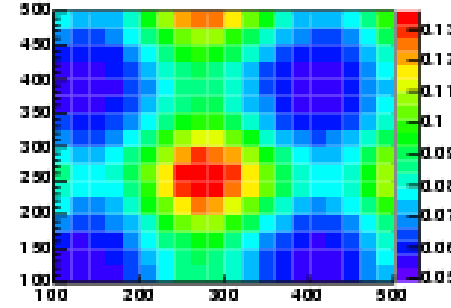
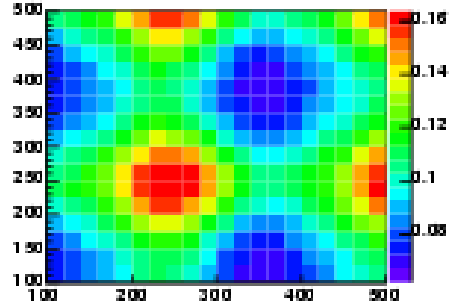
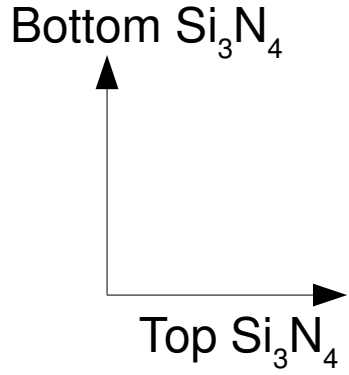
Conservative approach: deposit desired thickness of Si₃N₄ in few steps

Measure after each step

- We have calculated the expected transmittance using the measured thickness of the deposited materials
- Next 3 pages show $T = T(\text{top Si}_3\text{N}_4 \text{ thickness}, \text{bottom Si}_3\text{N}_4 \text{ thickness})$

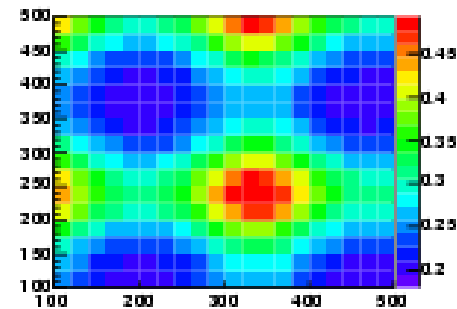
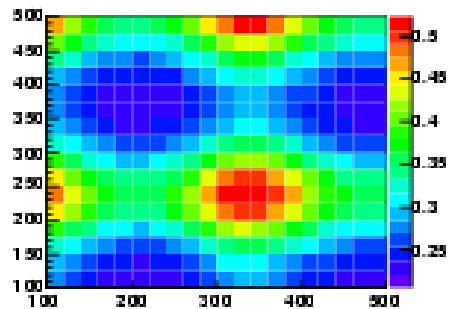
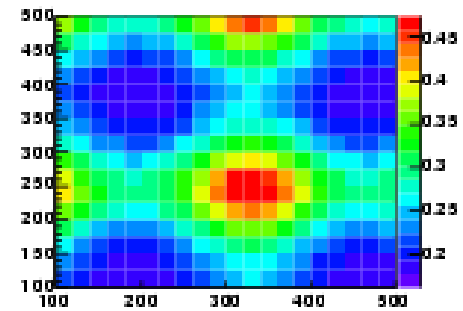
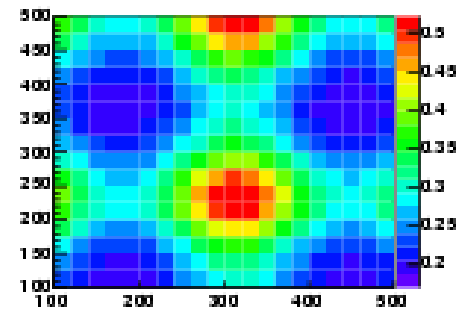
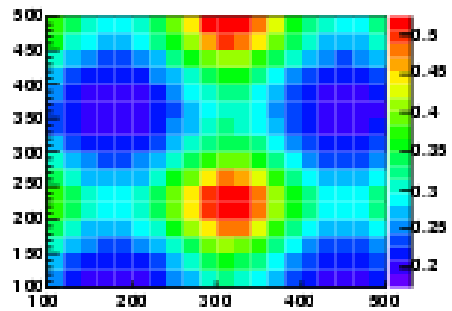
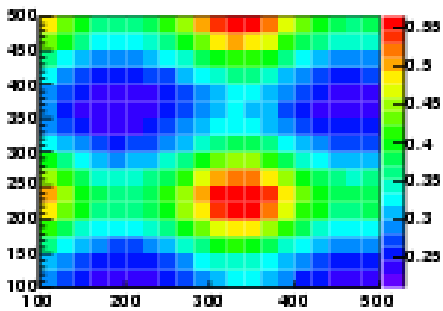
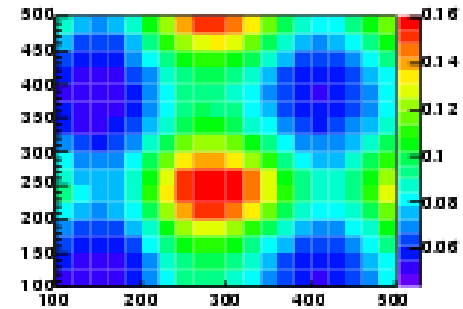
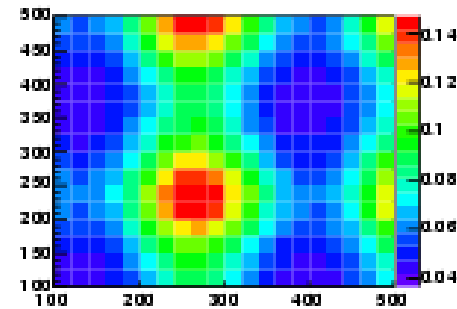
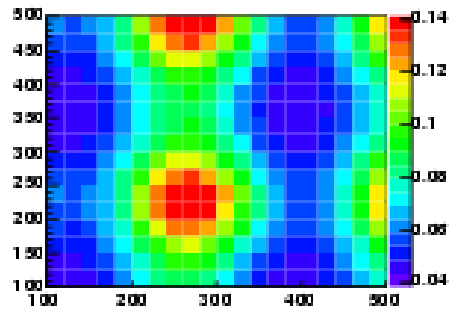
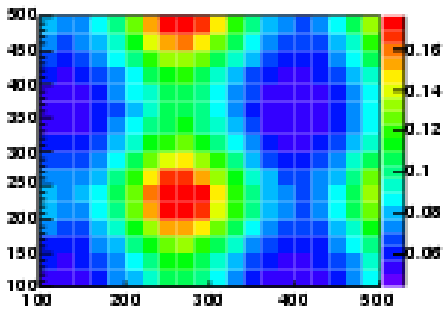
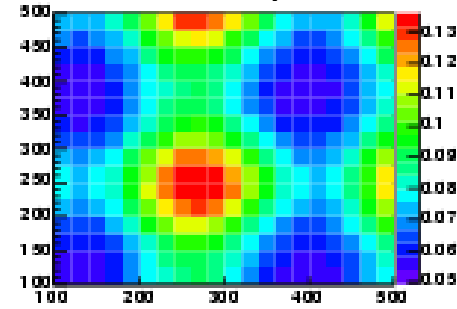
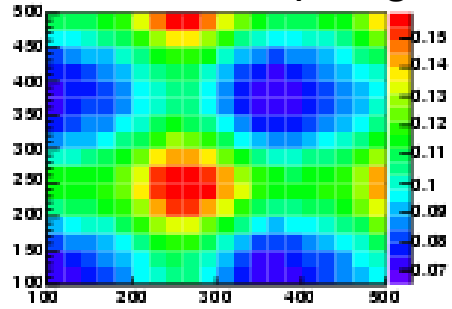
Wafer 3: Sequential deposition of Si₃N₄

(using measured thickness)



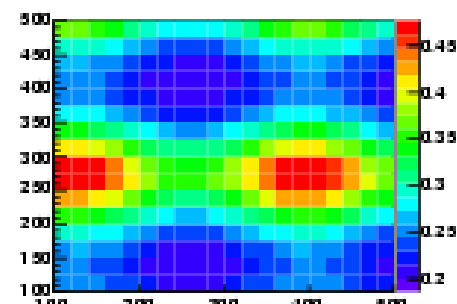
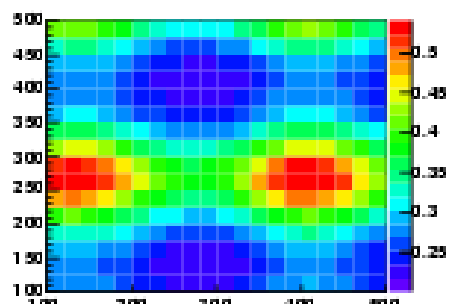
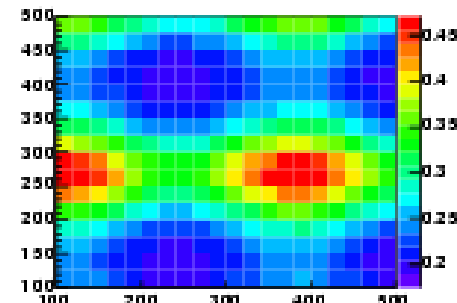
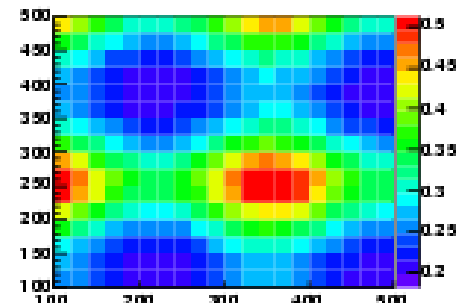
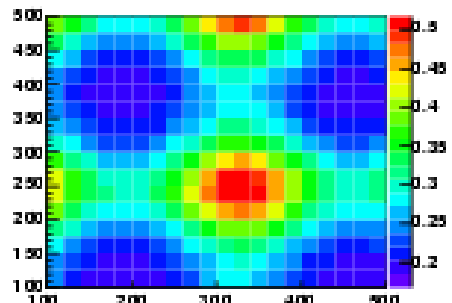
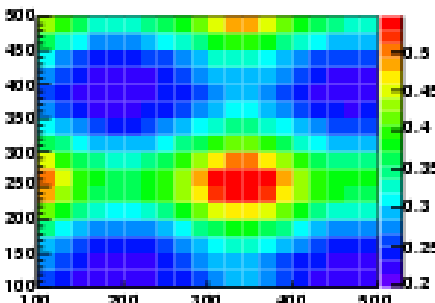
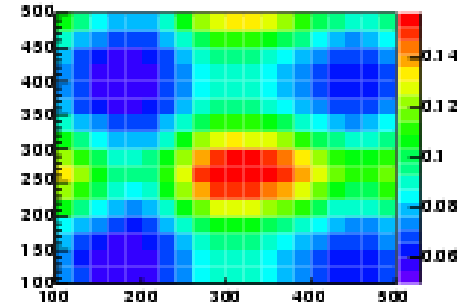
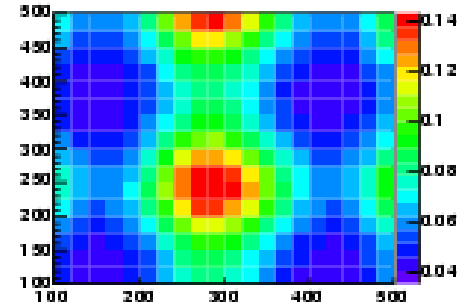
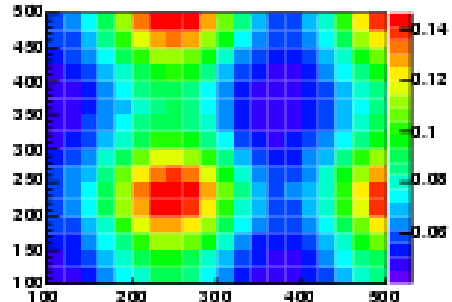
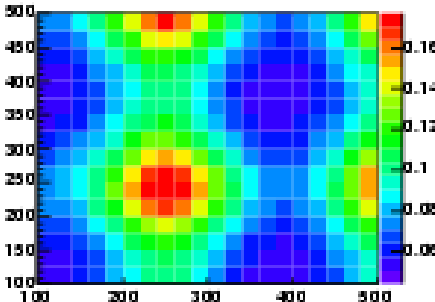
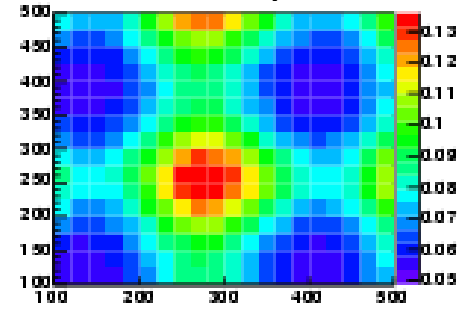
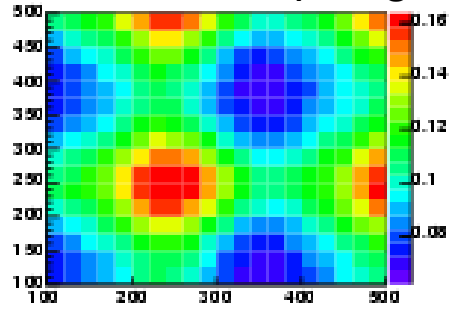
Wafer 4: Sequential deposition of Si₃N₄

(using measured thickness)

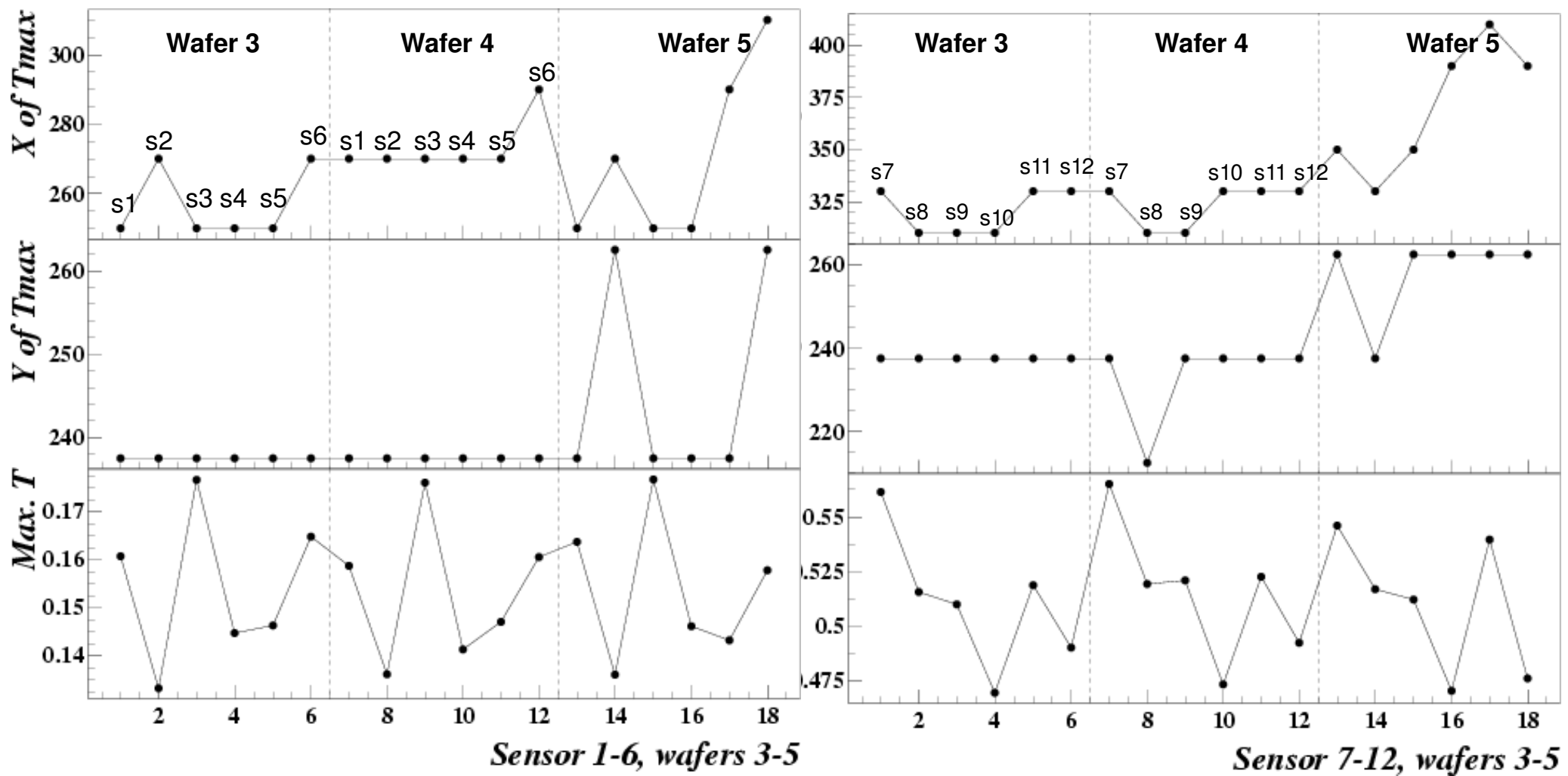


Wafer 5: Sequential deposition of Si₃N₄

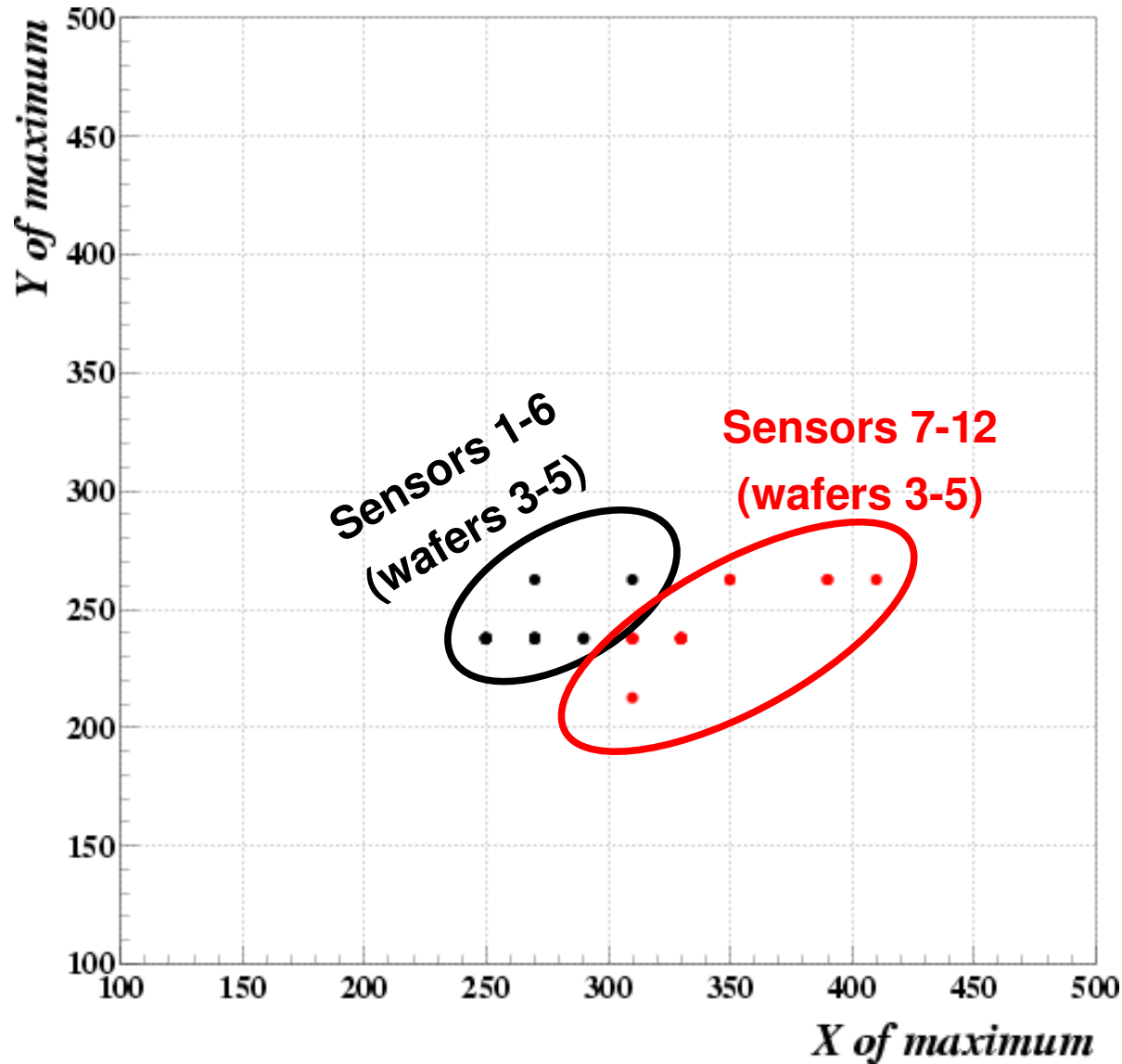
(using measured thickness)



(x,y) of first maximum vs sensor id in wafers 3, 4, 5



Scatter plot of (x,y) of first maximum for wafers 3, 4, 5



Note: Each ellipse contains 18 entries (6 sensors × 3 wafers) showed in the former slide

Conclusions

Sensors with intermediate microstrips have lower %T

Thickness of bottom Si₃N₄ passivation layer does not depend on the sensor type

Upper Si₃N₄ layer is thicker for sensors without intermediate strip

Therefore, thickness does not depend on the wafer but on the sensor

Deposition of last Si₃N₄ (2 layers/sensor) has been agreed with CNM

Run will be finalized in October.

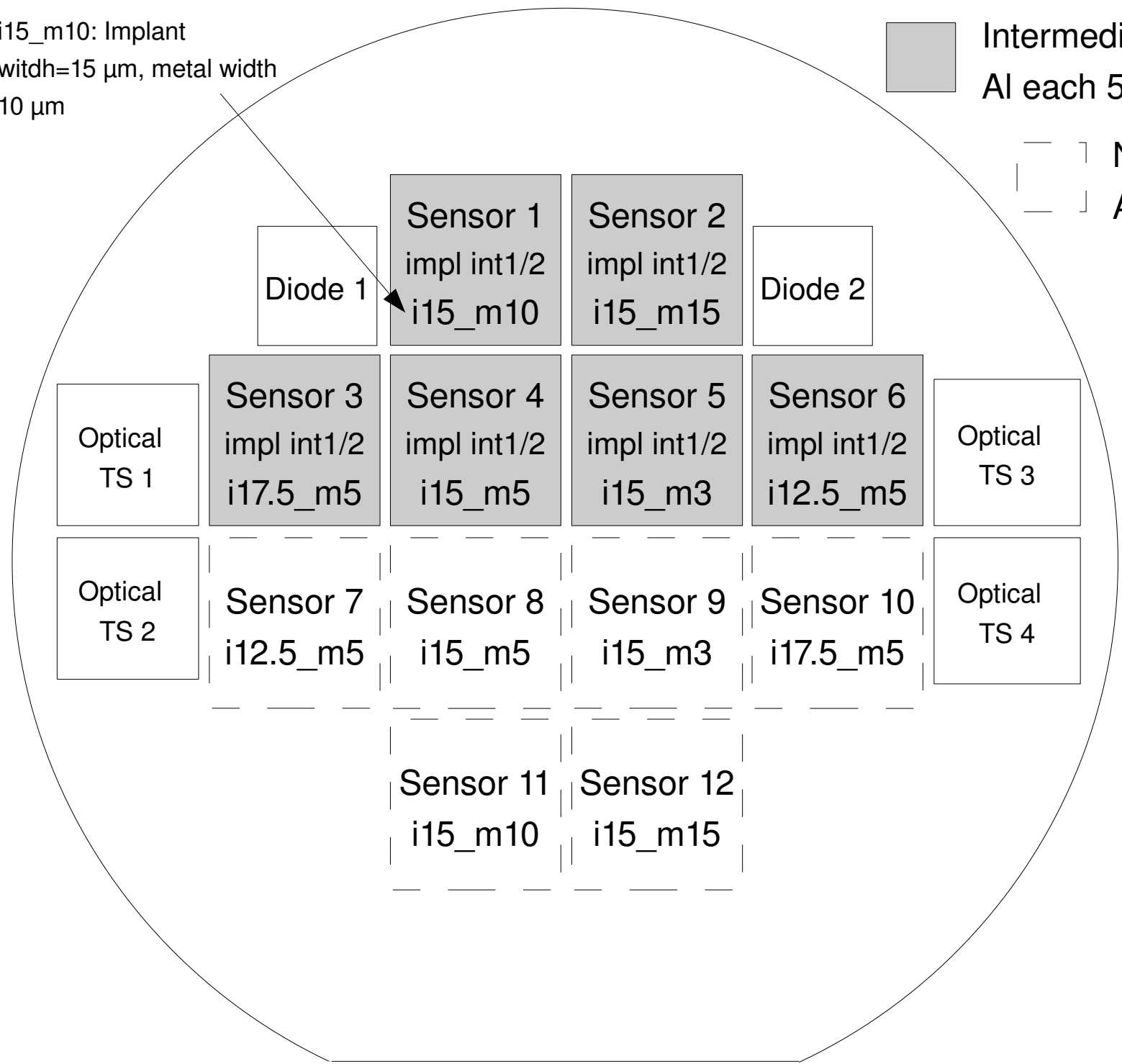
Final results of this project will be reported in the EUDET annual memo

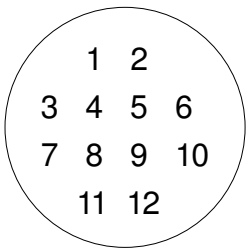
BACKUPS

i15_m10: Implant
width=15 μm, metal width
10 μm

Intermediate implant each 25 μm
Al each 50 μm

No Intermediate implant
Al each 50 μm

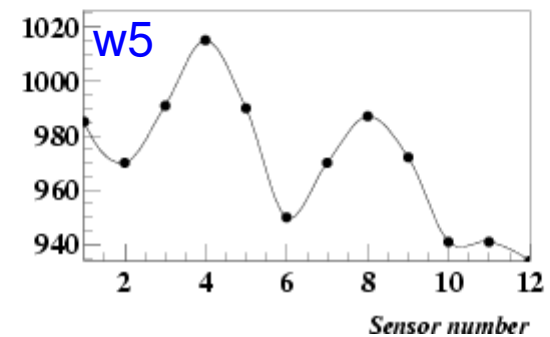
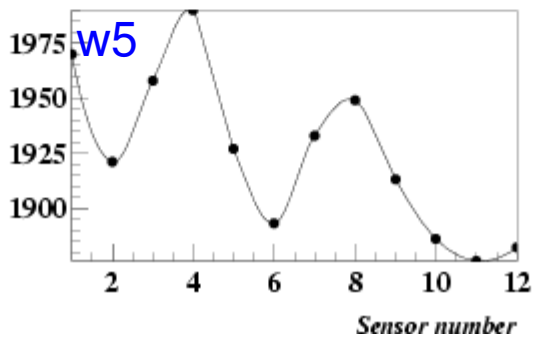
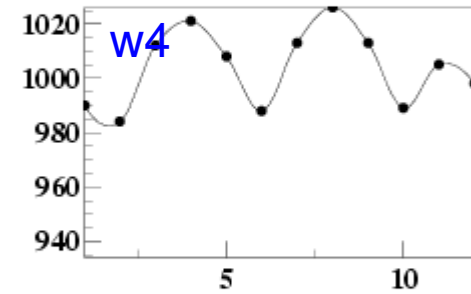
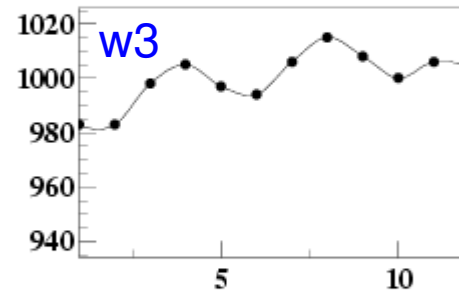
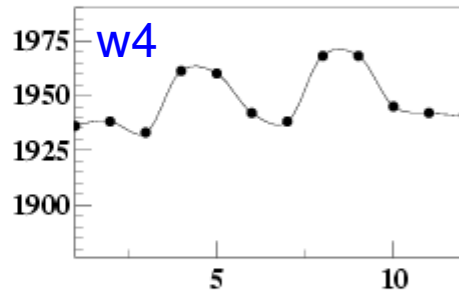
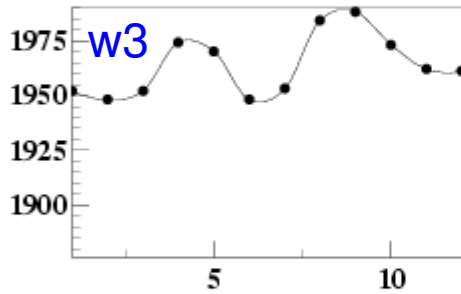
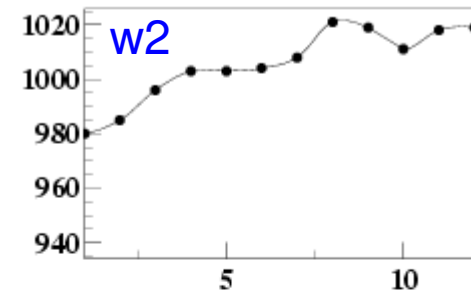
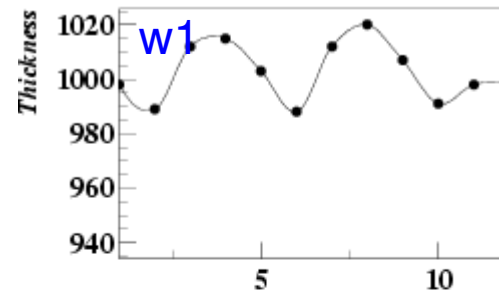
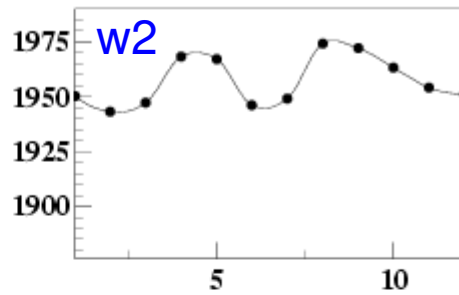
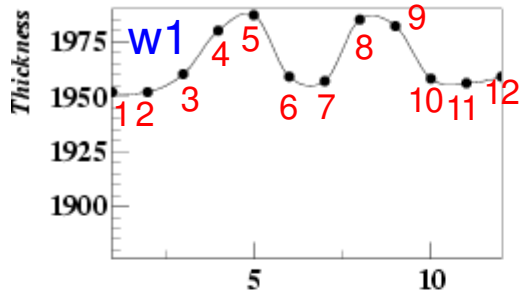




SiO2 thickness in each wafer (curves are interpolated)

Wafers 1-5, top SiO2 thickness

Wafers 1-5, bottom SiO2 thickness



Spread in wafers:

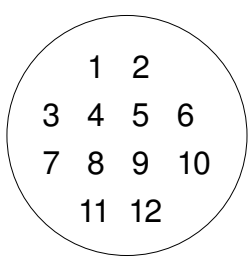
top: 1-4 < 1%, wafers 5,6 < 2%

bottom: 1-4 < 2% wafers 5 = 3%

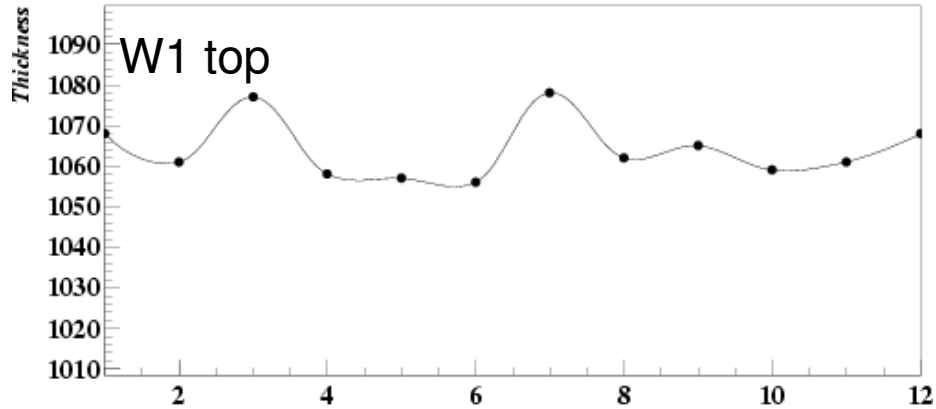
Thickness oscillations of wafer #5 are wider, both top and bottom thickness

Measurements compatible with thicker wafers in the middle, decreasing towards the border: mountain-like profile

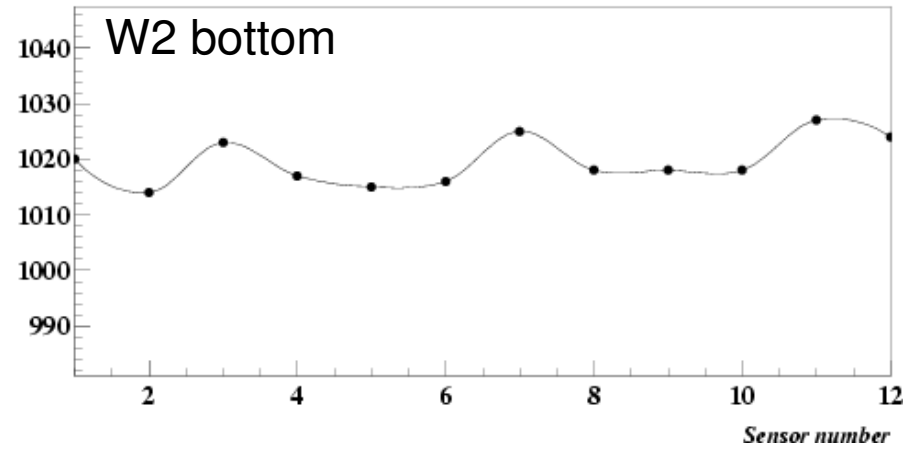
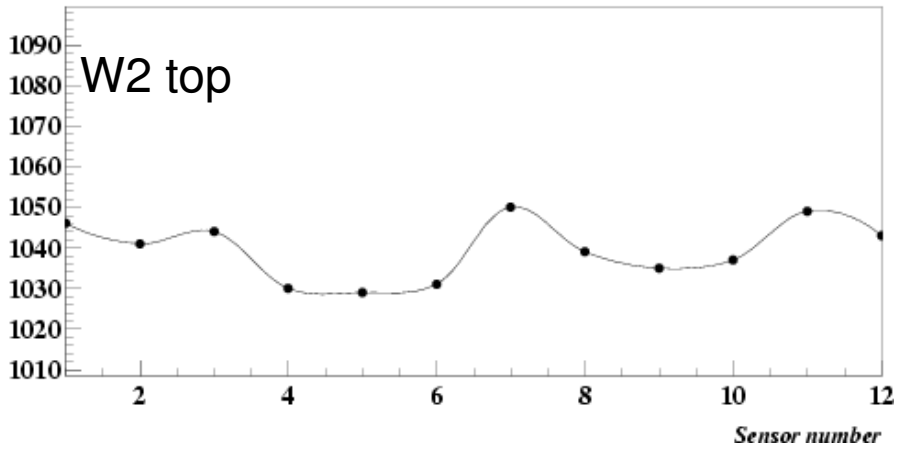
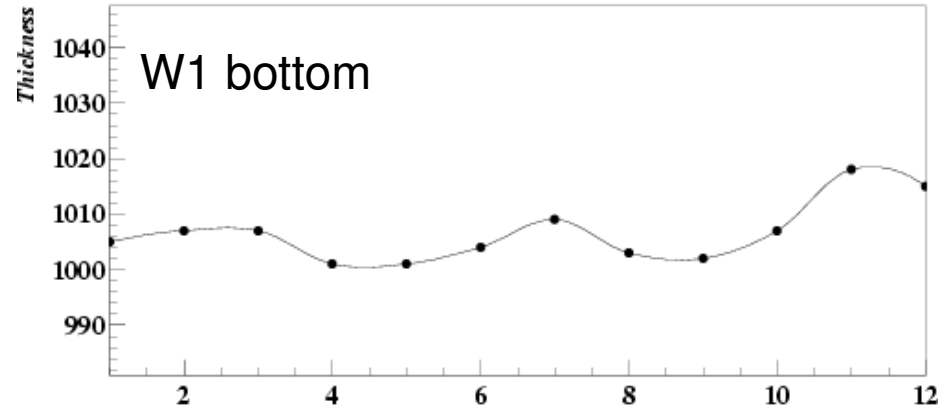
Top and bottom Si3N4



Wafers 1-2, top Si3N4 thickness



Wafers 1-2, bottom SiO2 thickness



Spread < 2%

Measured Gate and Field Oxide

Wafer	Gate Oxide [nm]	Field Oxide [nm]
1	49.5 ± 1.2	1002.7 ± 1.4
2	43.8 ± 1.3	996.5 ± 1.1
3	49.2 ± 1.0	1002.5 ± 1.5
4	49.0 ± 0.7	1002.6 ± 0.4
5	49.0 ± 1.1	1001.3 ± 1.2
6	51.5 ± 0.9	1001.8 ± 0.9

5 measurements/wafer

Measured Aluminum thickness

Wafer	Aluminum [nm]
1	940 ± 37
2	995 ± 42
3	929 ± 39
4	971 ± 36
5	965 ± 46
6	961 ± 41

5 measurements/wafer