SiTRA multipurpose and standalone test infrastructure

EUDET Meeting

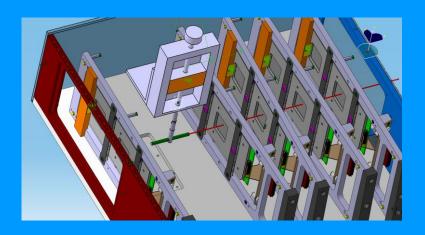
September 29, 2010,
Jacques David
On behalf of the LPNHE-LC team

Test beam Infrastructure

- Major deliverable for EUDET
- Several versions have been developed
- A new version was developed in 2009 and used since May 2010. It is multipurpose & standalone, i.e. includes
 - => a mechanical infrastructure with Faraday cage, cooling, alignment (including IR laser system), the possibility to host its own telescope system and several layers of Si modules.
 - => a dedicated DAQ hardware and software system easy to interface to any other DAQ was developed based on VHDL + C++ & ROOT for the software and a DAQ hardware that is adapted for the reference FE readout (VA1') or the new developed SiTR_130 chips.
- It multipurpose as it can be adapted to test any type of new sensors and/or FE readout chip.
- It can be used in Lab test bench or at test beam

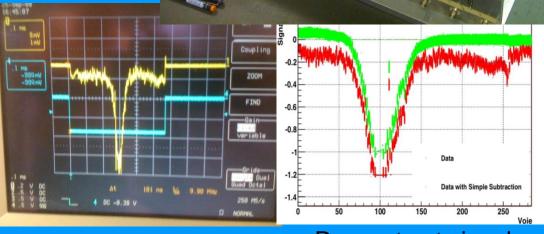
Stand-alone & portable test bench for multiple applications + associate DAQ

Ex: test of alignment system





Tests of alignment system based on AF HPK sensors



Alignement test with IR laser

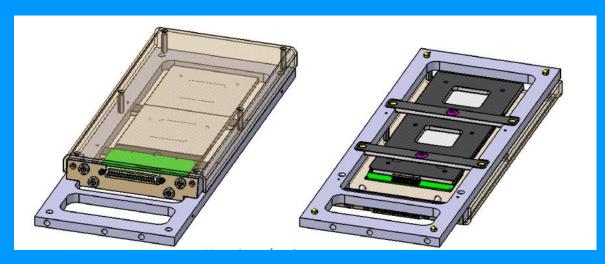
Mechanical conception of modules

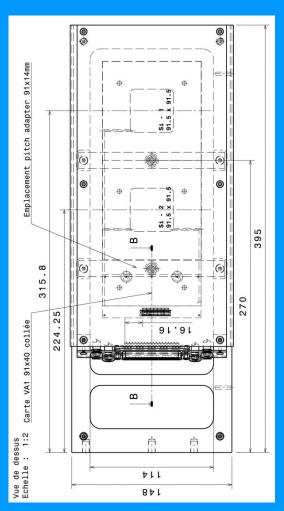
Module equipped with one or more sensors
Hybrid card (for now) ensure a kind of
flexibility for connection to front end electronics
(related to used ASIC)

Constraints linked to "bonding" between same module sensors and pitch adapter (now in CERN)

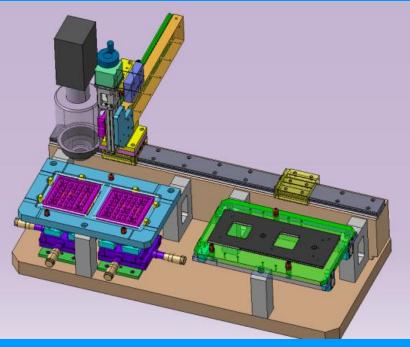
Choice of robust support structure to ease numerous manipulations when we test

Protection case for transportation or storage.





Mechanical conception of tools Modules building

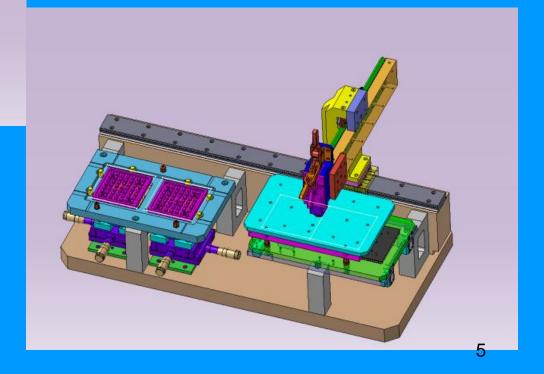


Gluing tool

Preservation of alignment Integration of sensors on Carbone support

Alignment tool

Precision alignment between different parts of module: Silicium sensors, pitch adapter, front-end electronics

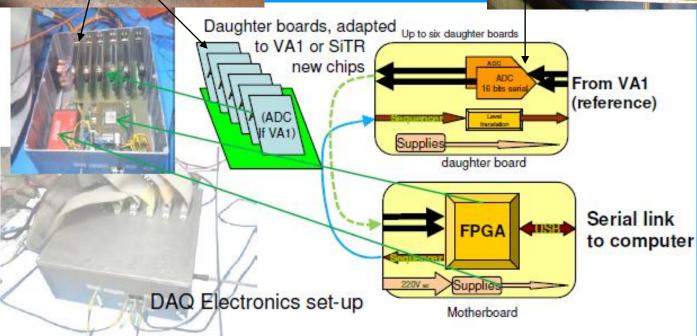


Standalone TB infrastructure: FE & DAQ Electronics



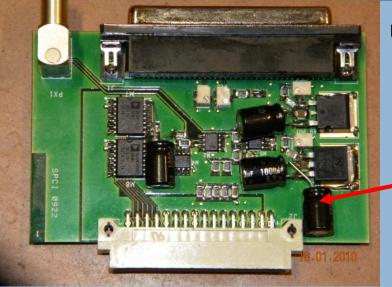
VA1' ASIC used as reference devices





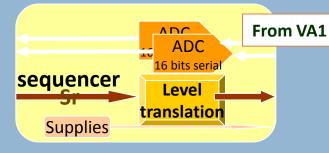
DAQ Software
VHDL & ROOT
C++ based
Easy to combine
to any other
DAQ system



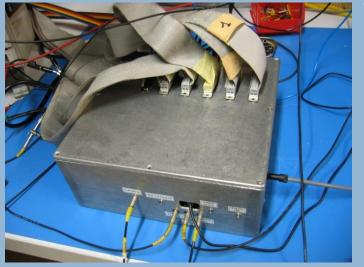


Up to 6 daughter boards for VA1'

ADC







A new DAQ electronics for VA1' readout only

Only one USB link for the whole box

Under development
USB TCP II

26-February-2010 2010 SPS Fixed Target Programme

Version 1.0

Colour code: green = SPS-exp; purple = LHC-exp; dark blue = Outside exp; yellow = not allocatable or Machine Development

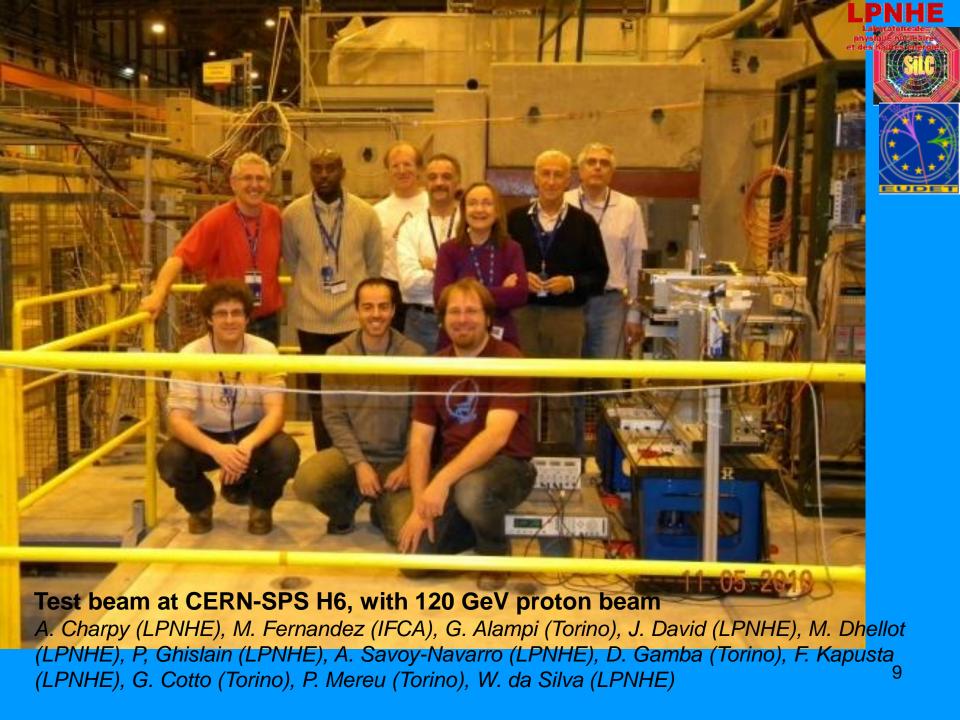
	P1	P2	P3	P4	P5	P8	
	35 29 Apr	35 3 Jun	35 8 Jul	35 12 Aug	35 16 Sep	32 21 Oct	
	3 Jun	8 Jul	12 Aug	16 Sep	21 Oct	22 Nov	
T2 -H2	NA NA61 TR 3 14 10	CMS CMS CMS PIX CALO HOLLES	CMS NA81	NA81 35		CMS AUCUSON SIBT 7 4 7 4 10 7	
T2 -H4	NA CMS LHCf NA83	PHOTAG CALICE RD51 MMEGAS 7	GRPC ECAL 11 10 14	RD51	CALET CMS RD51	PEBS NUMBER ALICE CMS WHATER SPD ECAL 4 7 7 7 7 7	
T4 -H6	3 7 8 6 3	**************************************	CERF custo MMEGAS PIX PIX 3	Diamond ALFA PEBS 11	SILC MAGGAS EUDET PIX 4 7 14 10	PIX IBL 7 7	
T4 -H8	TOTEM LHCb	HATOTEM UAQ SOURCE AND MOTIVE 10	DREAM ATLAS MDTMPI 4 14 14 3	4 10 11 10	UA9 TOTEM 3DSi 18 7 10	ATLAS ATLAS STGC MDTROM 4 14 14	
T4 -P0	3 24	35	35	35	35	32	
T6 -M2	COMPASS 3 24	COMPASS 35	COMPASS 35	COMPASS 35	COMPASS 35	COMPASS 32	
CNGS	6 29	CNGS 35	CN <mark>GS</mark> 35	CN <mark>GS</mark> 35	CNGS 35	CNGS 32	

SPS/PS-Coordinator: Horst Breuker

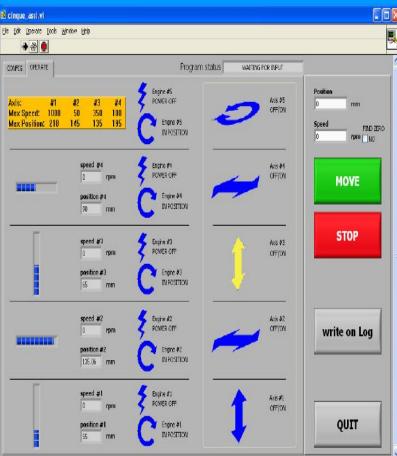
E-mail: SPS.Coordinator@cern.ch

phone: 73777 (ext. +41 22 767 3777) mobile: 164212 (ext. +41 76 487 4212) Comments:

- no comments



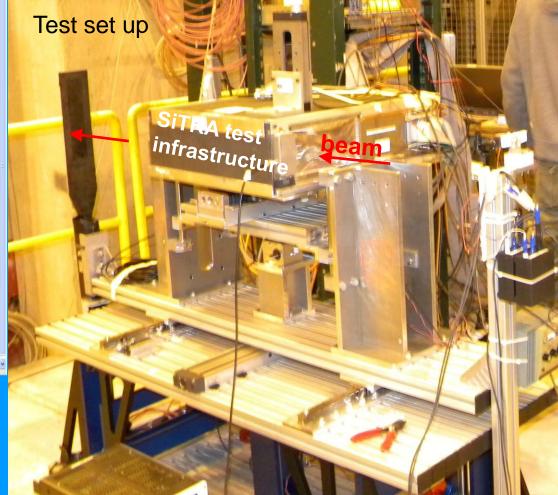
3D Table (Torino)



LabView based GUI allowing the adjustement of 4 movements available with this 4D Table

- 5 motorized & controlled movements:4 linear+1 rotation
 2 movements for positioning test bench; 3 for a 3D scan of the DUT
- Main feature: highly precise position repeatability: with Linear mvt □ 0.1mm and rot □ 0.01 degree (tested by TB)

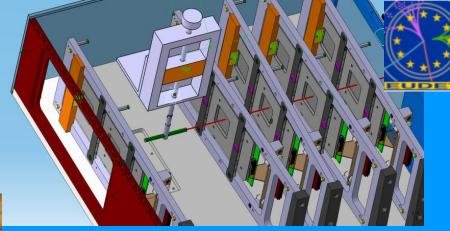
- Control & monitor via serial line by LabView and through Ethernet to DAQ thus recording DUT positions/each run.





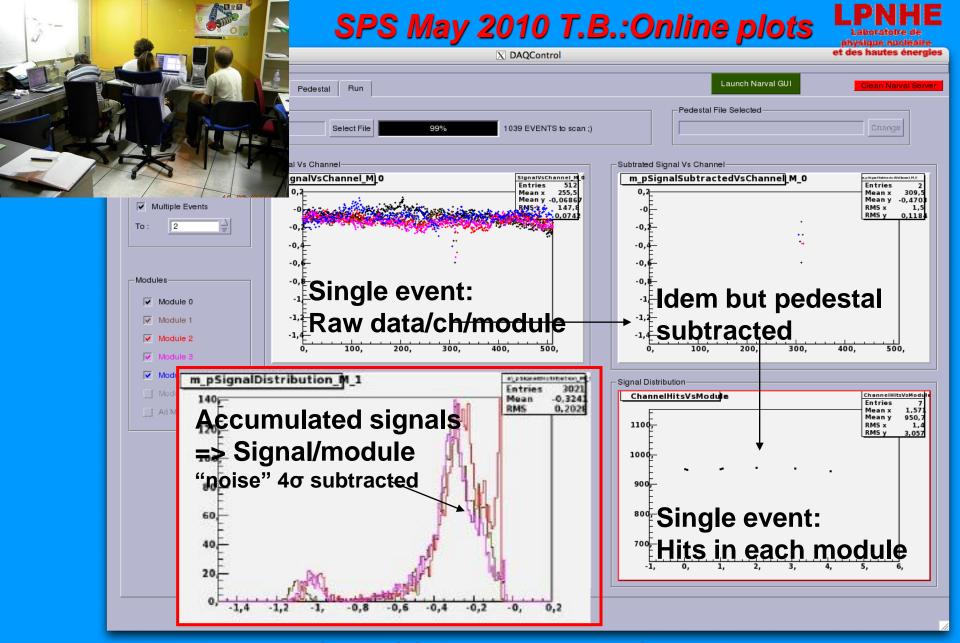
Standalone T.B. infrastructure







Test in May 2010 at SPS-CERN (alignment sensors and New 3D Table made by Torino



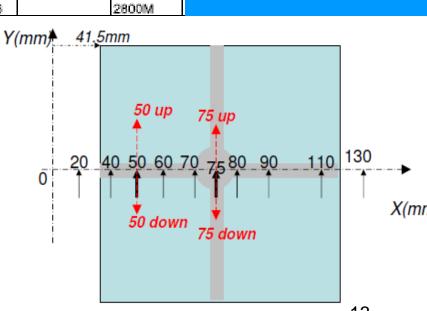
An online system (NARVAL, C++, ROOT) developed by A. Charpy works during May Tests. It is the system used also at Lab test bench for tests with system

run	jour	heure	Moteur 1	Moteur 2	Moteur 3	Moteur 4	nb evt
Run 1.txt	Thu 13 May 10	19:36	55	102	55	60	5088
Run 2.txt	Thu 13 May 10	21:17	55	102	50	60	2004
Run 3.txt	Thu 13 May 10	22:04	55	102	45	60	annuk
Run_4.txt	Thu 13 May 10	22:17	55	102	40	60	
	Thu 13 May 10	22:52	55	102	40	60	
Run_5.txt	Thu 13 May 10	23:45	55	135	40	60	
Run 6.txt	Thu 13 May 10	7	55	135	variable	60	
Run 7.txt	Thu 13 May 10	?	55	135	70	60	
Run_8.txt	Thu 13 May 10	7	55	135	70	60	60000 (
Run_9.txt	Fri 14 May 10	08:46	55	135	70	80	1039
Run_10.txt	Fri 14 May 10	09:10	55	135	70	100	1034
Run 11.txt	Fri 14 May 10	09:25	55	135	70	120	1047
Run 12.txt	Fri 14 May 10	09:44	55	135	70	130	1025
Run 13.txt	Fri 14 May 10	10:04	55	135	70	20	961
Run_14.txt	Frl 14 May 10	10:18	55	135	70	30	1013
Run_15.txt	Fri 14 May 10	10:50	55	135	70	50	
Run_16.txt	Fri 14 May 10	16:50	55	135	70	60	
Run 17.txt	Fri 14 May 10	16:55	55	135	70	70	
Run 18.txt	Fri 14 May 10	20:13	55	135	70	80	
Run_19.txt	Fri 14 May 10	23:30	55	135	70	75	57406
Run_20.txt	Sat 15 May 10	08:25	55	135	70	90	2004
Run_21.txt	501:15 Yay: 10	11.39	17	13.1	79	110	2003
Run 22.txt	Sat 15 May 10	16:01	55	135	65	90	1999
Run 23.txt	Sat 15 May 10	19:54	55	135	75	50	
Run 24.txt	Sun 16 May 10	00:17	55	135	65	75	
Run_25.txt	Sun 16 May 10	04:45	55	135	75	75	1999
Run_26.txt	Sun 16 May 10	09:00	55	135	70	60	



Taking Data

Scan in position of the HPK A.F. sensor



file stze

195M

89M 99M 108M

55M 62M

38M 1400M 38M 38M

38M

45M

45M

956M 791M

948M 951M

plot

Run1Plot.jpg

Run2Plot.jpg

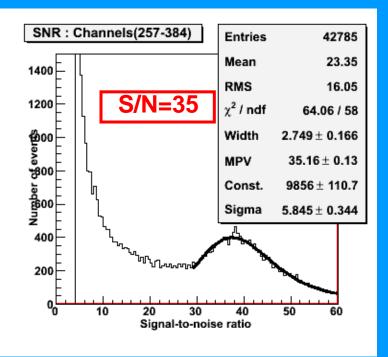
Run7Plot.jpg

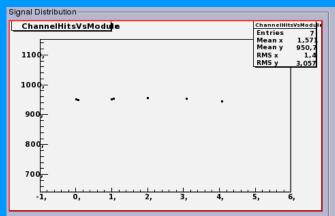
Run11Plot.jpg

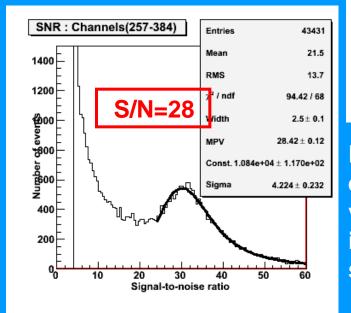
Run12Plot.jpg

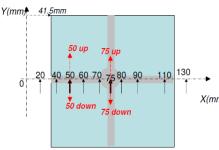
Run13Plot.jpg 42M

Data Analysis

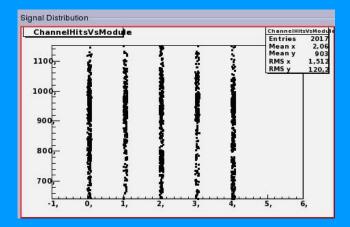








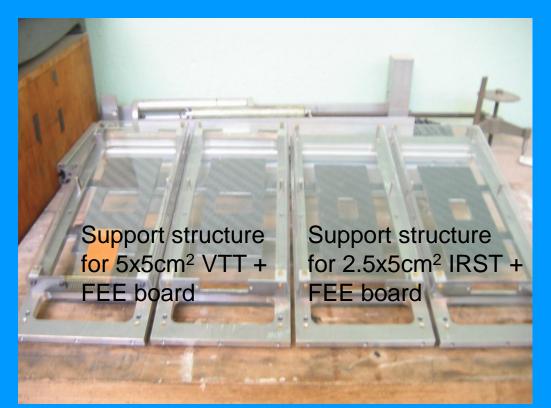
Evaluate S/N for each position and verify result is independent of scan position.



In progress: Tracks reconstruction (5 layers)



Preparing modules and FEE for tests of new sensor states of the states o



- Support structures:
 ready for the new VTT and IRST active edge sensor prototypes
- To be ready for the November test beam at SPS-CERN.
- New HPK DSSD sensors to be also tested at SPS.



New VA1' Front-end card support equipping all sensor-channels (1024 channels/sensor, 8chips; Each chip process 128 channels)

EDGELESS DETECTORS on 6" (150 mm) WAFER

Main edgeless strip detectors

- . 5 x 5 cm2
- · DC & FOXFET

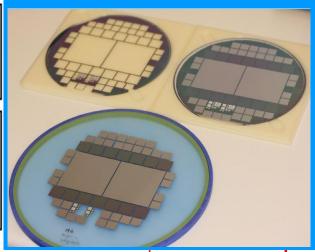
Medipix 2 edgeless pixels

- •1.4 x 1.4 cm²
- · 6 different designs

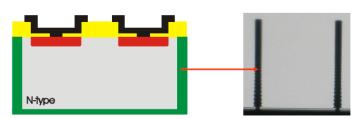
Baby edgeless strip detectors

- · 1 x 1 cm2
- · DC. PT & FOXFET
- · 24 different designs

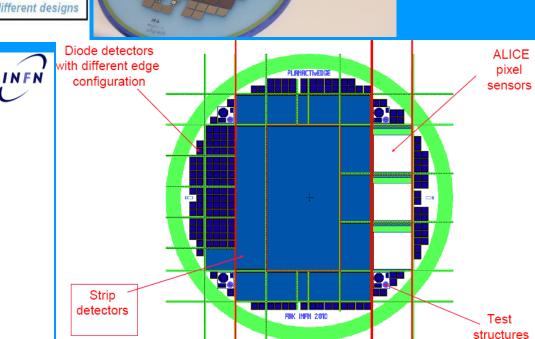
Goal in November: test of new sensor types





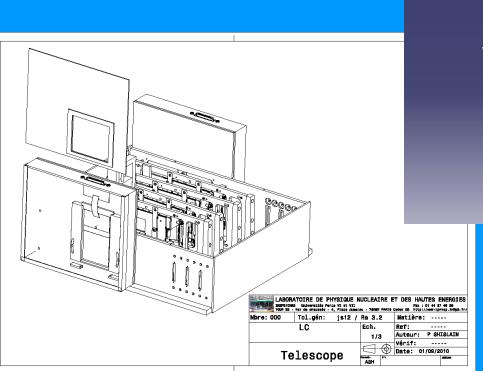


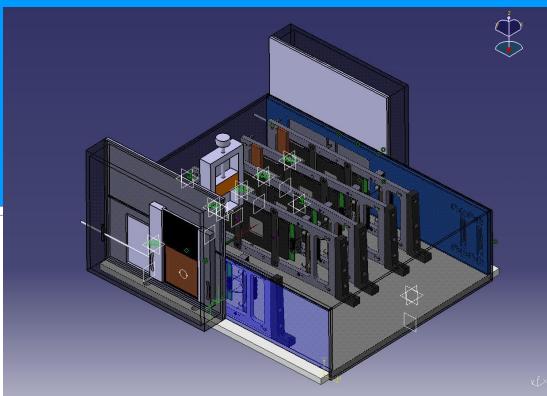
- Trench etching steps investigated on test wafers
- TCAD simulations for breakdown prediction
- Layout complete (p-on-n, mainly strips)



Modification of stand-alone test bench for November 2010 tests

Addition of a vertical strips sensor, each side i-e for the beam telescope-sensors to define a XY position (in& out)





Development of a new online system more powerful for beam tests

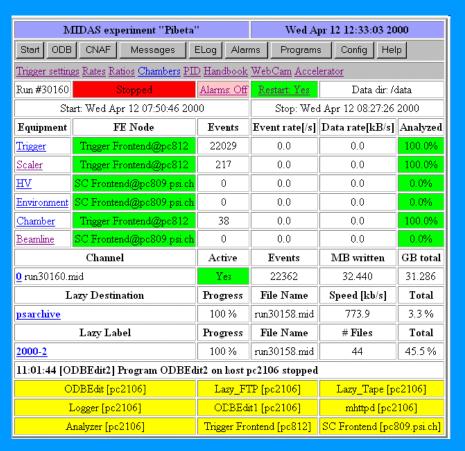
Actually based on NARVAL:

- Distributed acquisition system written in ADA
- Implement software layer of data processing.
- Divide every acquisition in two activities « Producers et Consumers » and one treatment: Filter



- •We use it for handling read data from USB card (Producer) up to disk writing(consumer).
- Pros: fast, distributed, flexible coding.
- Cons: weak docs, still need some complementary modules for user management, Slow Control & DAQ, very new.

⇒Alternative in progress based on « Midas »



- Generic acquisition system for small size & middle size experiments.
- Known for years at TRIUMF and PSI
- Easily portable for any operating system (embedded systems included)
- Include a « slow control » system, on-line database and an « history system »
- Tests in progress with this system to be used during November tests and a future embedded system.

VHDL software is slightly modified for processing data from new front-end cards in November