

VTT's EDGELESS DETECTORS FOR EUDET

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Business from technology



Outline

- Facilities and process resources
- 3D detector process
- Edgeless detector prototypes on 6" wafers
 - Wafer layout, fabrication process
 - Different designs: p-on-n and n-on-n
- Strip detector characteristics review
- N-on-n medipix2 pixel detector design & characteristics
 - IV-curves
 - First X-ray image
- Study of edgeless detector response
 - TCAD simulation
 - X-ray tube response
 - Radiation source responses
- Summary

MICRONOVA CLEANROOMS

Main Cleanroom Characteristics

Total Area m ²	2 600
Cleanroom Classification (in clean bays)	ISO 4...ISO 6 (10...1000)
Temperature	21 °C ± 0,5 °C
Relative humidity	45 % ± 5%

Clean bay - Service chase type
Ventilation based on filter fan units
Raised perforated floor
Subfab with technical support areas

Labs with built-in Cleanrooms

Micropackaging lab - dicing saws,
wire bonding

SubTech lab - Ion implantation, CMP,
backgrinder, wafer bonder

Process equipment is mainly for 150 mm
wafer size, but some processes can be
performed also on 200 mm wafers



Equipments

Furnace:

- oxidation, LTO, TEOS, Nitride, doped and undoped polysilicon
- 2 Centrotherm furnace stacks

Lithography:

- Contact aligners – MA150 and MA6 (bottom side alignment), MA200
- E-beam writing – Zeiss LEO 1560
- Step and Stamp Imprint Lithography – Suss MicroTec NPS 300
- i-line stepper, Canon FPA 2500i3
- Resist/development tracks, Suss ACS 200 and AIO Duna 700

Dry etching

- Etchers for silicon oxide, nitride, metals - LAM 4520/4420/9600
- Deep silicon etching - Aviza Omega i2L and STS ASE
- Silicon oxide ICP etching – STS AOE
- RIE – Oxford 80Plus
- Plasma strippers (PRS 800/801), microwave asher (Aura 1000), wet ozone stripping

Ion Implantation

- Medium current, 200 keV, P, As, B – Eaton NV8200-P



Equipments

Sputtering: AlSi, Mo, TiW, Si - Provac LLS 801

PECVD: Silicon oxide and nitride, incl. TEOS-process

Electroplating:

- Ni, Cu, SnAg, SnPb and SnBi – RENA and home-built plating systems

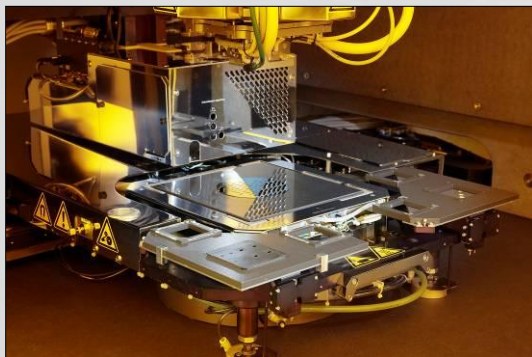
Flip-chip bonding: 2 Suss MicroTec FC150 bonders

Dicing: Disco DFD 651 and Loadpoint uAce-352

Fusion wafer bonding: EVG 5201S and EV 801 (non-IC materials)

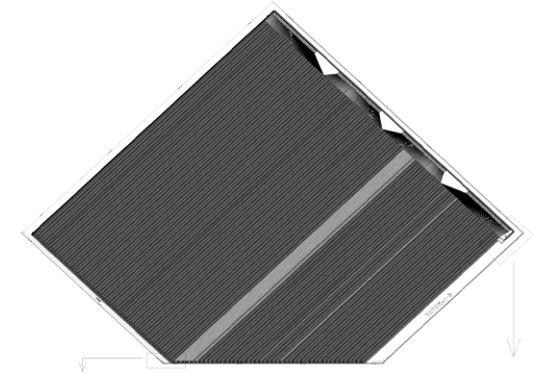
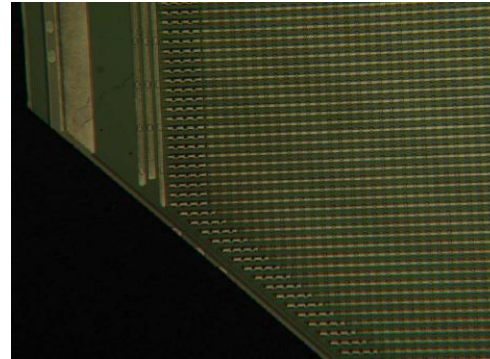
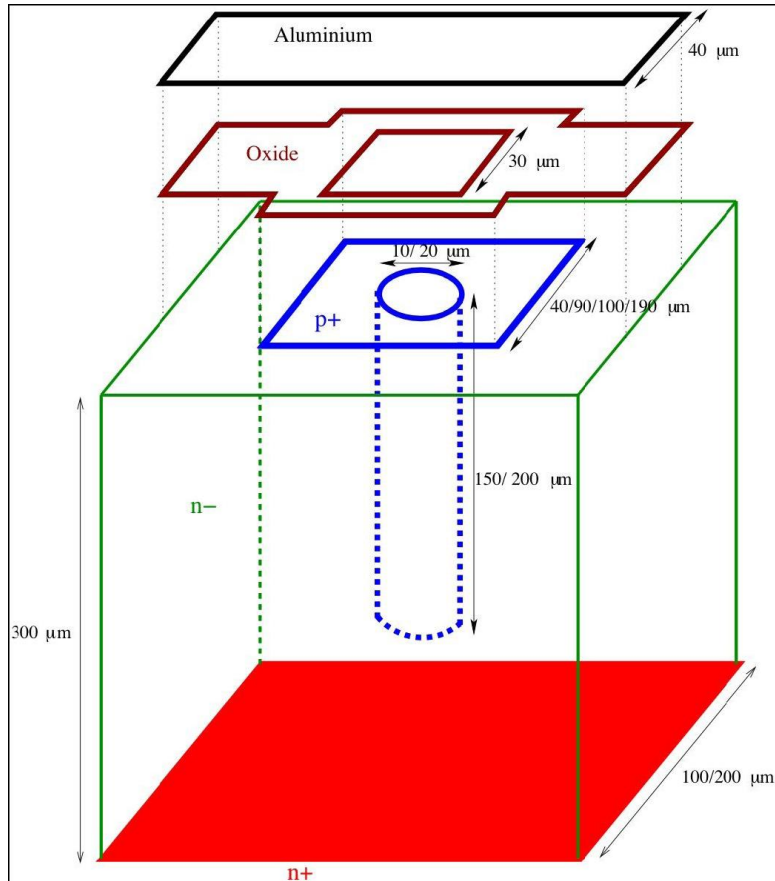
Backgrinding (wafer thinning): Strasbaugh 7AF

Polishing and planarization: Strasbaugh 6DS-SP



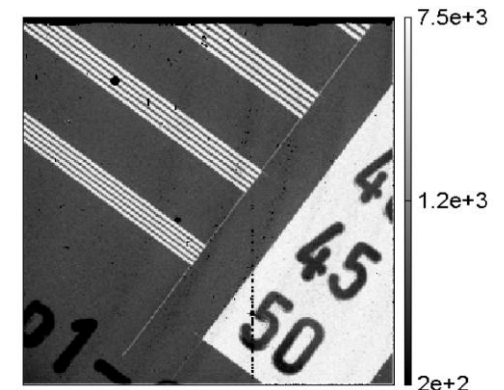
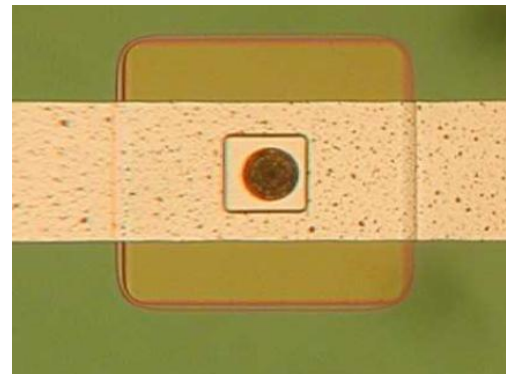
VTT's 3D DETECTORS

Pixel element of a strip detector



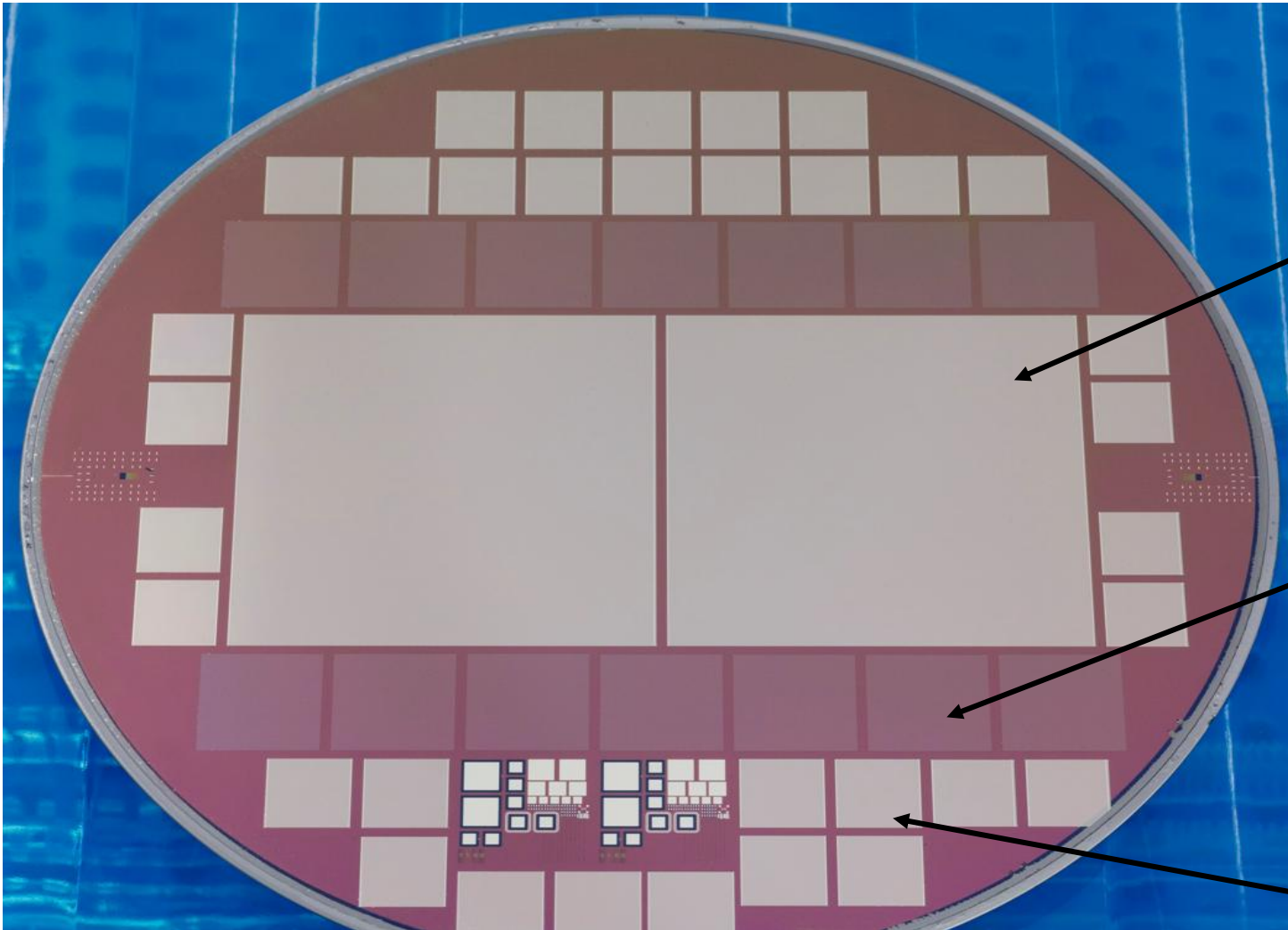
PROPERTIES

- GOOD SPATIAL RESOLUTION
- TUNABILITY OF THE VERTICAL DOPING PROFILES
- SMALL DEPLETION VOLTAGE
- LARGE AREA STRIP AND PIXEL DETECTORS DEMONSTRATED ($\sim 10 \text{ cm}^2$)
- SAME TECHNOLOGY FOR VERTICAL I/O's & EDGELESS DETECTORS



Pixel of a 3D strip detector and X-ray image taken with a 3D detector coupled to the Medipix2

EUDET EDGELESS DETECTORS on 6" (150 mm) WAFER



Main edgeless strip detectors

- $5 \times 5 \text{ cm}^2$
- DC & FOXFET
- $50 \mu\text{m}$ edge distance

Medipix 2 edgeless pixels

- $1,4 \times 1,4 \text{ cm}^2$
- 20 & $50 \mu\text{m}$ edge distance

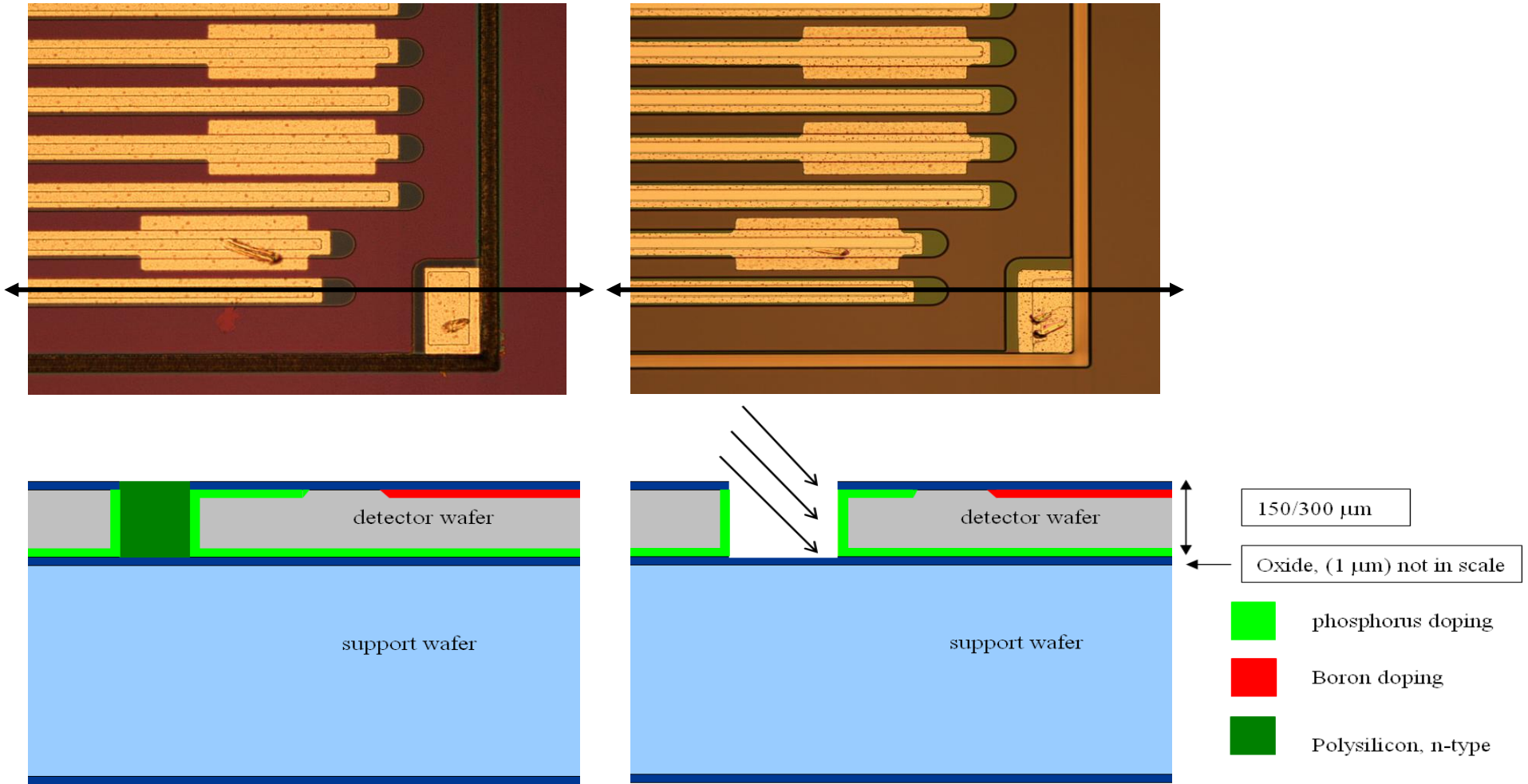
Baby edgeless strip detectors

- $1 \times 1 \text{ cm}^2$
- DC, PT & FOXFET
- 20, 50 & $100 \mu\text{m}$ edge distance

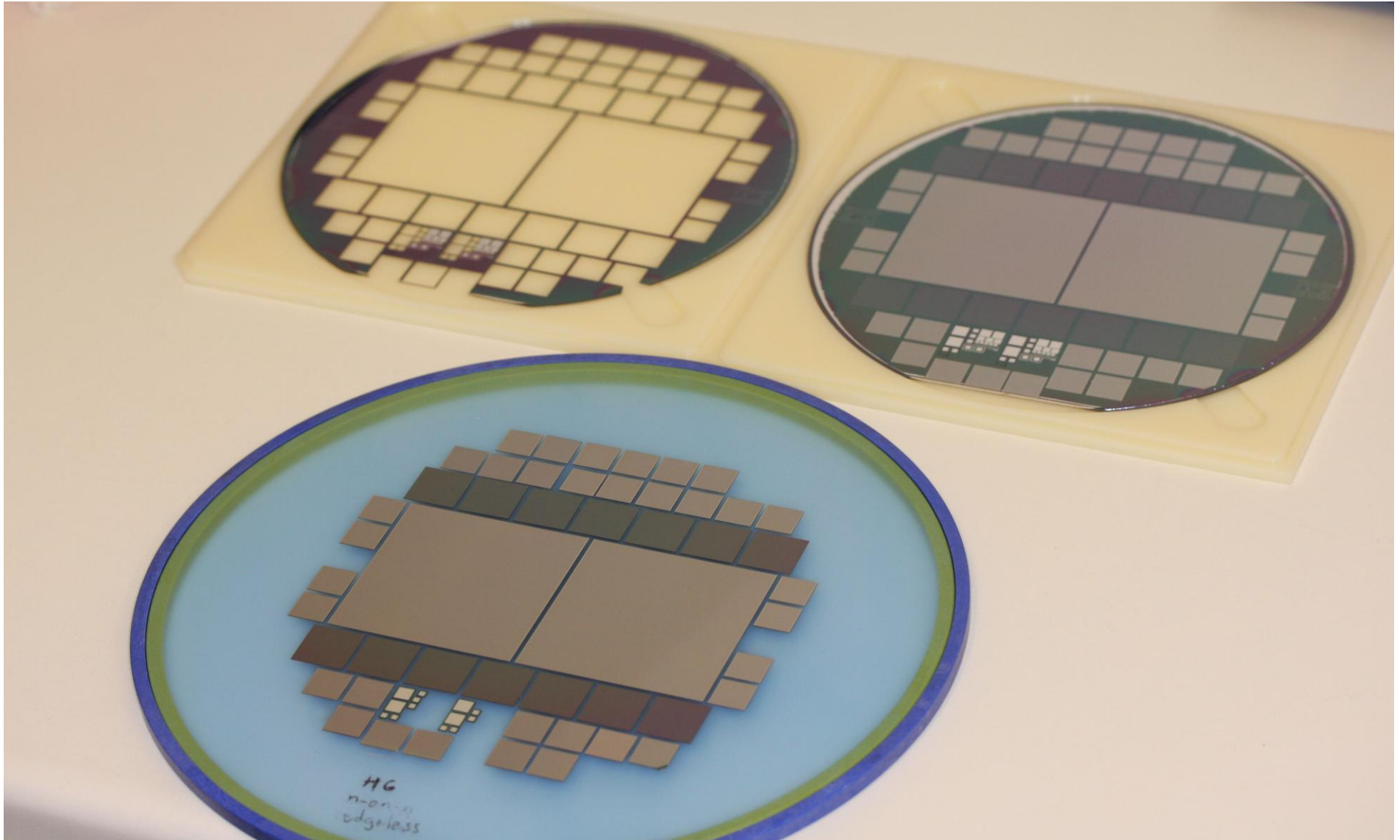
VTT's edgeless fabrication process

Poly process, p-on-n

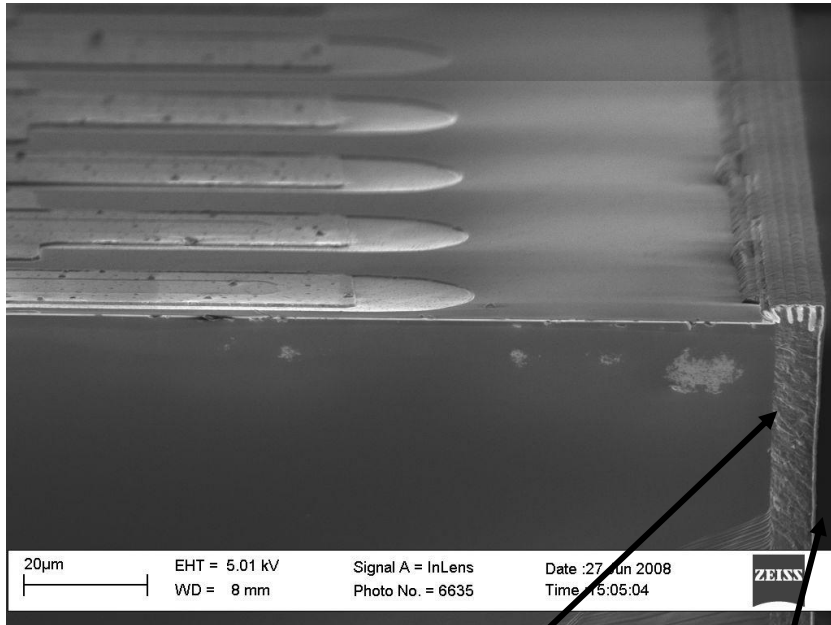
Edge implantation, p-on-n



Handle wafer removal



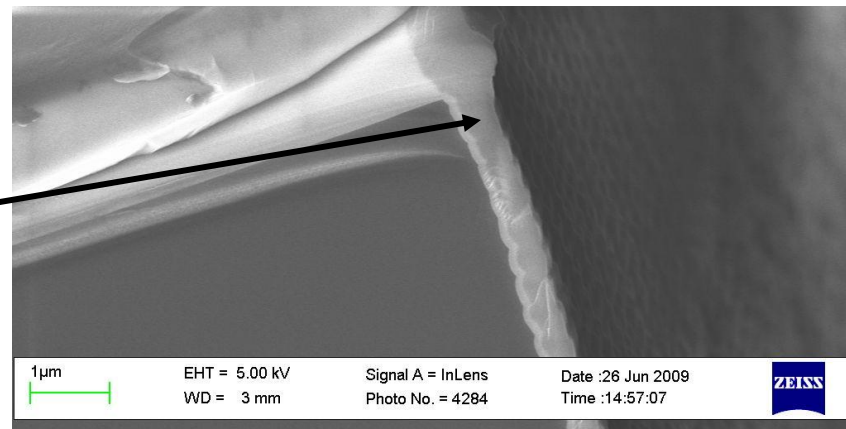
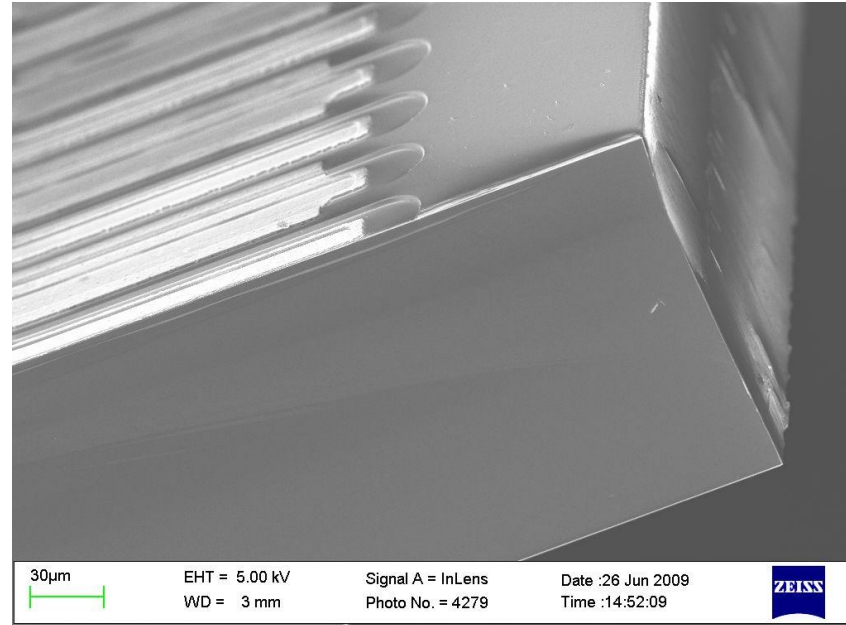
Poly process



6 µm inactive polysilicon

500 nm oxide

Edge implantation



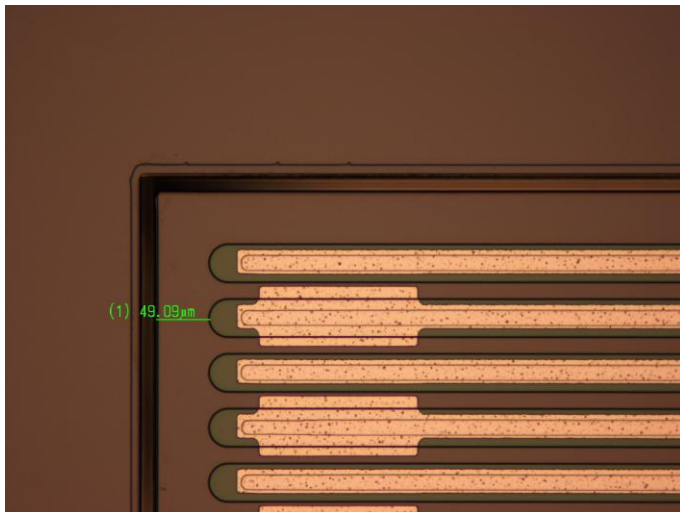
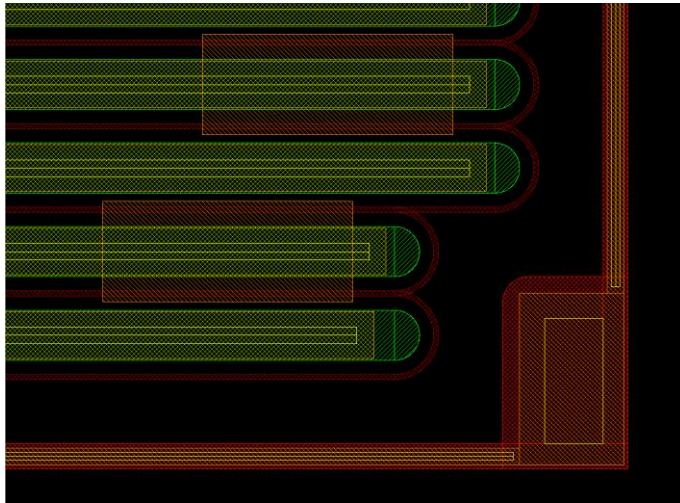
3D PROCESSING WITH POLYSILICON FILLING

- Polysilicon filling of the trenches is a slow process for the n-type active edge
 - Almost 50% of the edgeless process equipment time in furnace (diff, poly, anneal)
- Significant bowing of 6" wafers due to the polysilicon growth (~0.5 mm)
 - Difficulties in lithography, planarization and ion implantation
- Wafers brittle due to the polysilicon growth -> increased possibility of wafer cracking
- Slow planarization process required
- Detector edge cracking after the support removal
- Physical inactive edge region ~5-10 μm

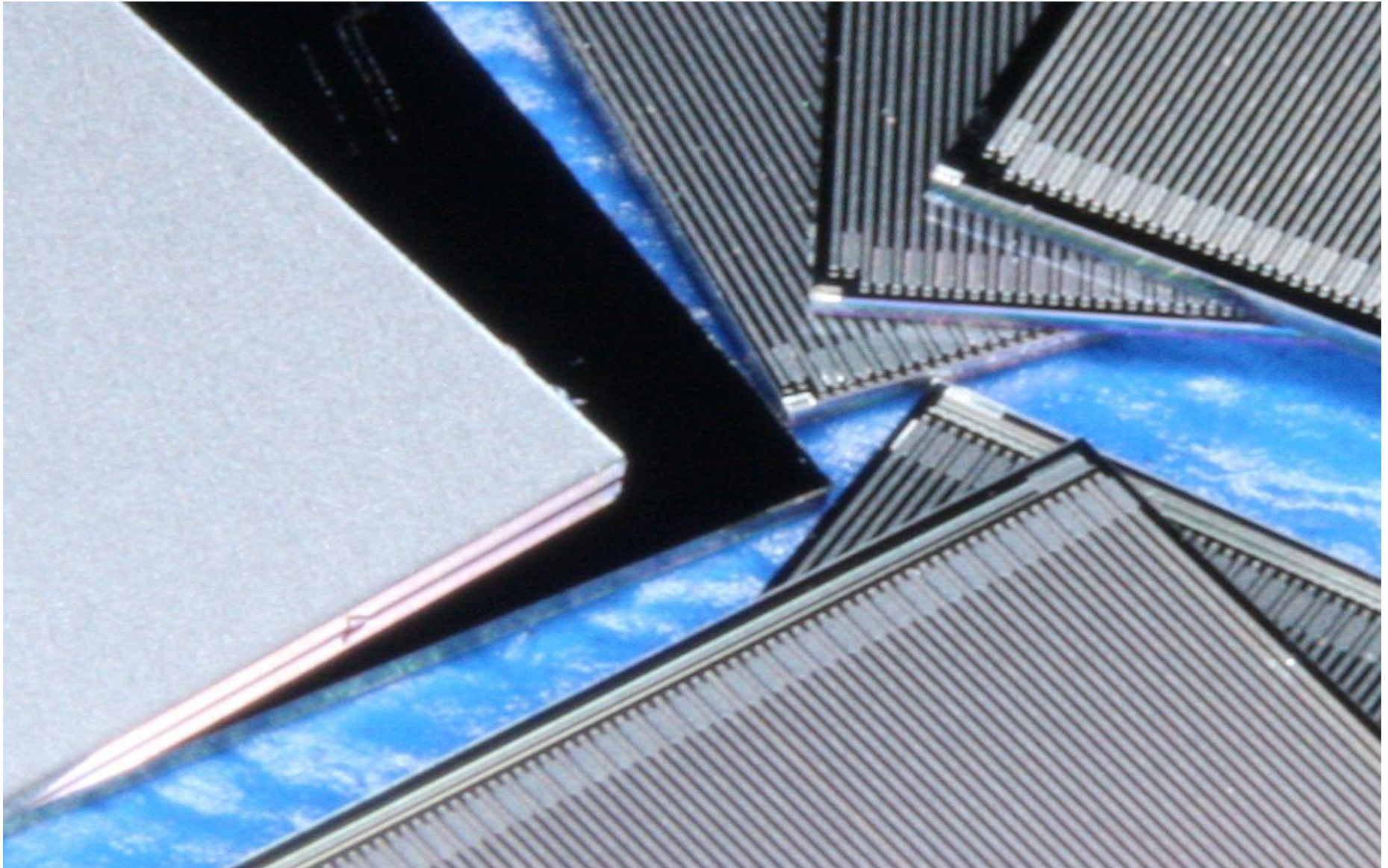
3D PROCESSING WITH ALTERNATIVE PROCESS

- No need for polysilicon filling, planarization and separate ICP dicing
- Fast process and no bowing of the wafer
- Detector edges sustain handling – no edge cracking
- Physical inactive edge region <1 μm
- Requires non-planar lithography -> readiness available at VTT

DC-coupled strip designs & n-on-n layout

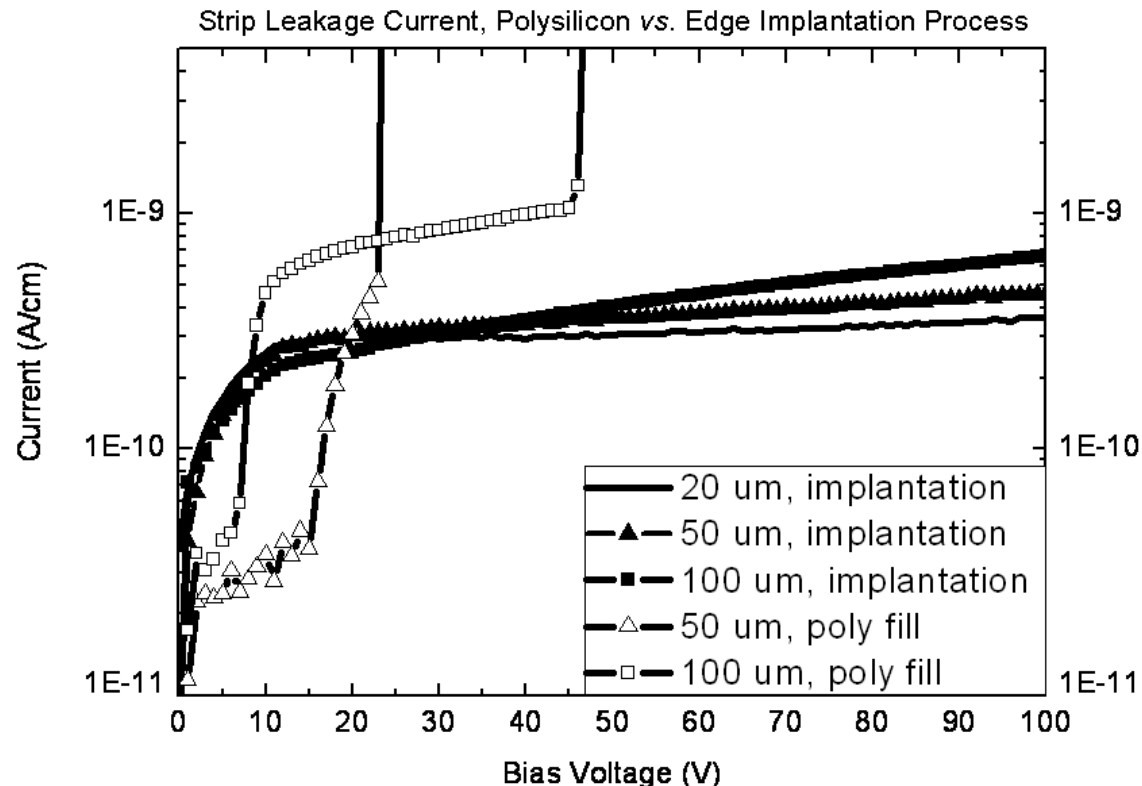


Edgeless strip detectors



Strip leakage current: p-on-n implantation vs. poly

- Low leakage currents for both process approaches
- Very early breakdown voltages for poly filling
- Leakage current depends on the active edge distance

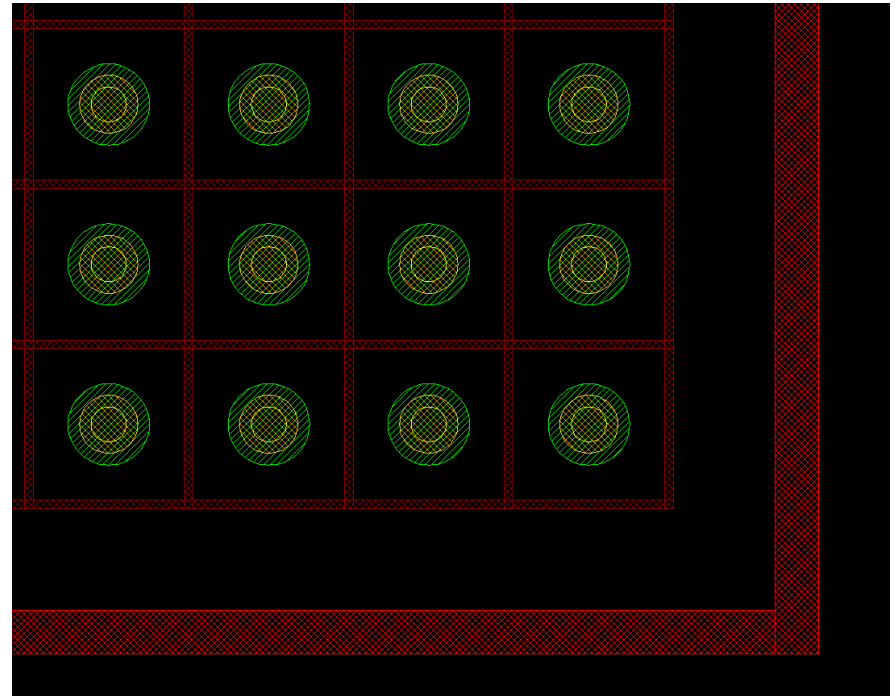
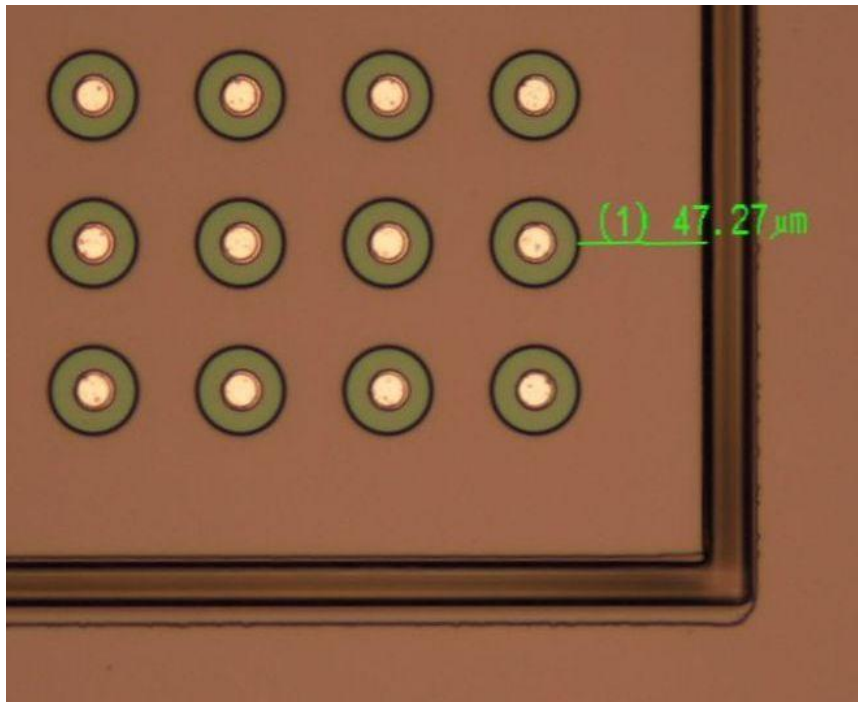


Characteristics of 150 μm thick edgeless strip detectors

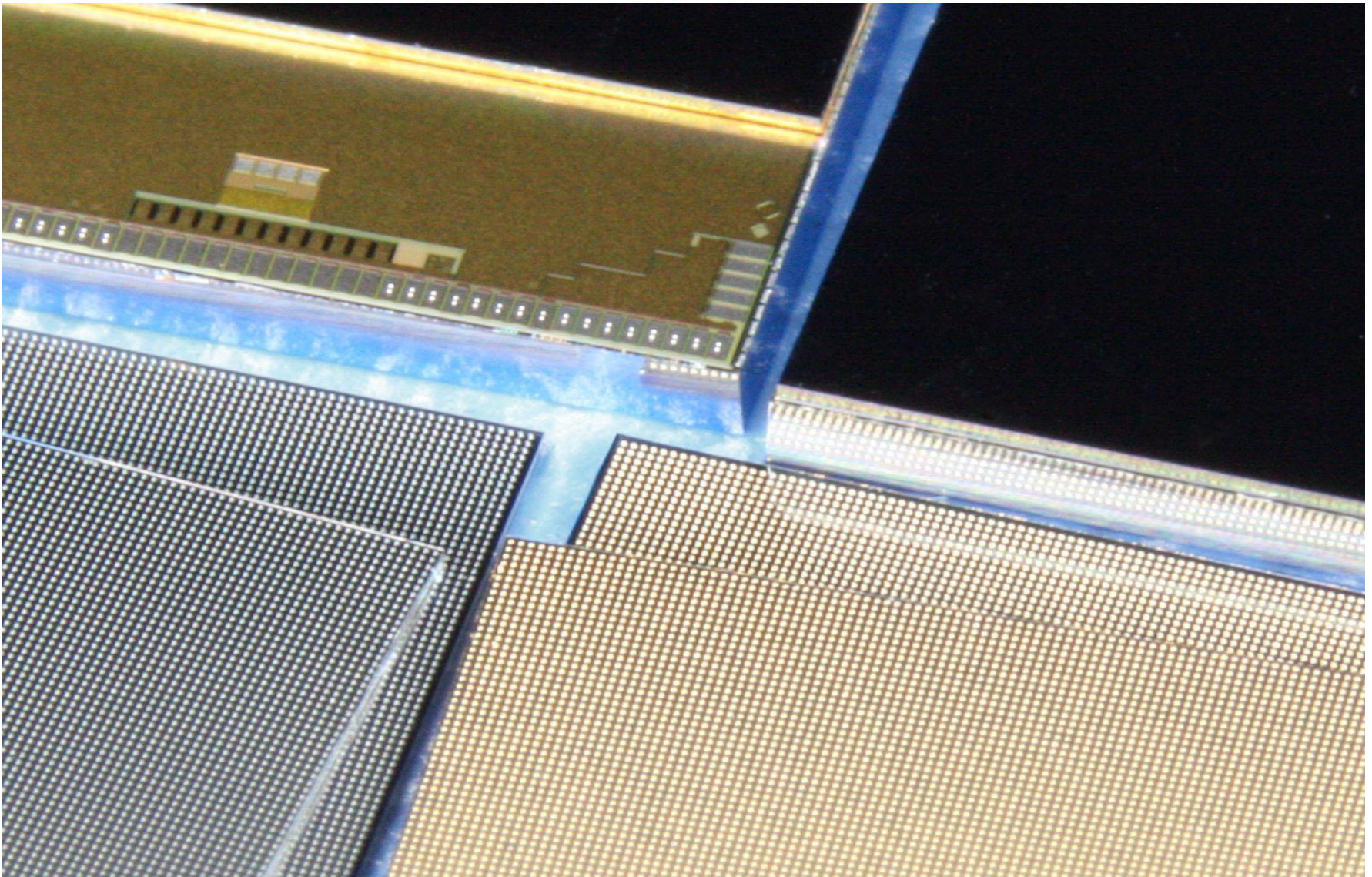
<i>Edge distance polarity</i>	<i>20 μm</i>		<i>50 μm</i>		<i>100 μm</i>	
	<i>p-on-n</i>	<i>n-on-n</i>	<i>p-on-n</i>	<i>n-on-n</i>	<i>p-on-n</i>	<i>n-on-n</i>
<i>Full depletion voltage</i>	~25 V	~13 V	~35 V	~16 V	>40 V	~25 V
<i>IV @ 40 V (nA/cm²)</i>	50-59	118	58-68	116	66-70	117
<i>CV @ 40 V (pF/cm²)</i>	580-620 705 (edge)	940-960 855	652-665 593 (edge)	930-950 800	650-655 543 (edge)	937-955 805
<i>Breakdown voltage</i>	~145 V	~75 V	~180 V	~90 V	>200 V	~95 V

Medipix2 pixel desing & n-on-n layout

- Pixel pitch of 55 μm
- Active edge distances 20 and 50 μm
- UBM service available from subcontractor
- Own line for electroless plating under development

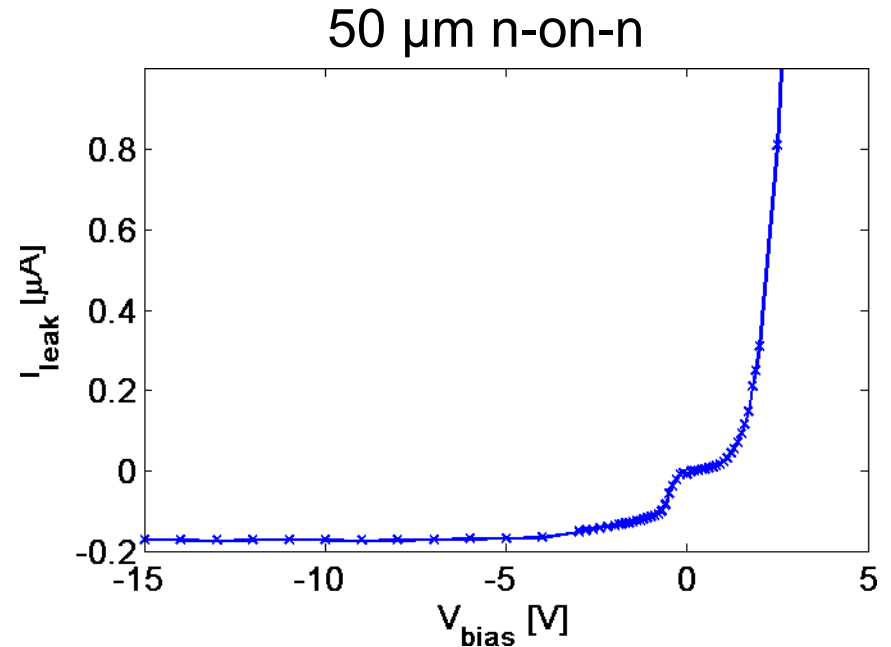
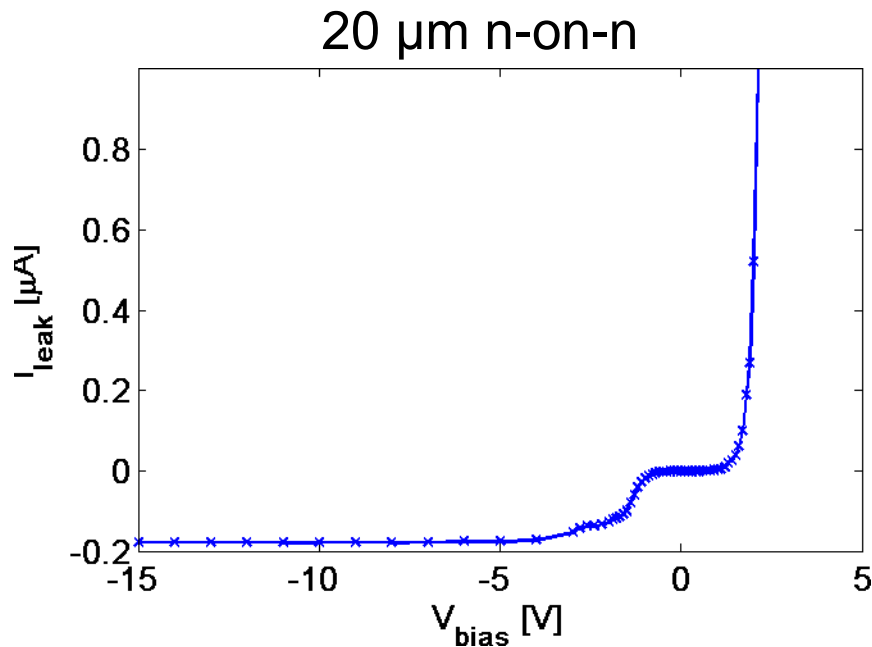


Flip-chip bonding to Medipix2

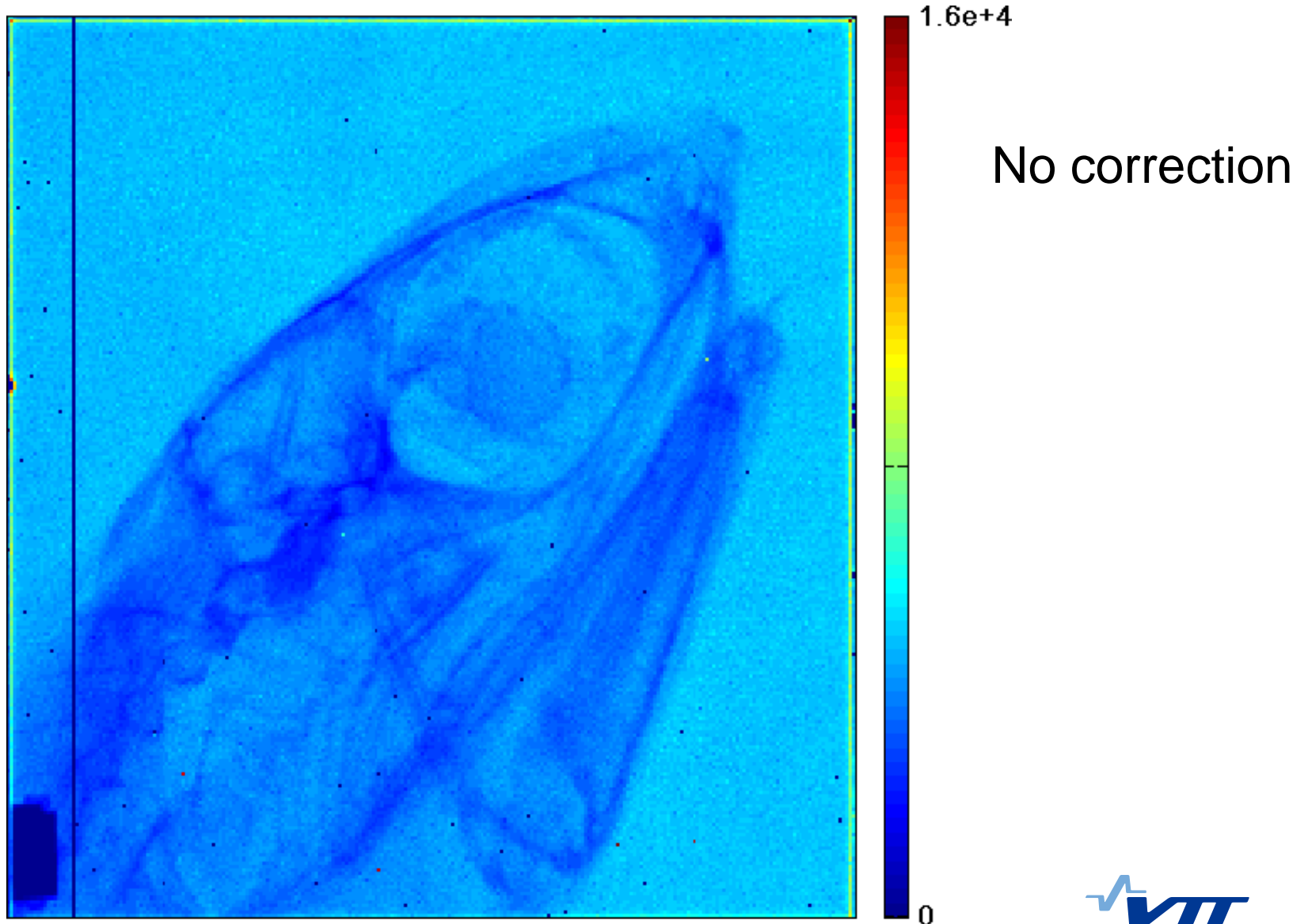


Leakage current

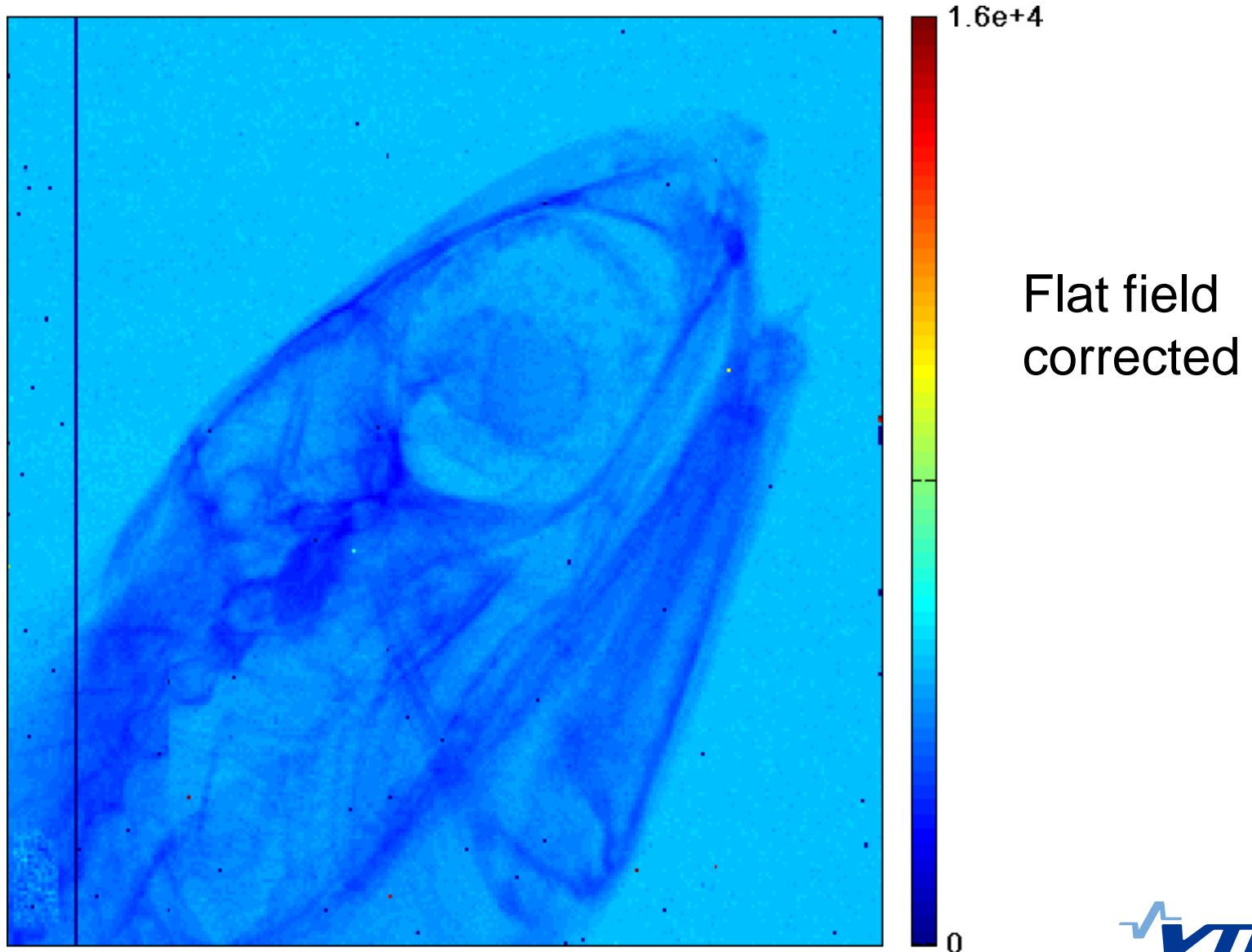
- Leakage currents of 90 nA/cm^2 and 88 nA/cm^2 for $20 \text{ }\mu\text{m}$ and $50 \text{ }\mu\text{m}$ active edge distances
- Full depletion at 5 V
- No breakdown below 70 V

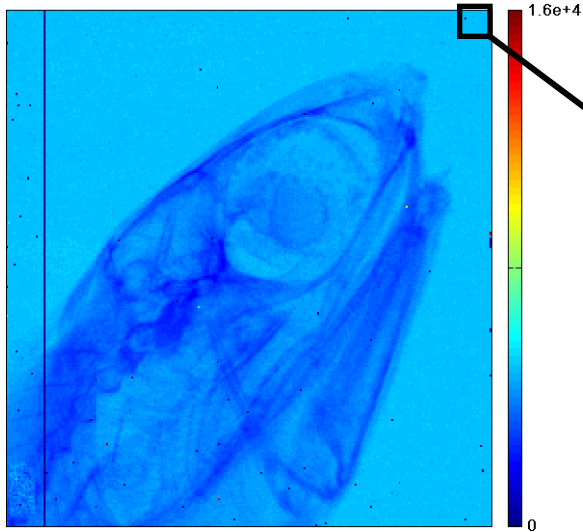


First Medipix2 X-ray images with 50 μm detector

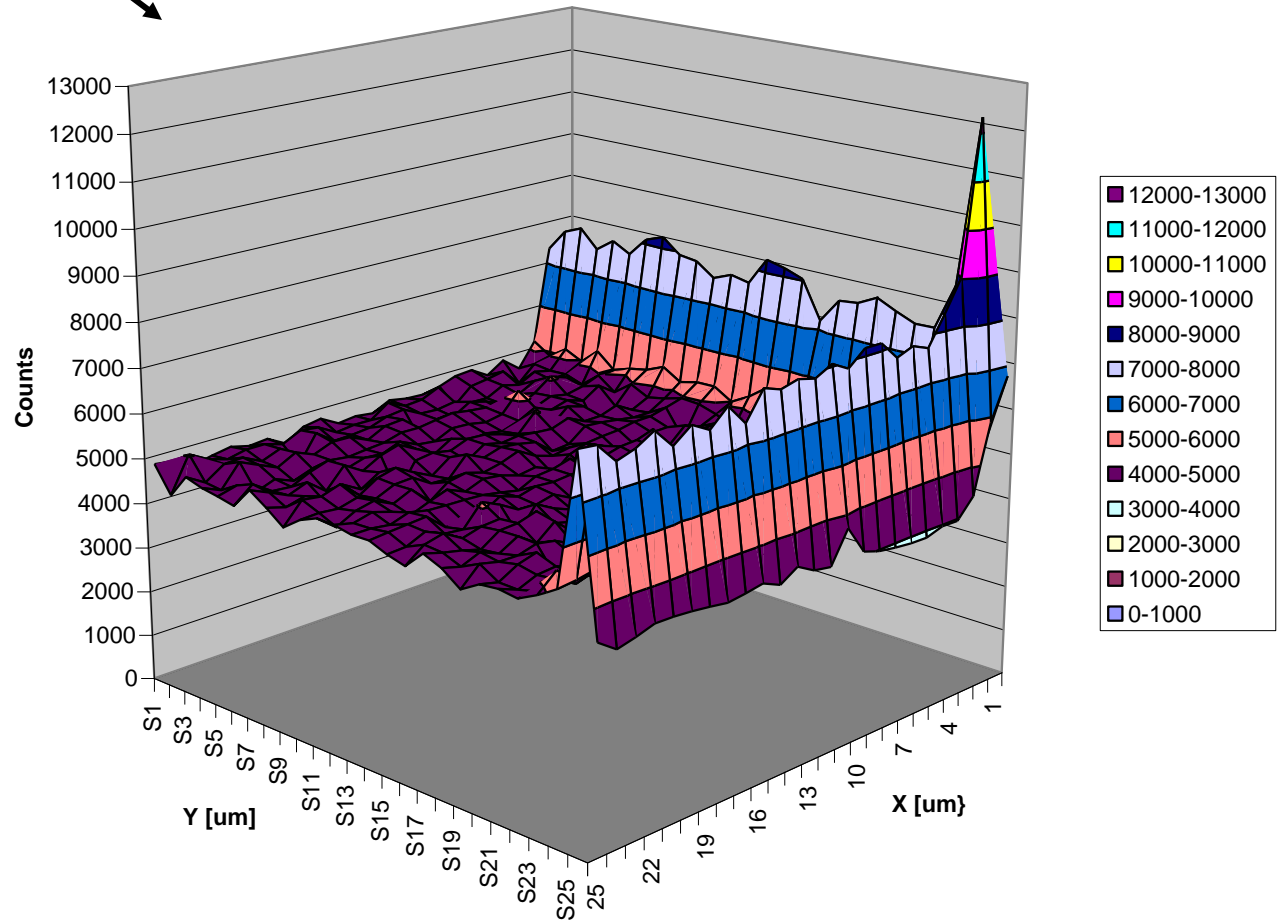


First Medipix2 X-ray images with 50 μm detector



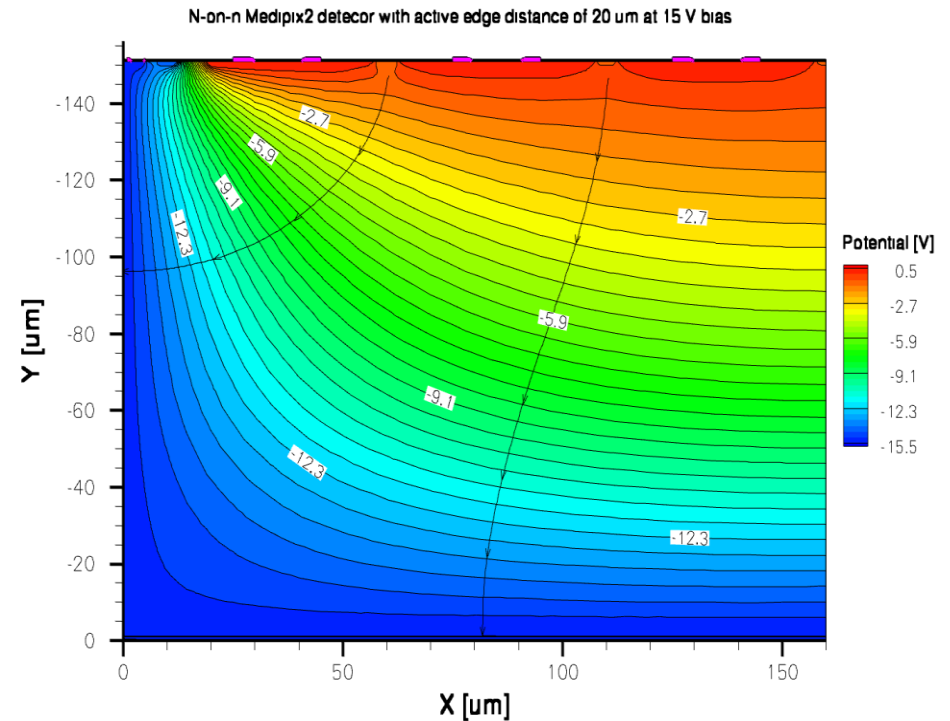
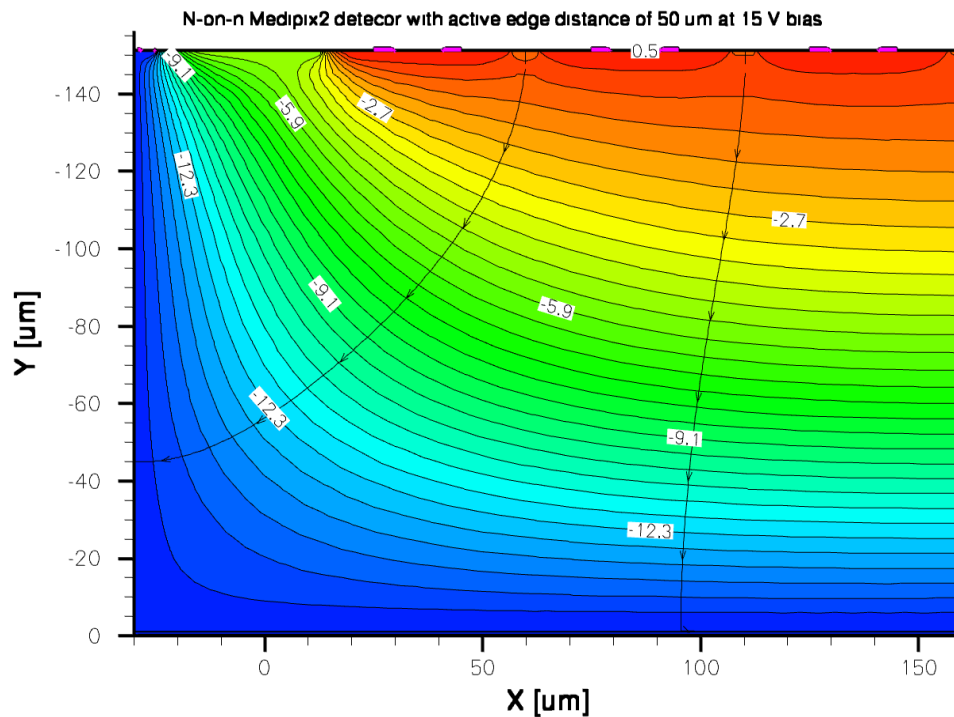


M7 (50 um) corner image, 36 s



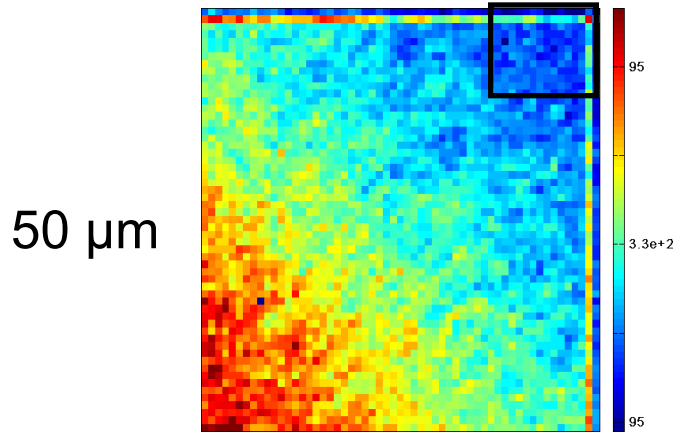
Study of edgeless detector response

- N-on-n detector at -15 V bias
- Area ratios (vs. charge collection ratio):
 - 50 μm : edge/third ~ 0.76 and second/third ~ 1.47
 - 20 μm : edge/third ~ 0.28 and second/third ~ 1.13
- Even ratios between pixels at ~ 60 μm active edge distance



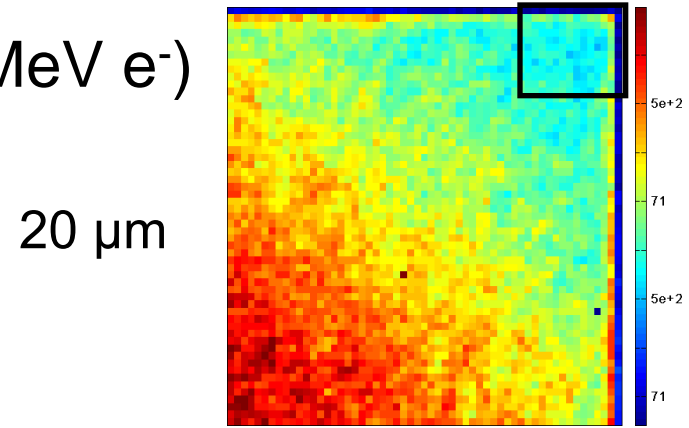
Study of edgeless detector response

- X-ray tube:
 - 30 keV, 10 mA current and 2 mm Al filtering
 - Acquisition time 606 s
- Fe55:
 - ~6 keV X-rays, less than 100 μm range in Si ($1/e \sim 30 \mu\text{m}$)
 - Acquisition time 300 s
- Cd109:
 - ~22 keV X-rays ($1/e \sim 1.3 \text{ mm}$)
 - Acquisition time 300 s
- Sr90:
 - ~560 keV electrons, 200 μm range in Si
 - Acquisition time 120 s

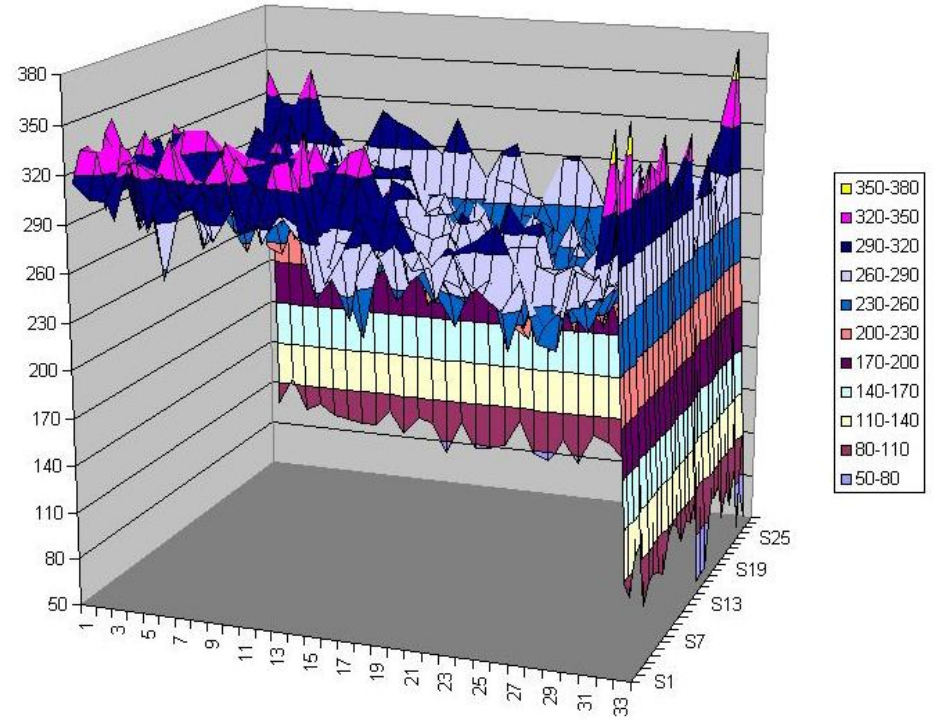
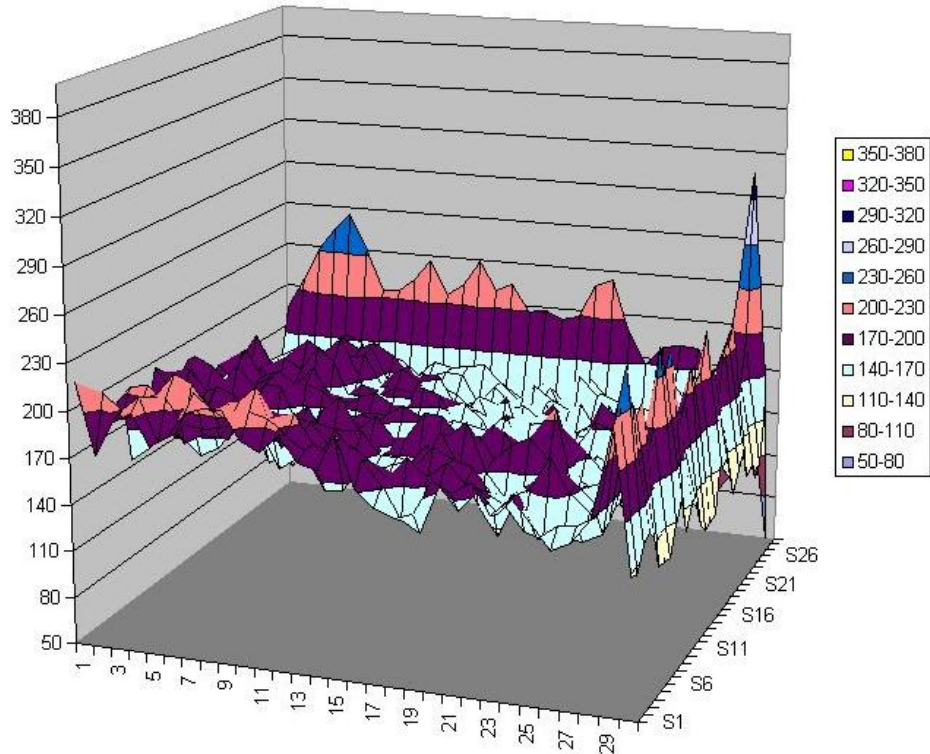


M7 detector corner response to Sr90 (e-)

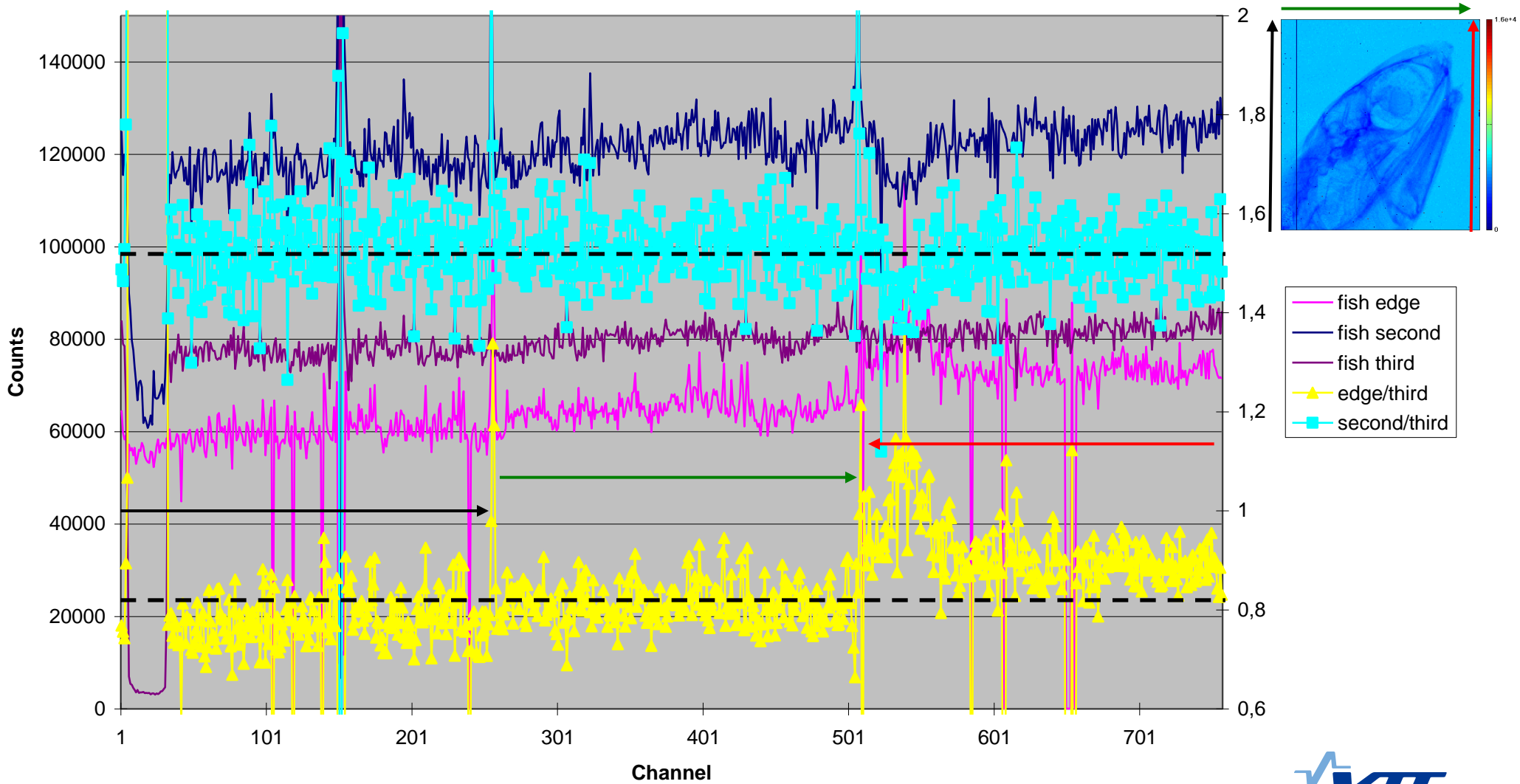
Sr90 (0.5 MeV e⁻)



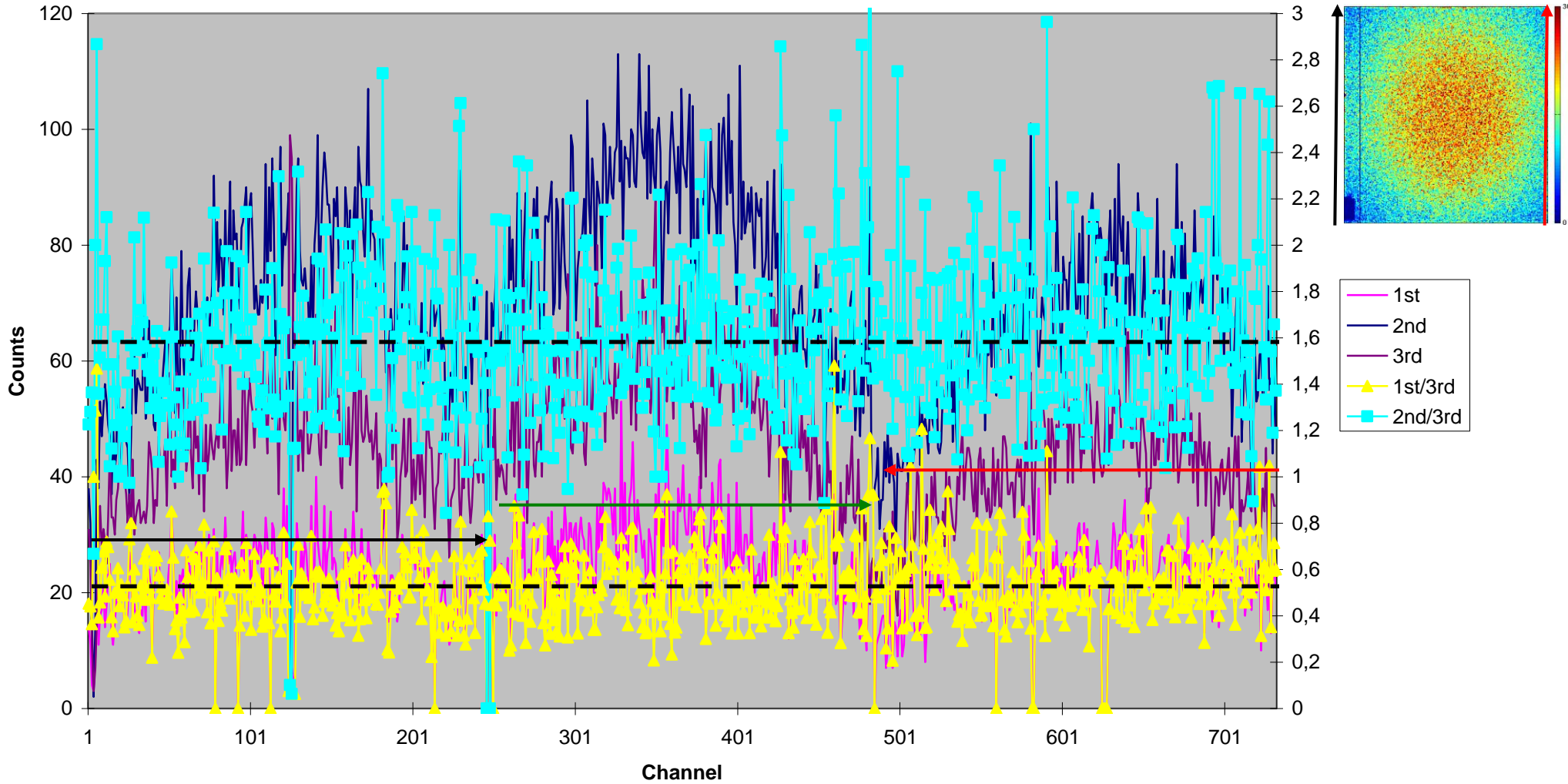
L6 detector corner response to Sr90 (e-)



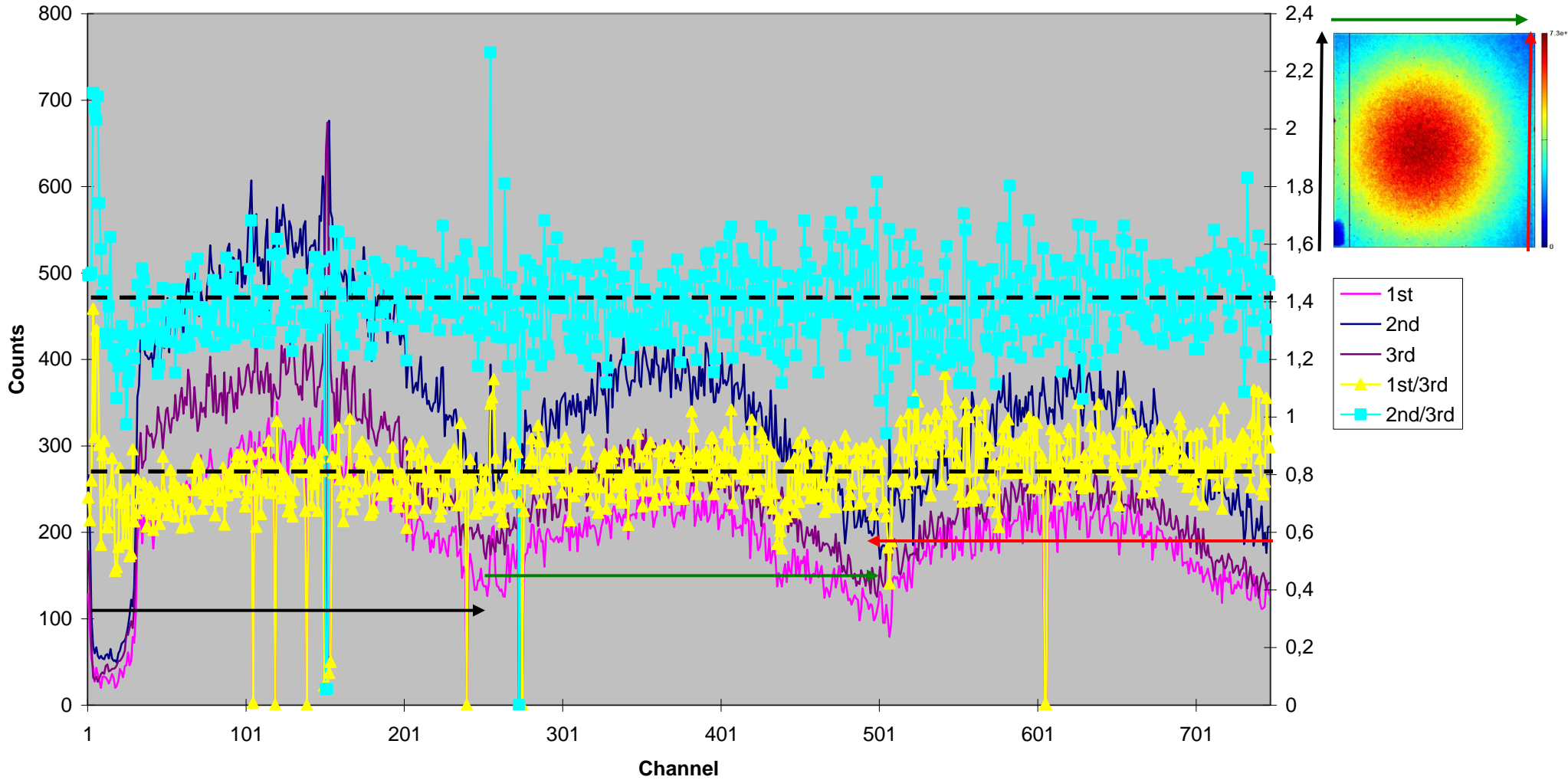
M7 (50 um), 30 keV, ff-image, 606 s



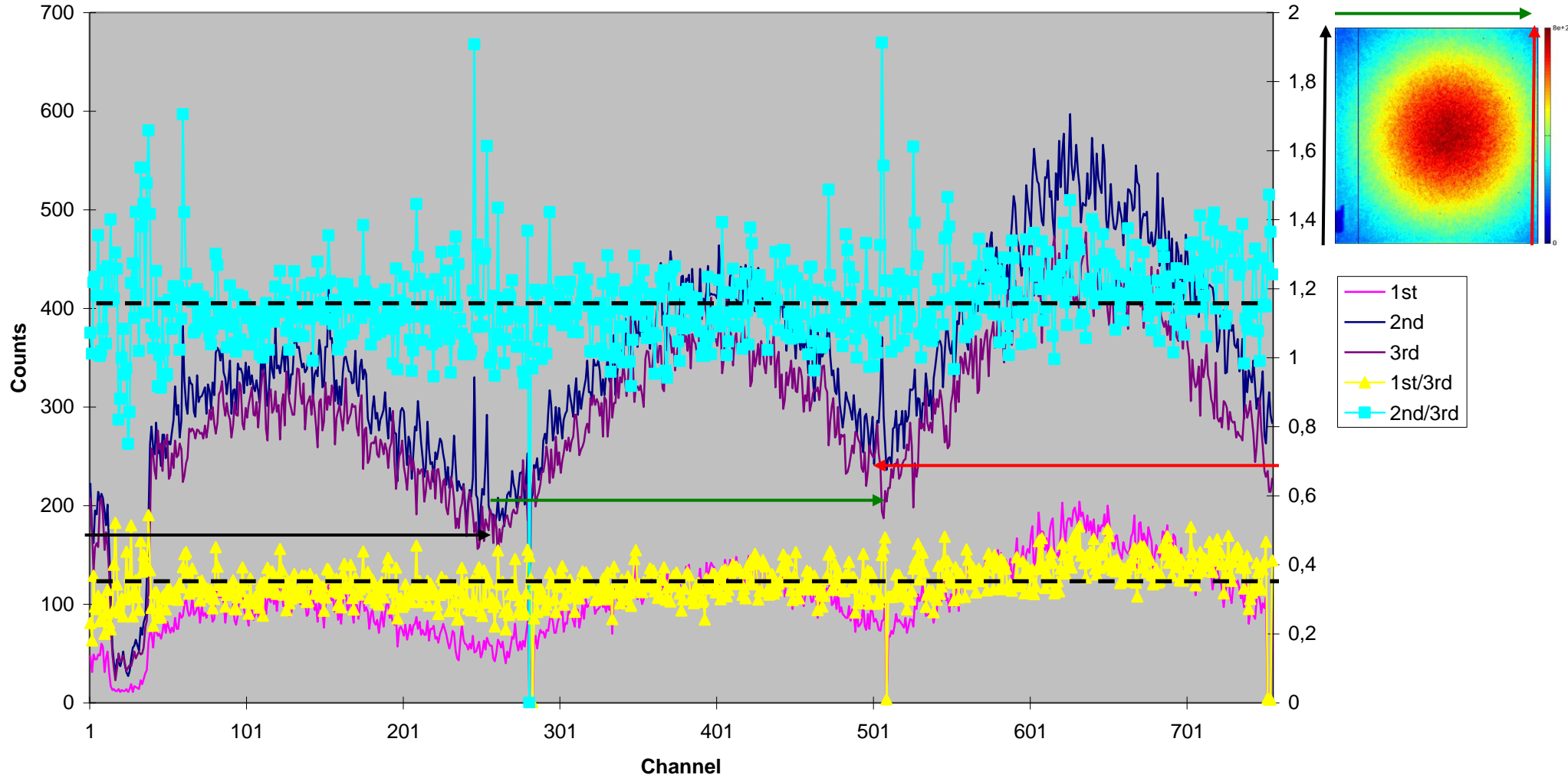
M7 (50 um) Cd109 (22 keV)



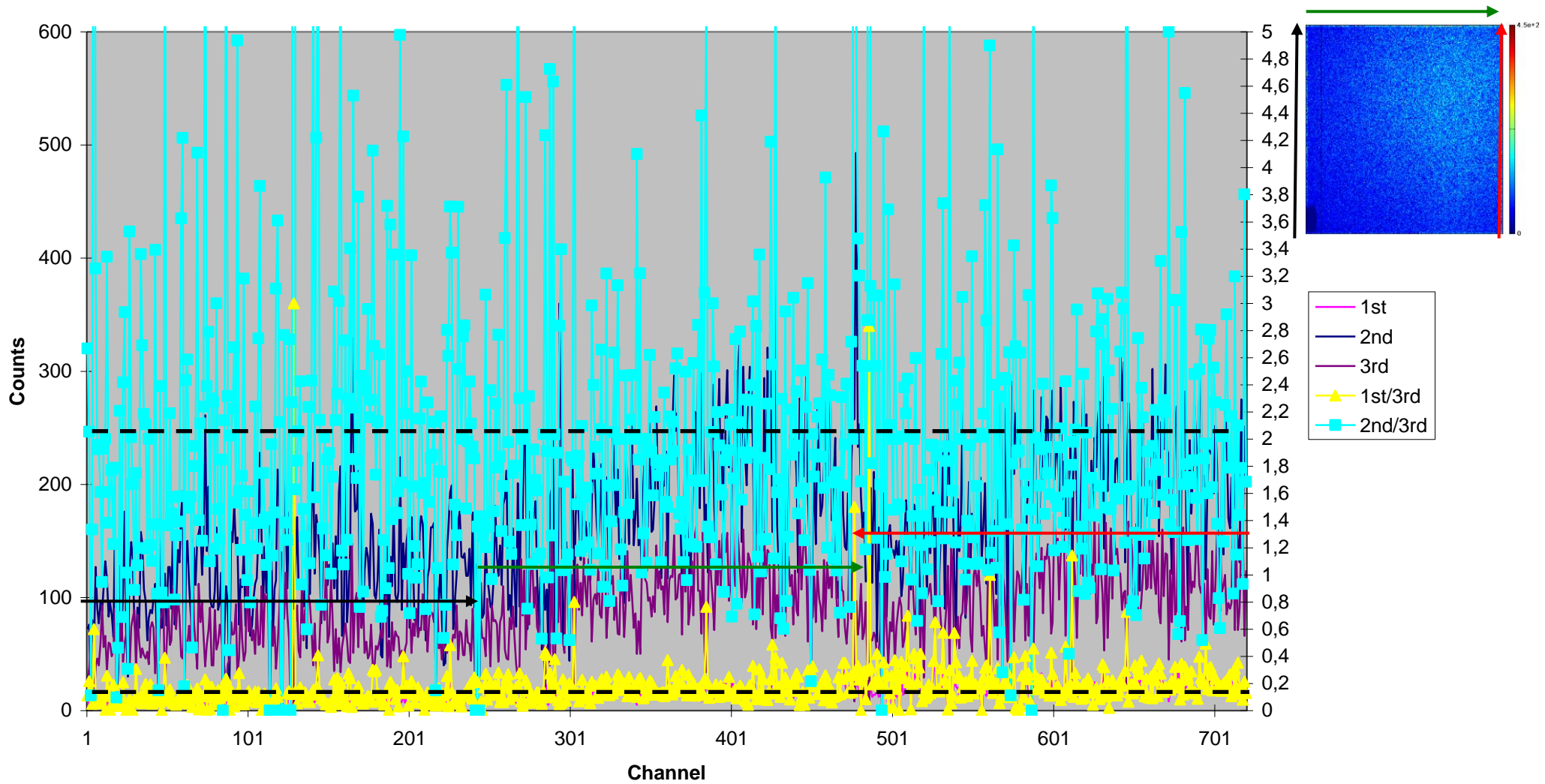
M7 (50 um) sr90 (e-)



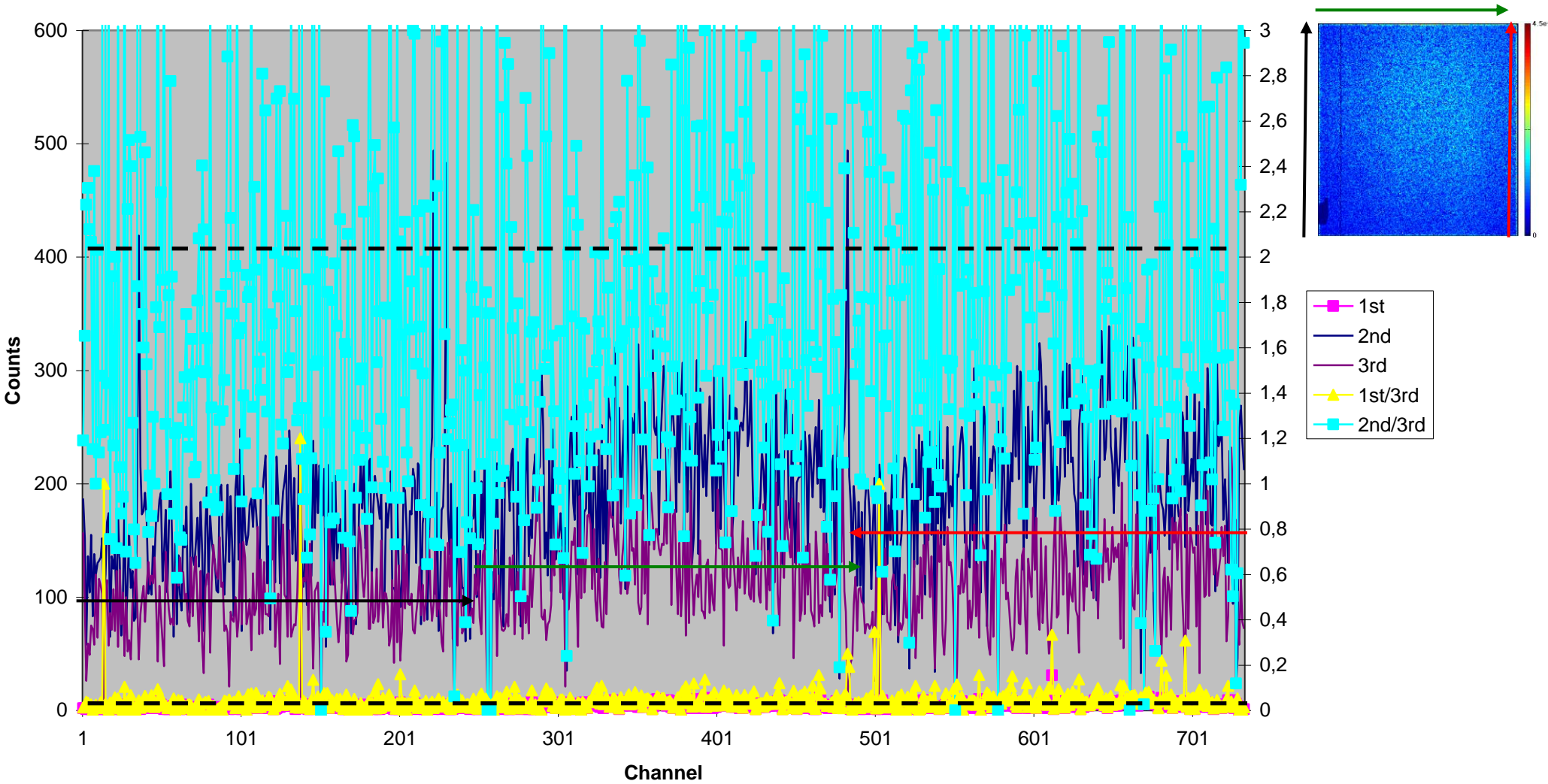
L6 (20 um) Sr90 (e-)



M7 (50 μm) Fe55 ($1/e \sim 30 \mu\text{m}$)



L6 (20 μm) Fe55 (1/e $\sim 30 \mu\text{m}$)



Detector Response summary

- Flat field image responses very close to the simulated area ratios
- Radiation source responses support the simulated model
- Uniform response could be obtained with 60 μm edge distance for 150 μm thick detector, *i.e.* edge distance/thickness ratio $\sim 40\%$

	Edge distance	1st/3rd	2nd/3rd
Simulation	20 μm	0,28	1,13
	50 μm	0,76	1,47
ff-image	50 μm	0,82 \pm 0,08	1,52 \pm 0,06
Cd109	50 μm	0,53 \pm 0,13	1,60 \pm 0,27
Sr90	20 μm	0,35 \pm 0,04	1,16 \pm 0,06
	50 μm	0,80 \pm 0,09	1,39 \pm 0,11
Fe55	20 μm	0,04 \pm 0,03	2,06 \pm 1,18
	50 μm	0,18 \pm 0,09	2,12 \pm 0,91

Summary

- First n-on-n edgeless pixel detector prototypes have been fabricated, packaged to the Medipix2 ROC and characterized with X-ray tube and radiation sources.
 - Leakage currents of 90 nA/cm^2 and 88 nA/cm^2 for $20 \text{ }\mu\text{m}$ and $50 \text{ }\mu\text{m}$ active edge distances
 - Full depletion at 5 V
 - No breakdown below 70 V
 - Response of the edge pixels depends dramatically on the active edge distance
 - Detector geometry can be optimized to give uniform pixel response
- VTT has capability to produce and deliver edgeless and full 3D edgeless pixel detectors in 2-4 months.
 - Three edgeless prototype processes done (1 poly & 2 edge implantation)
 - Good understanding of the edgeless 3D process and non-planar lithography
 - Improved process started: includes AC-coupled FOXFET and PT detectors
- Further work in edgeless detectors: fabrication for different ROC designs, radiation hardness tests and beam tests.



VTT creates business from technology



VTT's process capabilities for advanced detectors

- Operator time 48-54% of the equipment time -> parallel batch processing
- Delivery time includes possible UBM process and handle wafer removal
- Add 1 month to the delivery time for the prototype process

	DC PIXEL (realized)	EDGELESS POLY (realized)	EDGELESS IMPLANTATION (realized)	NEW EDGELESS IMPLANTATION (estimate)	FULL 3D EDGELESS POLY (estimate)
PROCESS TIME (h)	118 (2-3 WEEKS)	511 (10-11 WEEKS)	305 (6-7 WEEKS)	246 (5 WEEKS)	356 (7-8 WEEKS)
PROCESS STEPS	72	118	119	109	152
BOTTLE NECKS (% OF THE PROCESS TIME)	LITHOGRAPHY 25% FURNACE 24%	FURNACE 46% DRY ETCH 13% PLANARIZATION 12 %	LITHOGRAPHY 23% FURNACE 20%	LITHOGRAPHY 22% FURNACE 20%	FURNACE 27% DRY ETCH 20%
DELIVERY TIME	<i>1 MONTH</i>	<i>3-4 MONTHS</i>	<i>2-3 MONTHS</i>	<i>2 MONTHS</i>	<i>3 MONTHS</i>