

SiLC DAQ



EUDET Meeting 2010

Alexandre CHARPY & LPNHE team



Conducted by LPNHE:

- Research baseline: wafer 6"-8", 200 μ m of thickness, pitch of 50 μ m, transparency ~70%, active edge
- Testing of the SiTr130 prototype and VA1' chip

Edgless with SOI technology

VTT- Juha Kallopuska

Manufacturing achievement:

- edgeless & pixels sensors, 6" wafer, 50 μ m pitch

HPK designed by Vienna w/wo surface treatment of silicon wafers(Santander)

- 50 μ m pitch, 320 μ m of thickness
- ~ 20% transmittance
- Alignment System (IFCA) using an infra-red laser in labs & tests beam

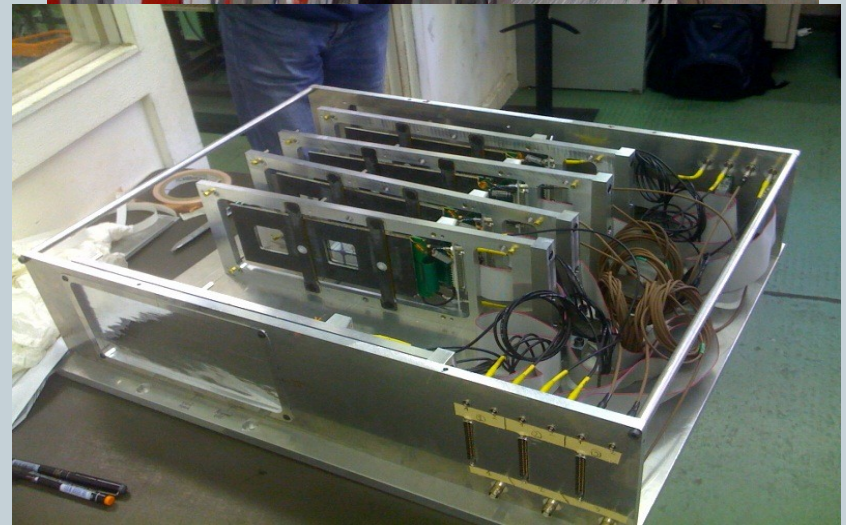
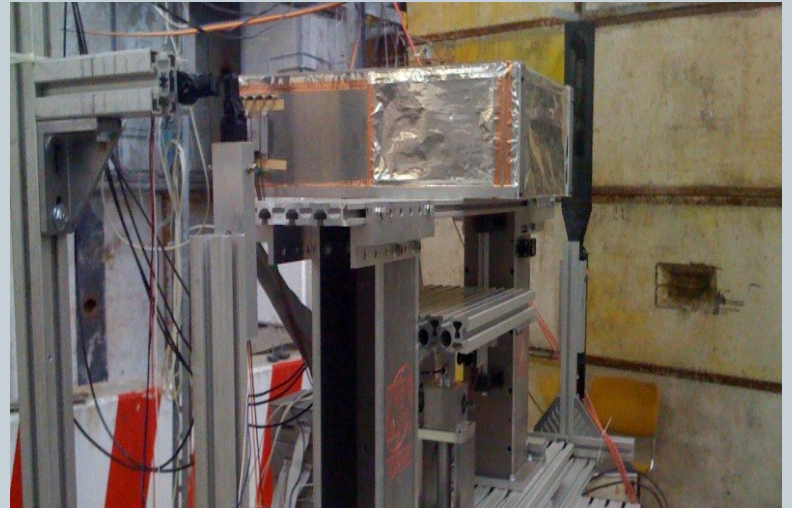
Edgeless planar strips

FBK-irst-U. Trento/INFN - Gian Franco Dalla Betta

- Prototyped sensors 2.5x5cm² (Trento & LPNHE)
- full characterization at Lab followed by beam test & HPK comparison

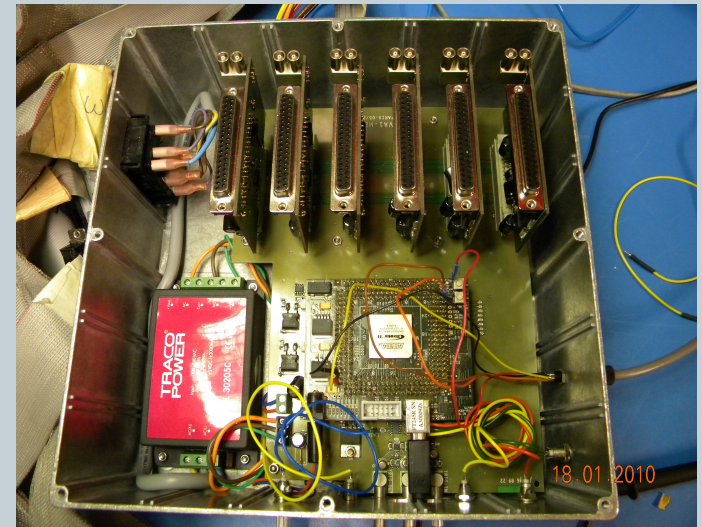


- Standalone telescope, with five silicon sensors layers: until 2048 channels active strips/modules
- Intended to be easily integrated to a test beam
 - High customization
 - All Electronic features In One “AlteraBox”
 - Main functionalities (Peaking Time, Laser Alignment etc...)





- Evolutive DAQ Hardware ToolKit (EUNET deliverable)
 - Adapted to both: VA1 (référence) prototypes SiTr-130 and next, mix mode (VA1+SiTr chips)
 - USB/FPGA interface with microcontroller
 - TTL/NIM for triggering and laser alignment
 - AlteraBox chaining
 - Power supplied embedded
 - **Need to integrate the TLU ?**



Faster serial Interface:

- Ethernet

Development toward the final DAQ design for ILD → link with the mechanical constraint



Acquisition requirement:

- Increasing of the data size management
- Addressing of the data
- On-line control
- High Flexibility

Narval is the main frame (ADA-oriented) <https://forge.in2p3.fr/projects>

→ module programming: ADA/C/C++

→ *Can be easily connected to any global DAQ software → what is needed ?*

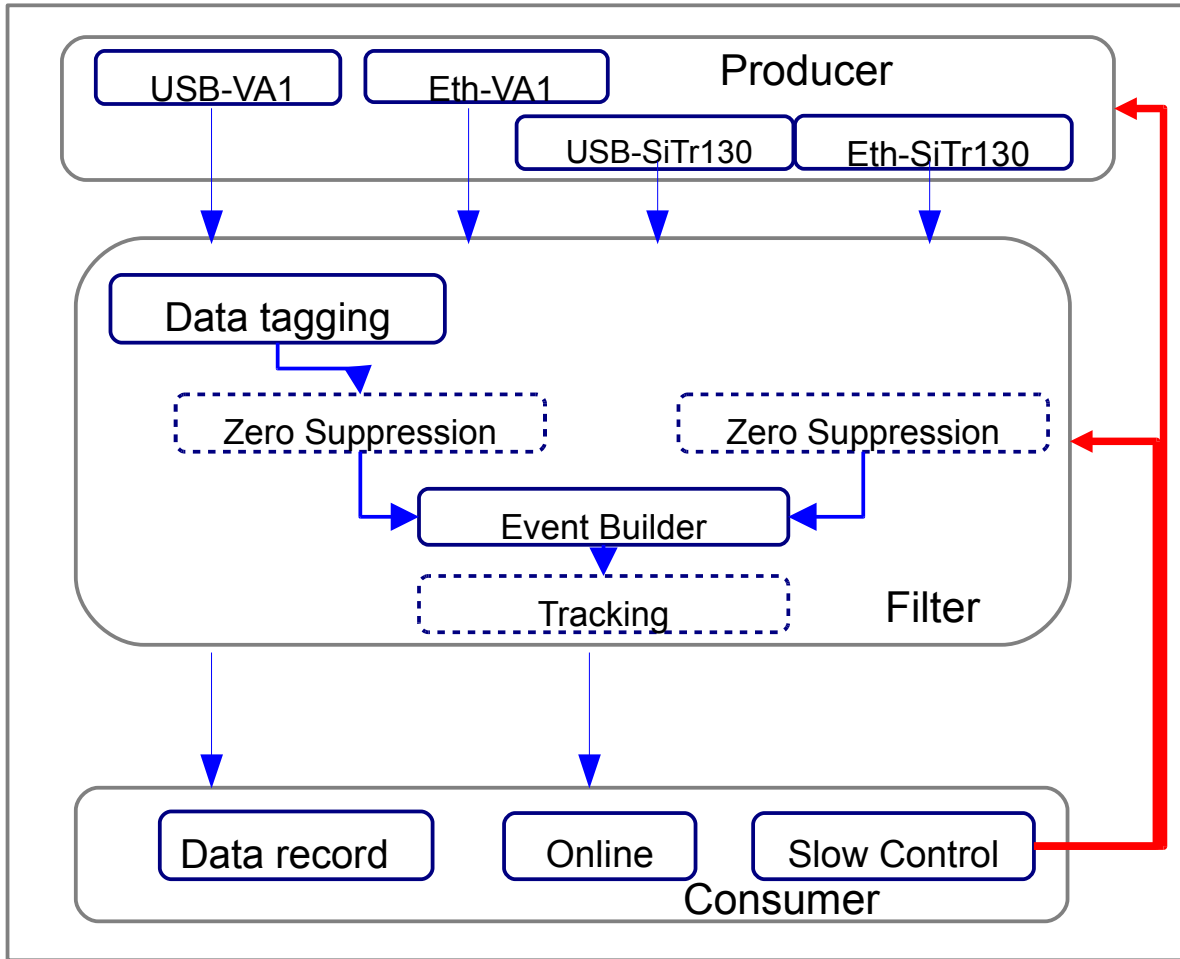
→ *Can easily include another DAQ system*

→ *ENX for the slow Control*

FPGA system is handled by a full VHDL software package



Master: Narval as a linux server

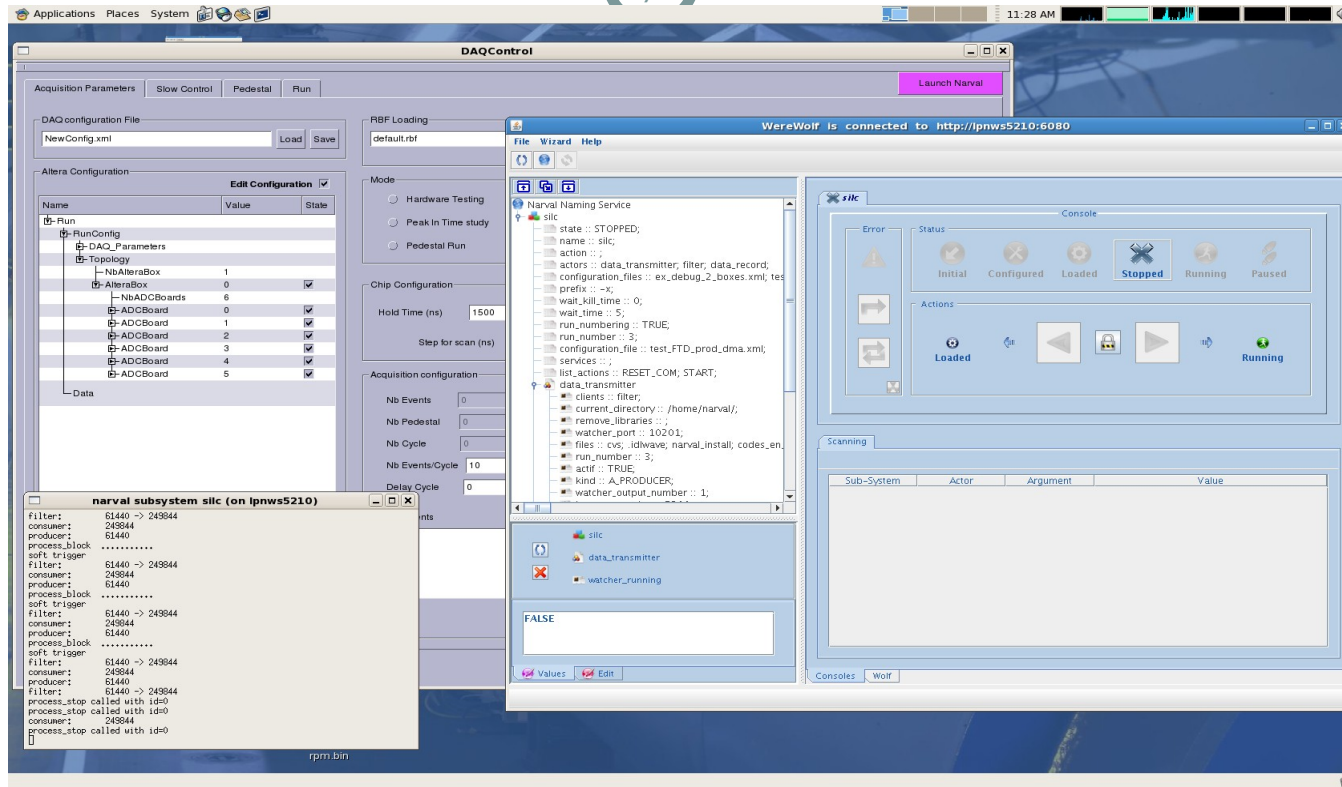


- Three basic actors:
 - Producers
 - Filters
 - Consumers (could be created)

• Dedicated libraries in C/C++/ADA95

• High flexibility with very simple scripts & xml files

Raw Data format for combined test beam ?



•Narval Control

•Configuration and online:

- QTRoot → developped @ LPNHE for SiLC
- DAQ Configuration, Basic Analysis, Online

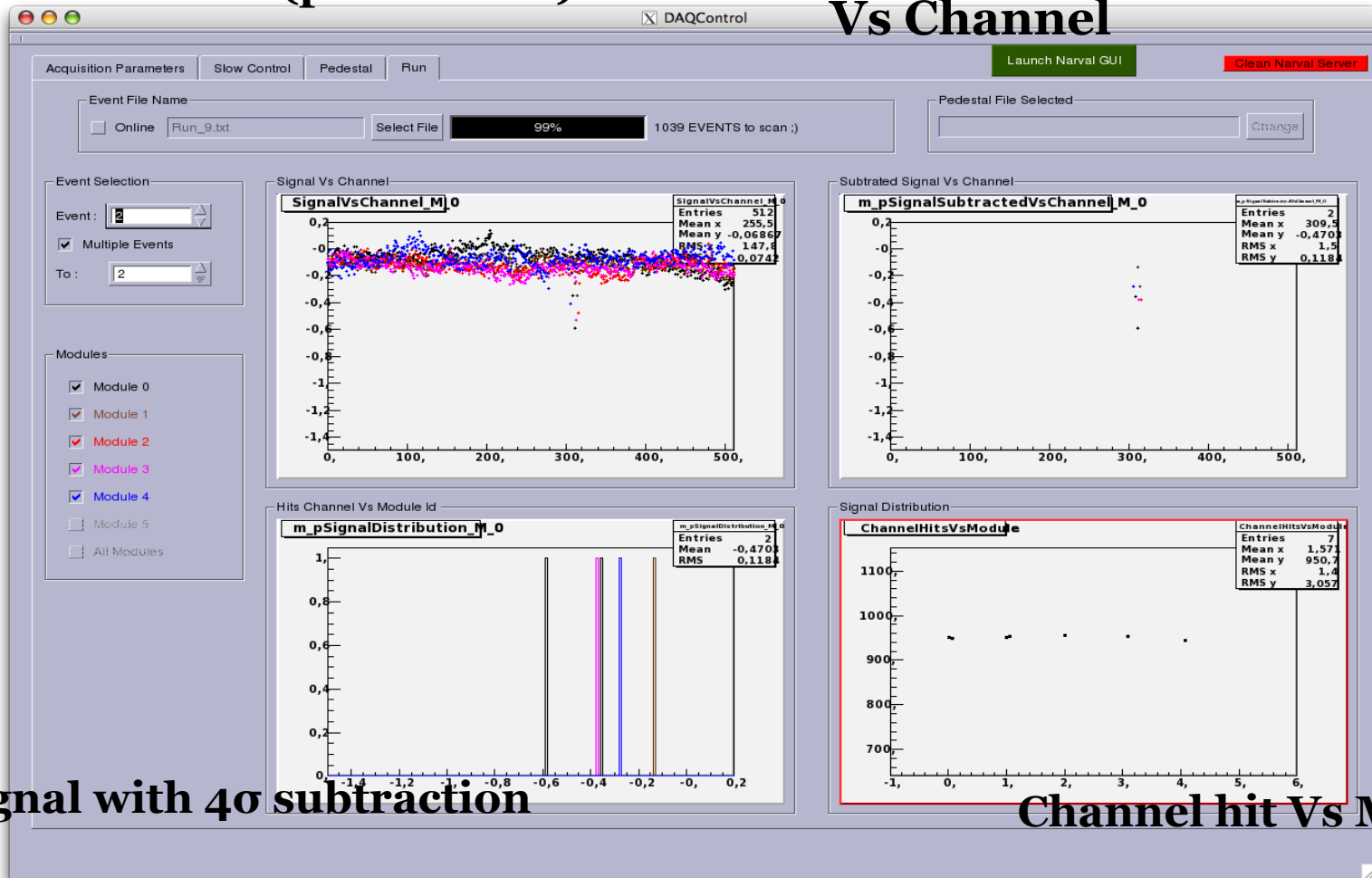
Next evolution: web
interface



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Signal vs Channel (per module)

Signal with subtracted pedestal Vs Channel



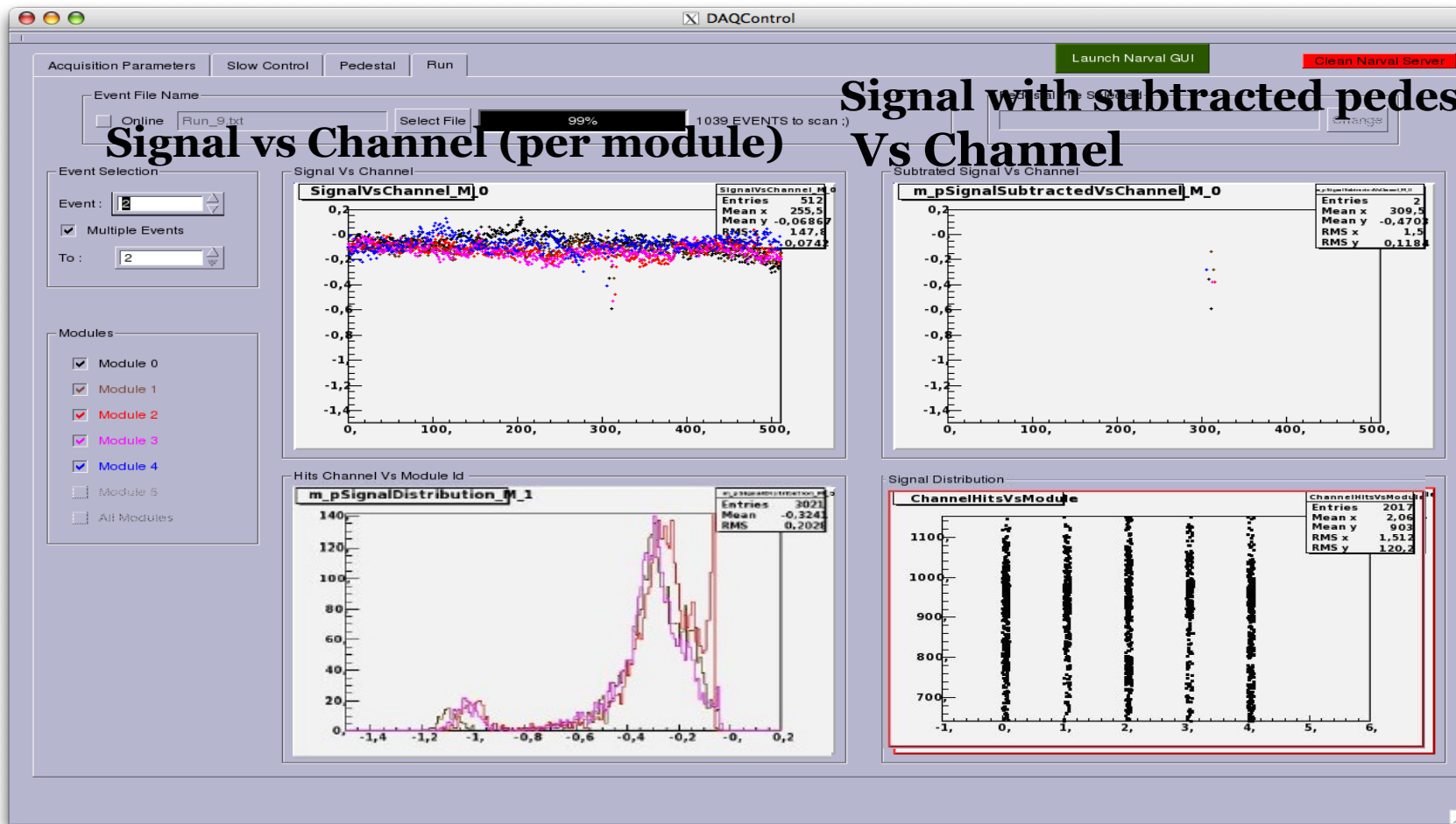
Signal with 4σ subtraction

Channel hit Vs Module

Online Monitoring Cumulated events



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Signal vs Channel (per module)

Signal with subtracted pedestal Vs Channel

Signal with 4σ subtraction

Channel hit Vs Module



MIDAS experiment "Pibeta"		Wed Apr 12 12:33:03 2000						
Start	ODB	CNAF	Messages	ELog	Alarms	Programs	Config	Help
Trigger settings Rates Ratios Chambers PID Handbook WebCam Accelerator								
Run #30160	Stopped	Alarms Off	Restart Yes	Data dir: /data				
Start: Wed Apr 12 07:50:46 2000				Stop: Wed Apr 12 08:27:26 2000				
Equipment	FE Node	Events	Event rate[/s]	Data rate[kB/s]	Analyzed			
Trigger	Trigger Frontend@pc812	22029	0.0	0.0	100.0%			
Scaler	Trigger Frontend@pc812	217	0.0	0.0	100.0%			
HV	SC Frontend@pc809.psi.ch	0	0.0	0.0	0.0%			
Environment	SC Frontend@pc809.psi.ch	0	0.0	0.0	0.0%			
Chamber	Trigger Frontend@pc812	38	0.0	0.0	100.0%			
Beamline	SC Frontend@pc809.psi.ch	0	0.0	0.0	0.0%			
Channel	Active	Events	MB written	GB total				
0 run30160.mid	Yes	22362	32.440	31.286				
Lazy Destination	Progress	File Name	Speed [kb/s]	Total				
psarchive	100 %	run30158.mid	773.9	3.3 %				
Lazy Label	Progress	File Name	# Files	Total				
2000-2	100 %	run30158.mid	44	45.5 %				
11:01:44 [ODBEdit2] Program ODBEdit2 on host pc2106 stopped								
ODBEdit [pc2106]		Lazy_FTP [pc2106]		Lazy_Tape [pc2106]				
Logger [pc2106]		ODBEdit1 [pc2106]		mhttpd [pc2106]				
Analyzer [pc2106]		Trigger Frontend [pc812]		SC Frontend [pc809.psi.ch]				

- Generic acquisition system for little & middle size experiments .
- Known for years at TRIUMF and PSI
- Easily portable for any operating system (embedded systems included)
- Include a « slow control » system, on-line database and an « history system »
- Tests in progress with this system for being used during November tests and a future embedded system.

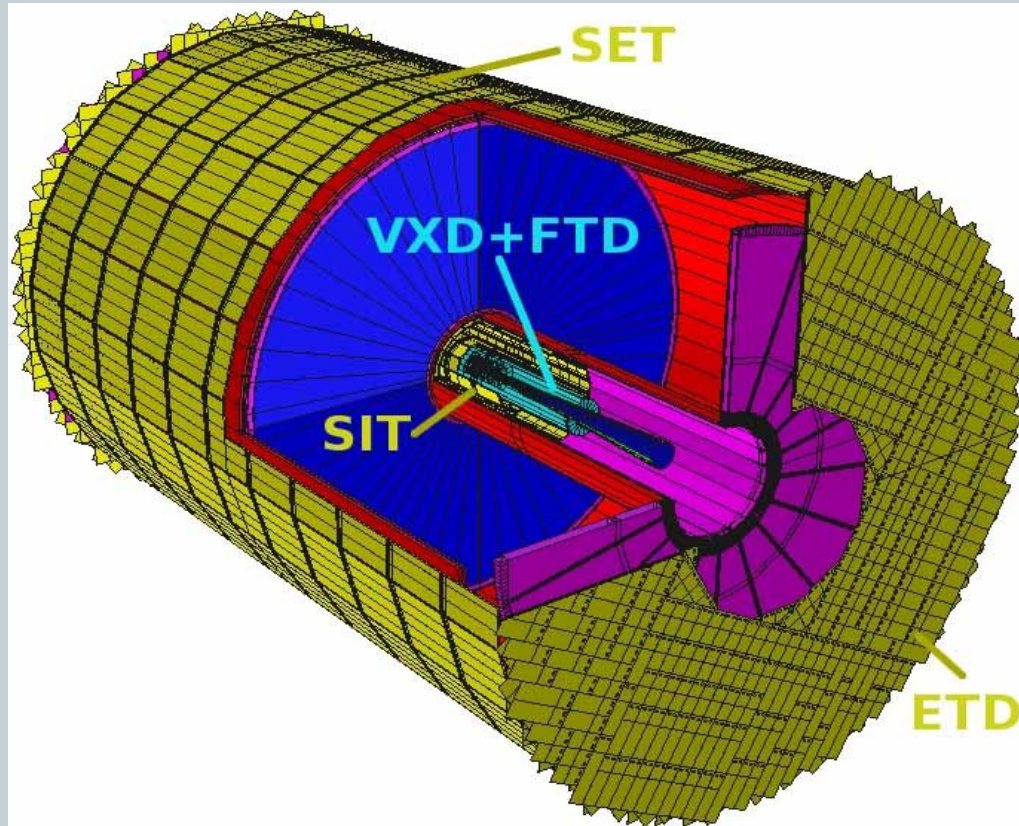
VHDL software is slightly modified for processing data from new front-end cards in November(cf. Marc Dhellot)

Prospect for 2012

The Silicon Envelope of ILD



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Total number of modules:

500 (SIT) + 2500 (SET) + 2000 (ETDs)

5000 modules of 1792 channels

Total number of channels:

10^6 (SIT) + 5×10^6 (SET) + 4×10^6 (2 ETD)

10×10^6 channels

~5.12 Gbytes

Component	Layer #	# modules	# sensors/ module	# channels	Total surface m ²
SIT1	1 st layer	33	3	66.000	0.9
	2 nd layer	99	1	198.000	0.9
SIT2	1 st layer	90	3	180.000	2.7
	2 nd layer	270	1	540.000	2.7
SET	1 st layer	1260	5	2.520.000	55.2
	2 nd layer	1260	5	2.520.000	55.2
ETD_F	X or U or V	82/quad =328/layer =984/ETD	2 or 3 or possibly 4	2.000.000	30
ETD_B	idem	idem	idem	idem	30

Detailed design

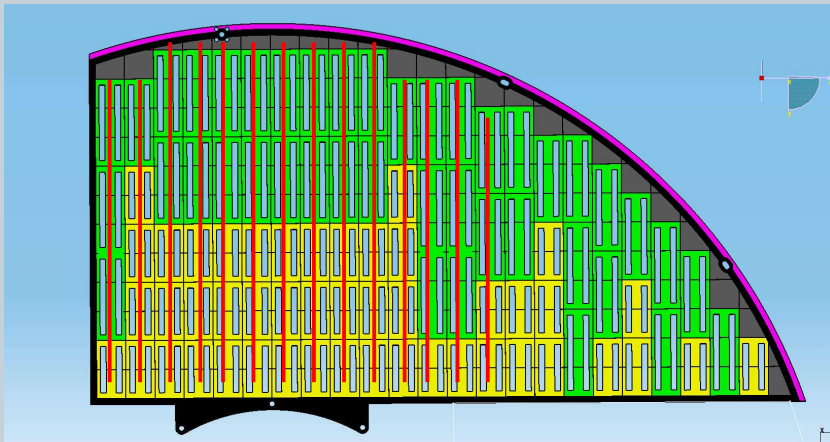
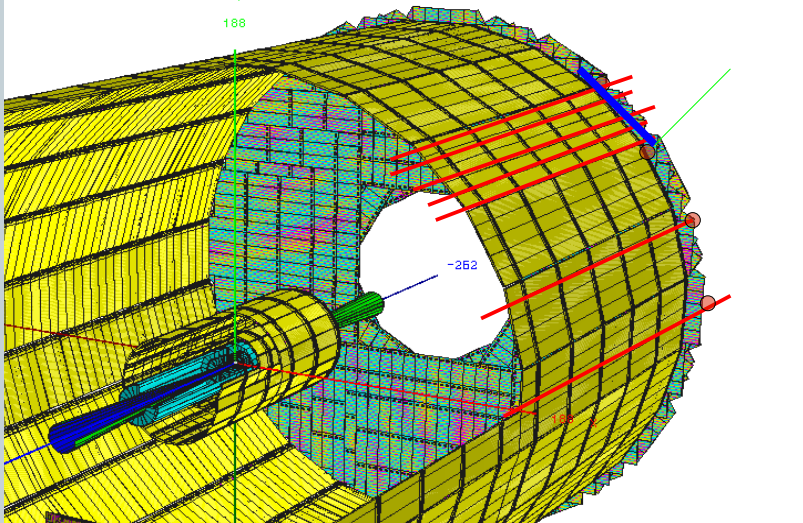
GEANT4 simulation both in MOKKA & ILCROOT
(here) & mechanical design (CATIA) in progress

Prospect for 2012

The Silicon Envelope of ILD

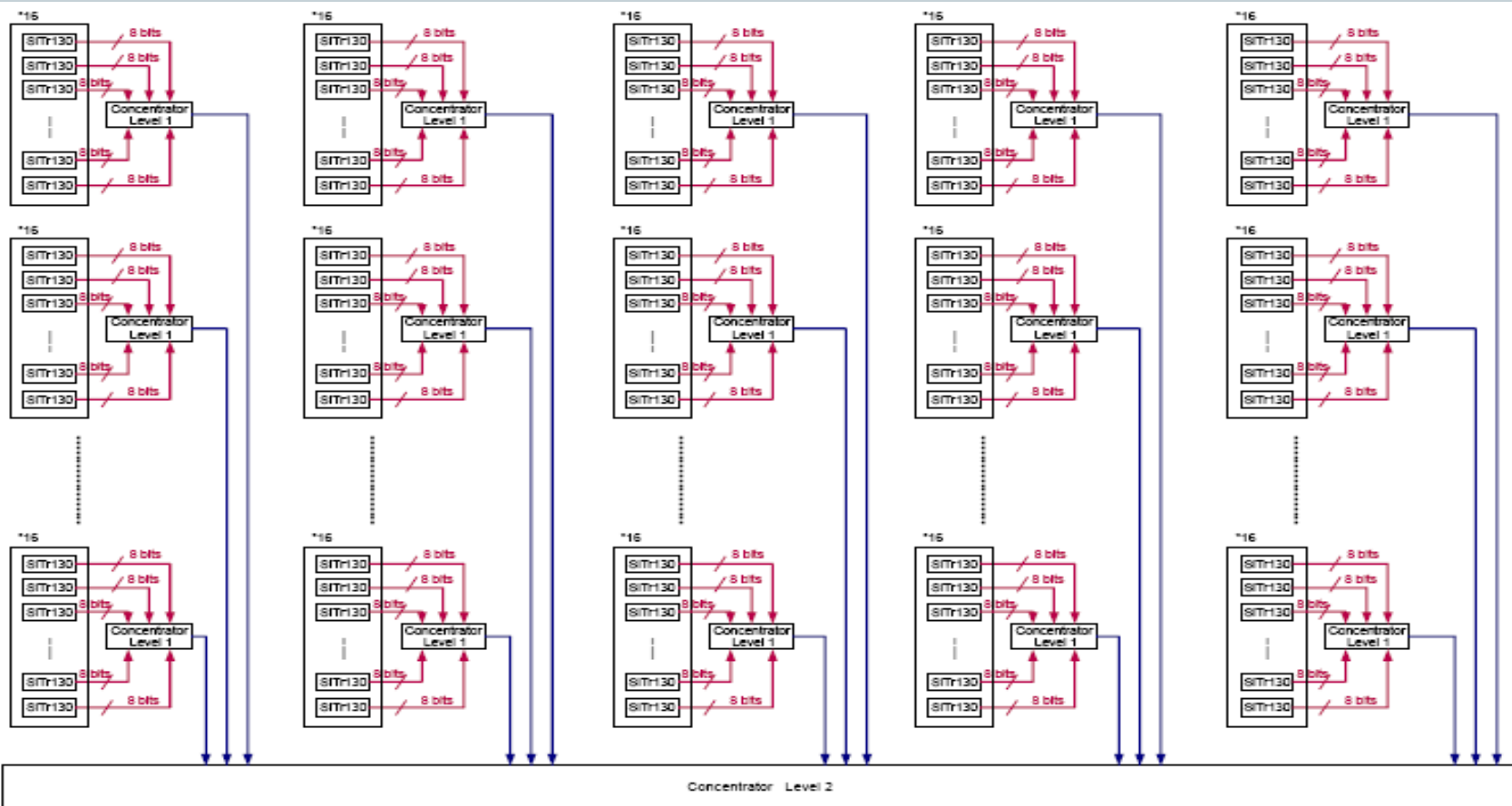


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- On the “module”:
Chaining of 14 SiTR130-128
- “Super Module”:
Chaining the adjacent ladders toward a level 1 concentrator
- Half cylinder (“Detector Element”):
Level 1 concentrator (toward level 2 ?)
- Toward the global Silicon DAQ system
by Optical fibers
- Send to Global DAQ system

Depending on the final requirements



Preliminary study: micro-FPGA BGA on board



Thanks for your intention