Digital processing and characterization plans of the 16-channel S-ALTRO demonstrator

People :

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Massimiliano De Gaspari ….. **Front-end + ADC**

Hugo França-Santos ……. **ADC**

Eduardo Garcia …….. **Data Processing & Control**

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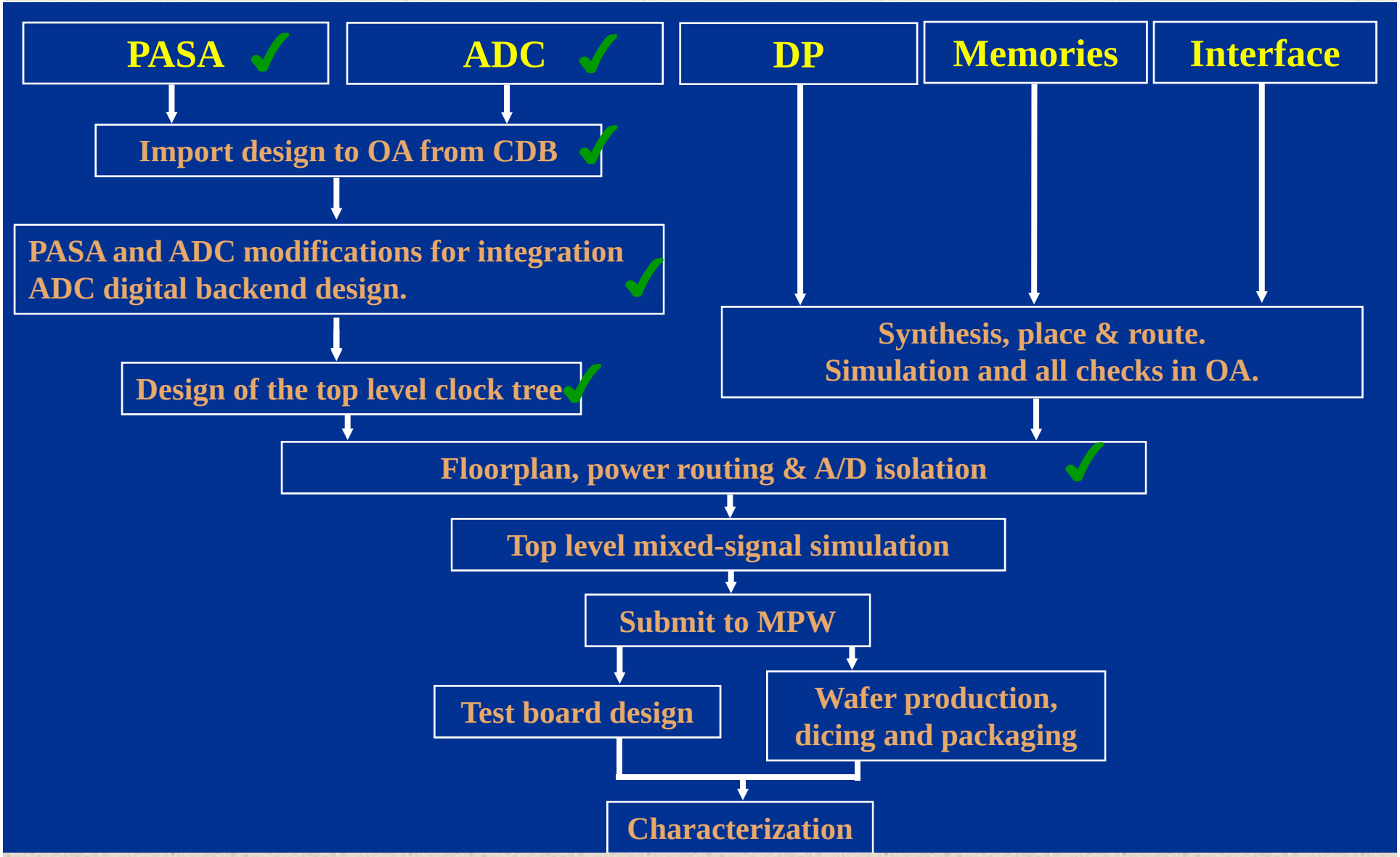
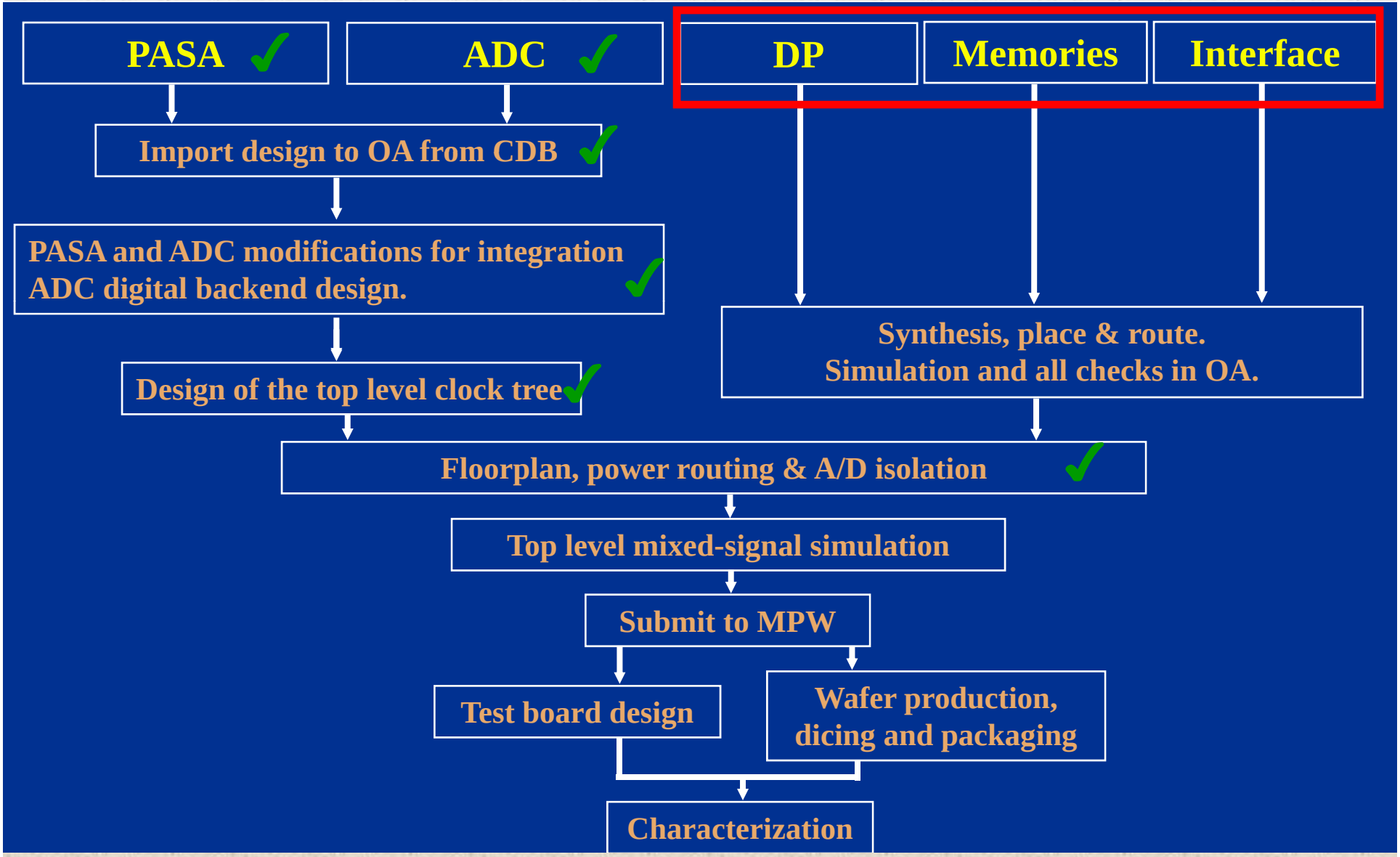
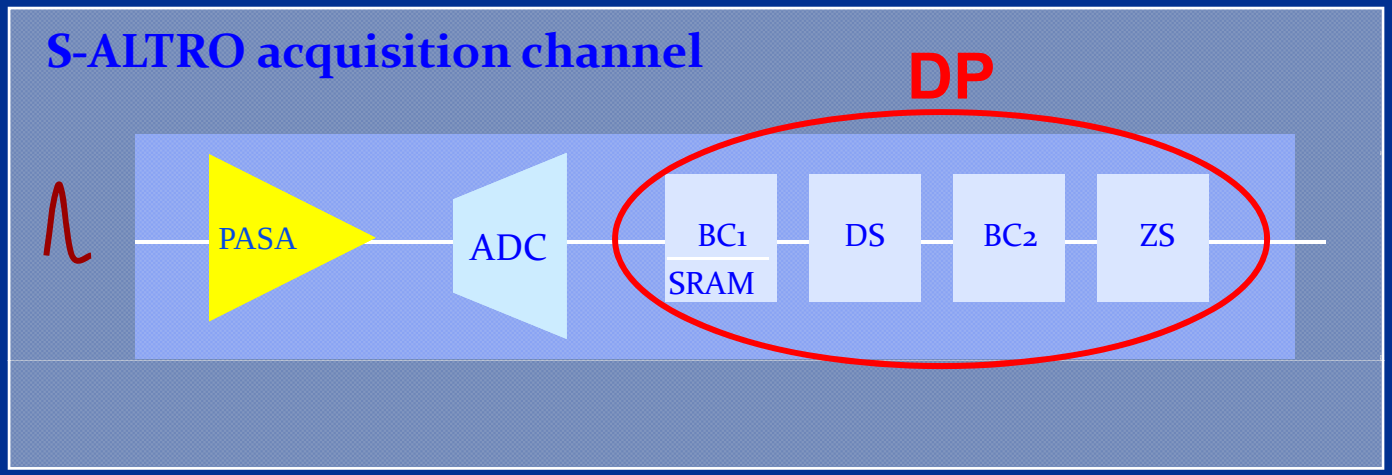
Demonstrator work flow



Demonstrator work flow



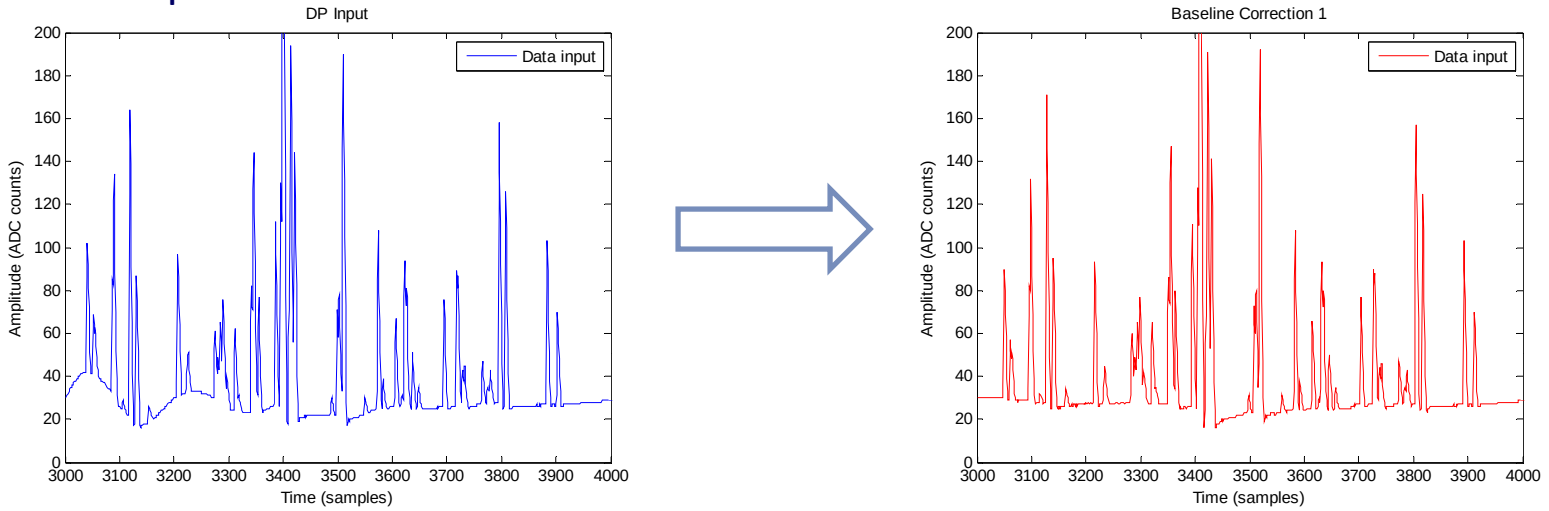
DP functions



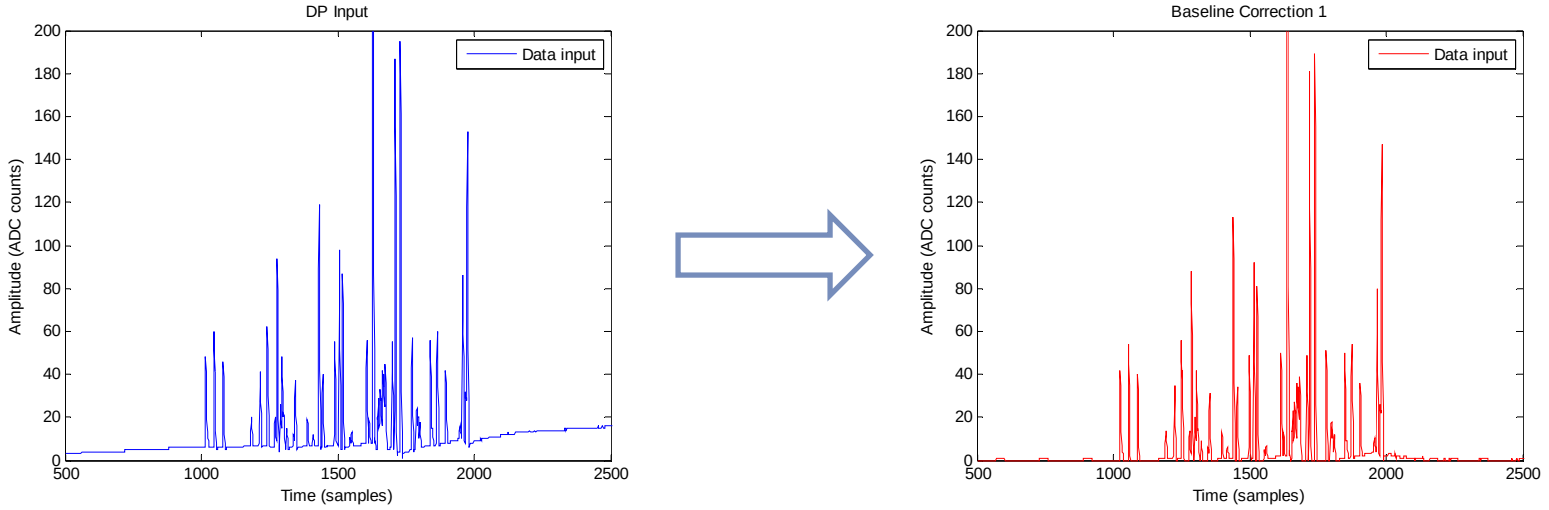
Baseline Correction 1	Removes the systematic offsets that are introduced due to clock noise pickup and switching of the gating grid of the detector. A baseline memory is used for storage of baseline constants which are used for look-up table correction of the base line.
Digital Shaper	Compensates the distortion of the signal shape due to very long ion tails.
Baseline Correction 2	Reduces non-systematic low frequency baseline movements based on a moving average filter.
Zero Suppression	Removes samples that fall below a programmable threshold.

DP simulation results

- BC1 example test: rest of the filters are disabled.

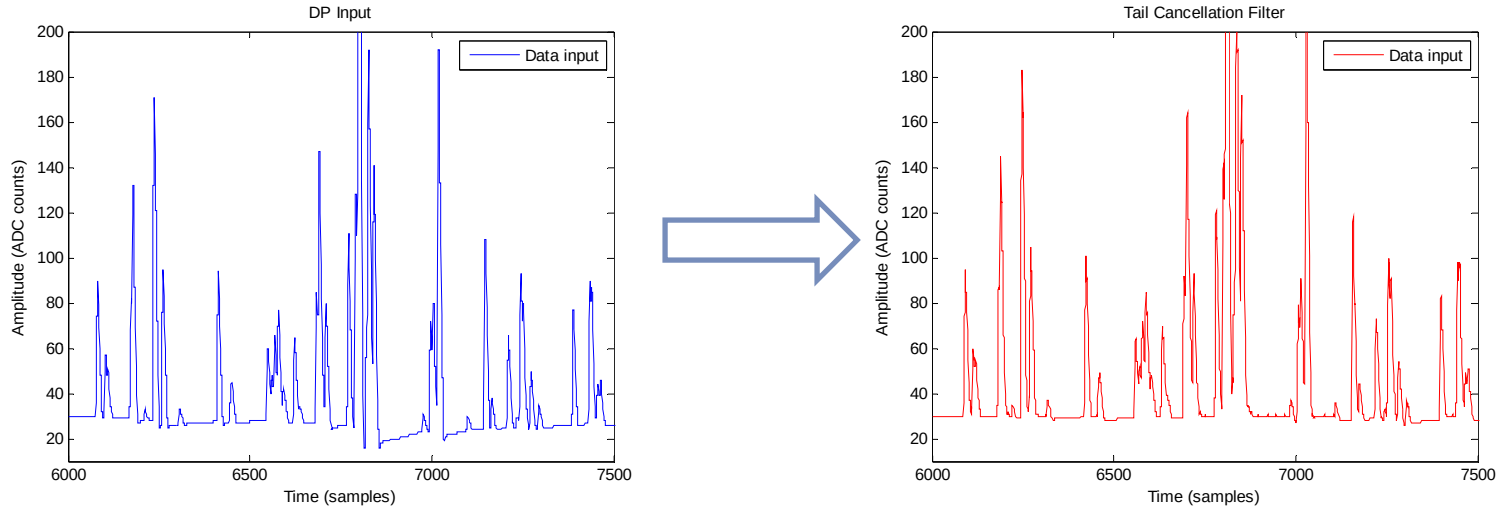


- BC1 example test: rest of the filters are disabled.

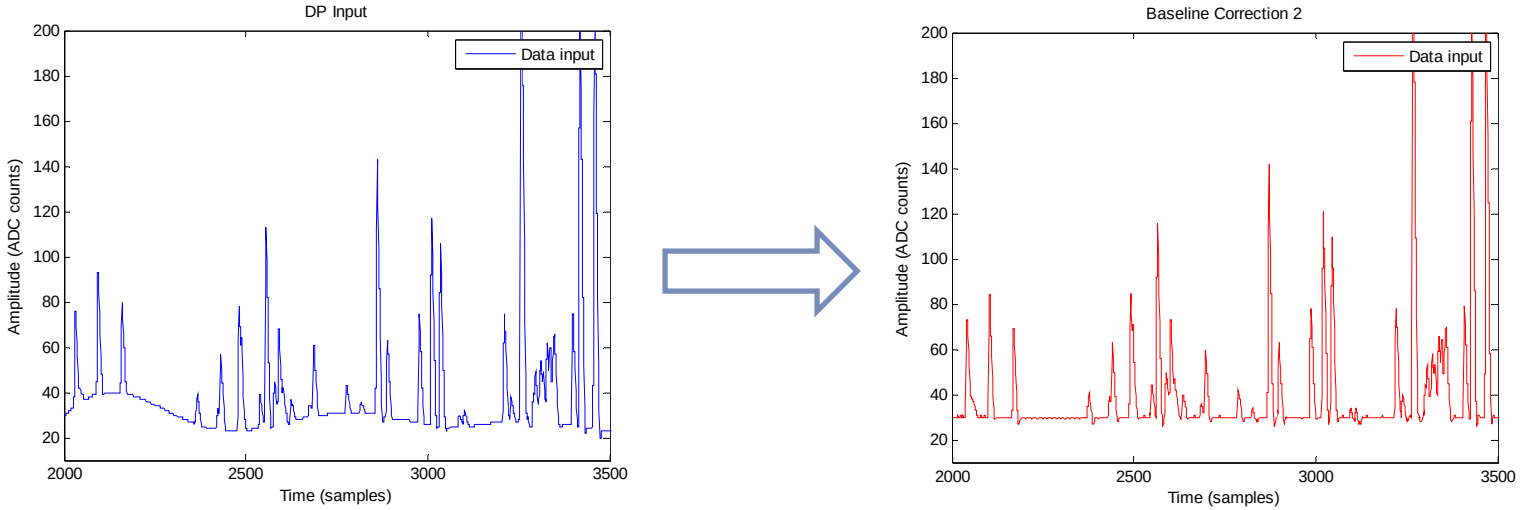


DP simulation results

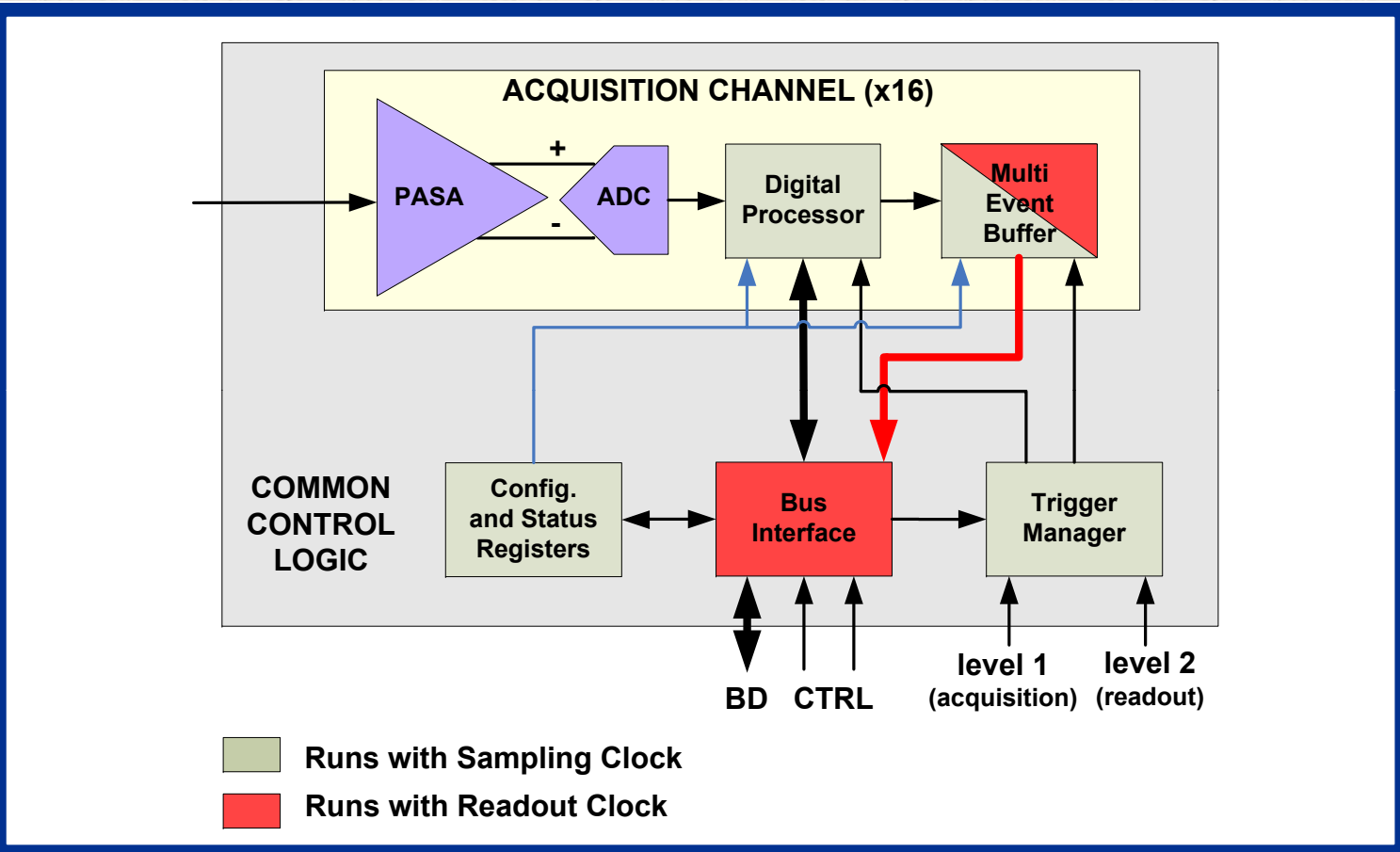
- DS example test: rest of the filters are disabled.



- BC2 example test: rest of the filters are disabled.

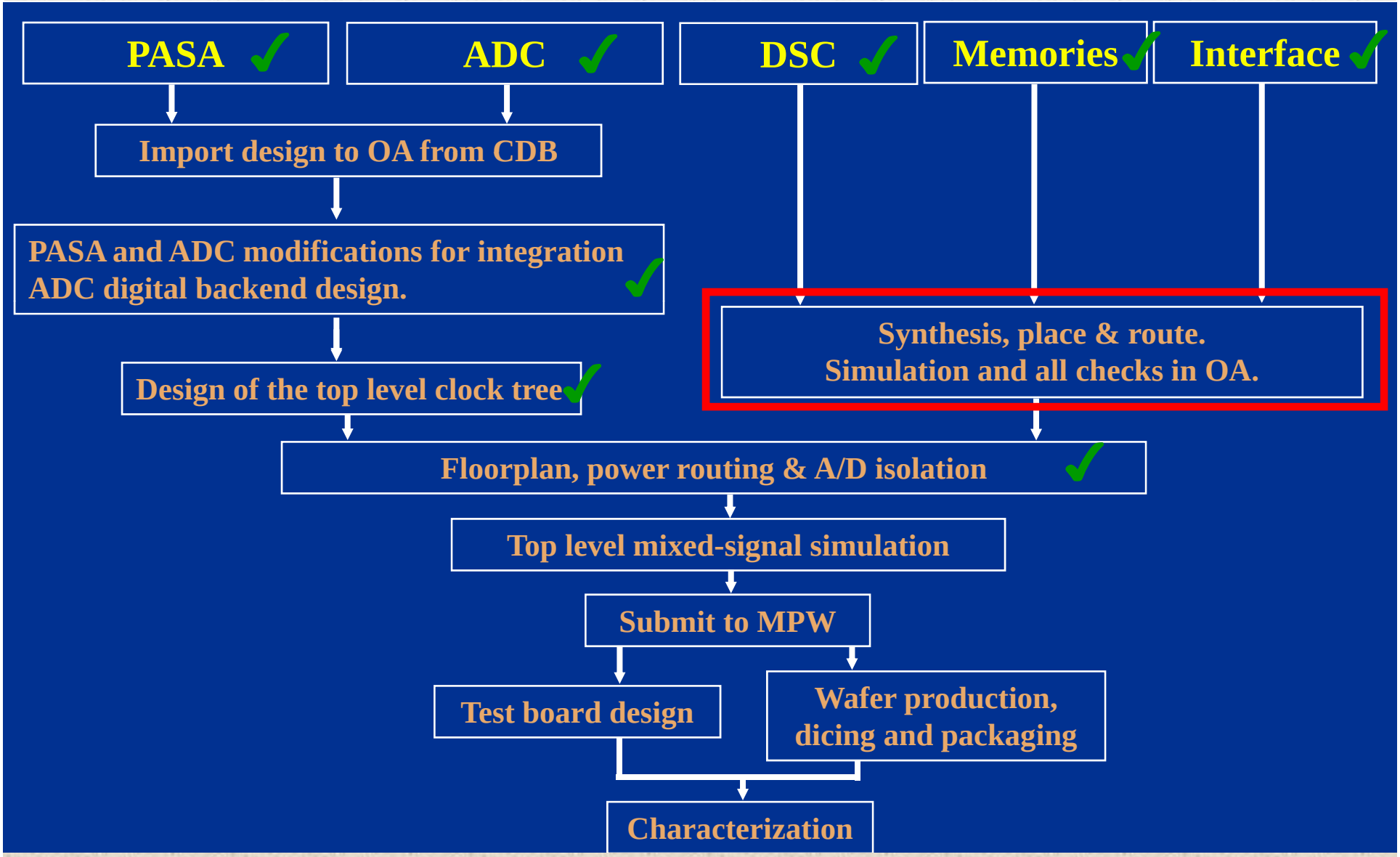


S-ALTRO Interface (based on ALTRO interface)

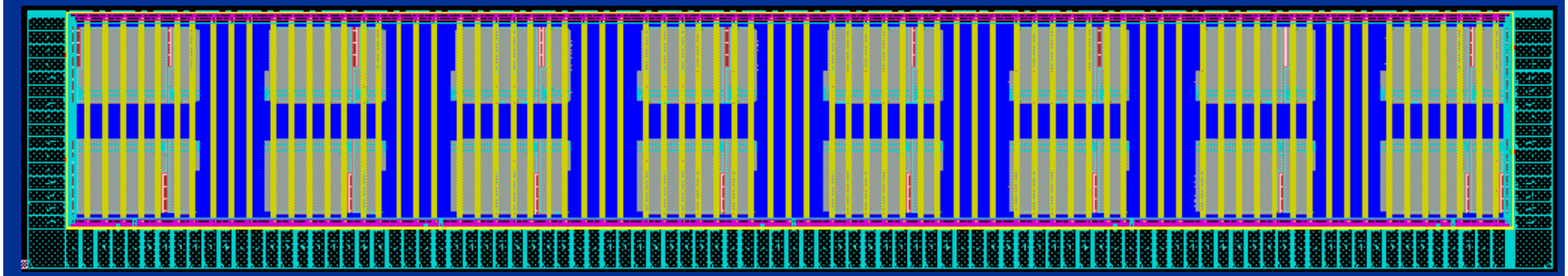


Level 1: Starts the data acquisition.
Level 2: Validates data from previous L1.
BD : 40 bit bidirectional bus; 20 bits address + 20 bit data. 80 Mbps readout.
CTRL : 6 bits.
Global Reset, Sampling and Readout clocks.

Demonstrator work flow



Power plan



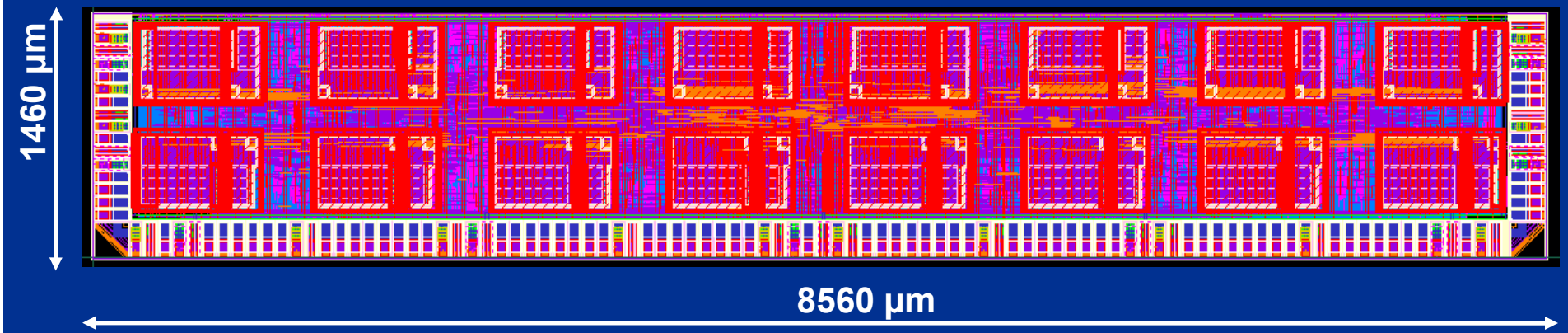
Conditions:

Static Analysis	Toggle probability: 0.3
VDD = 1.5V	Temperature: 25 C
Sclk = 50MHz	Voltage variation: 10%
Rdoclk = 90Mhz	Signoff verification

Encounter Statistical Power Analysis:

- Average power (considered in rail analysis): **118.62 mW**
- Worst IR drop peak: **7.2 mV**
- Max peak current: **19.856mA**

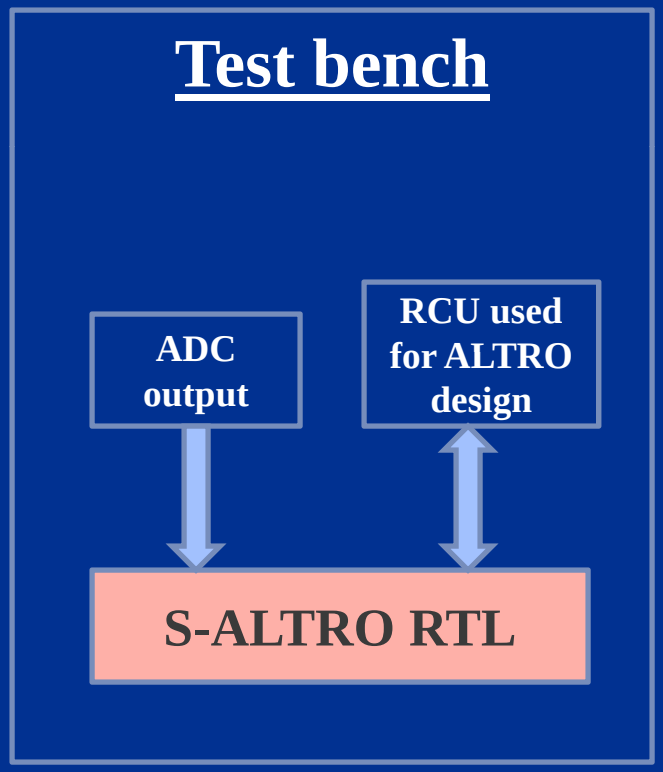
Layout and checks



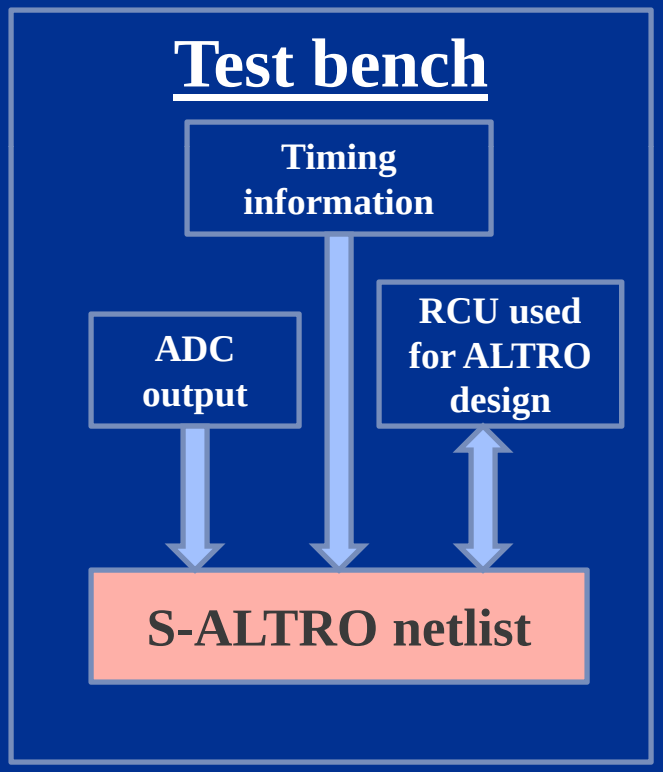
LVS ✓ DRC ✓

Simulation

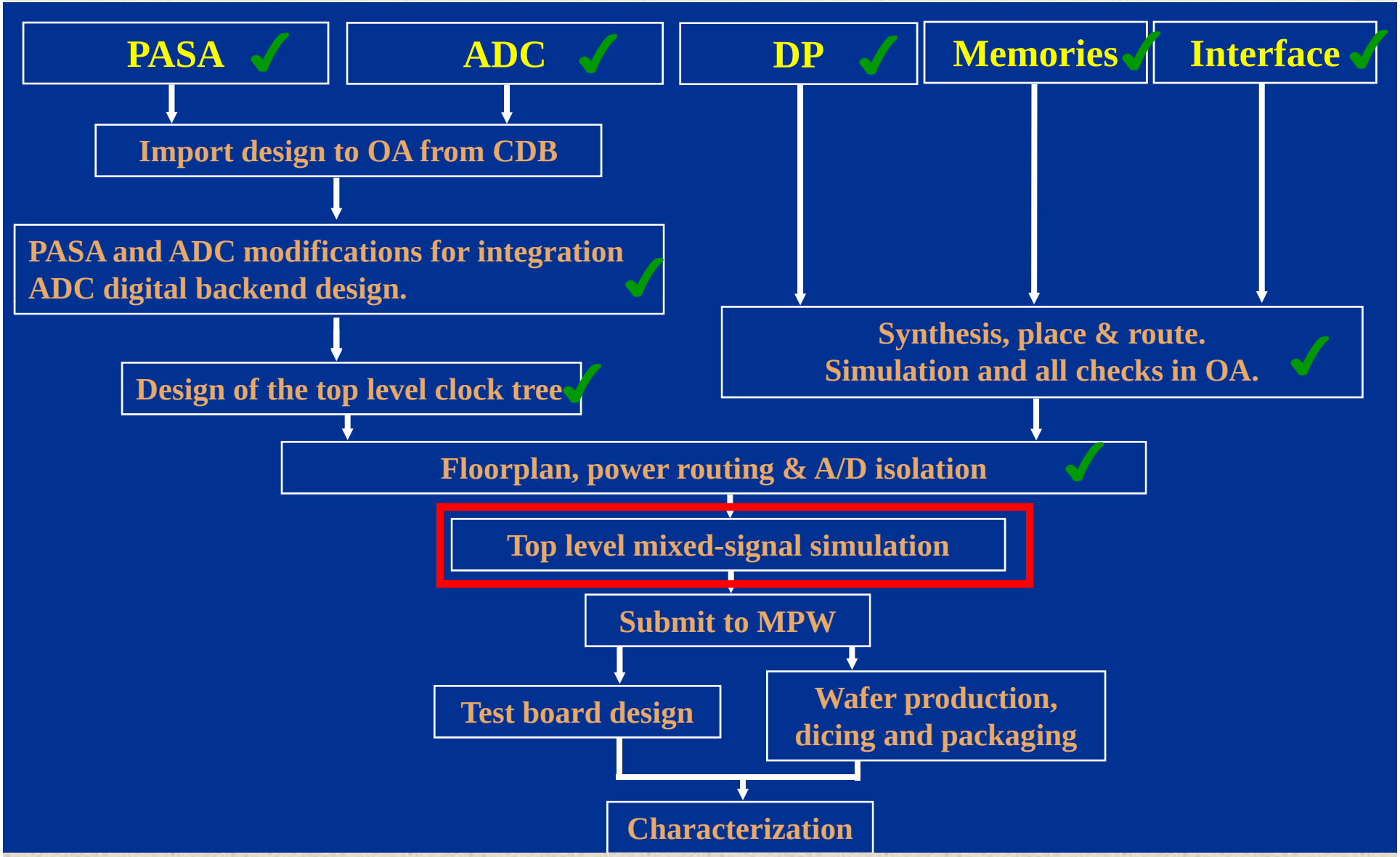
- **Functional test**



- **Back-annotated**

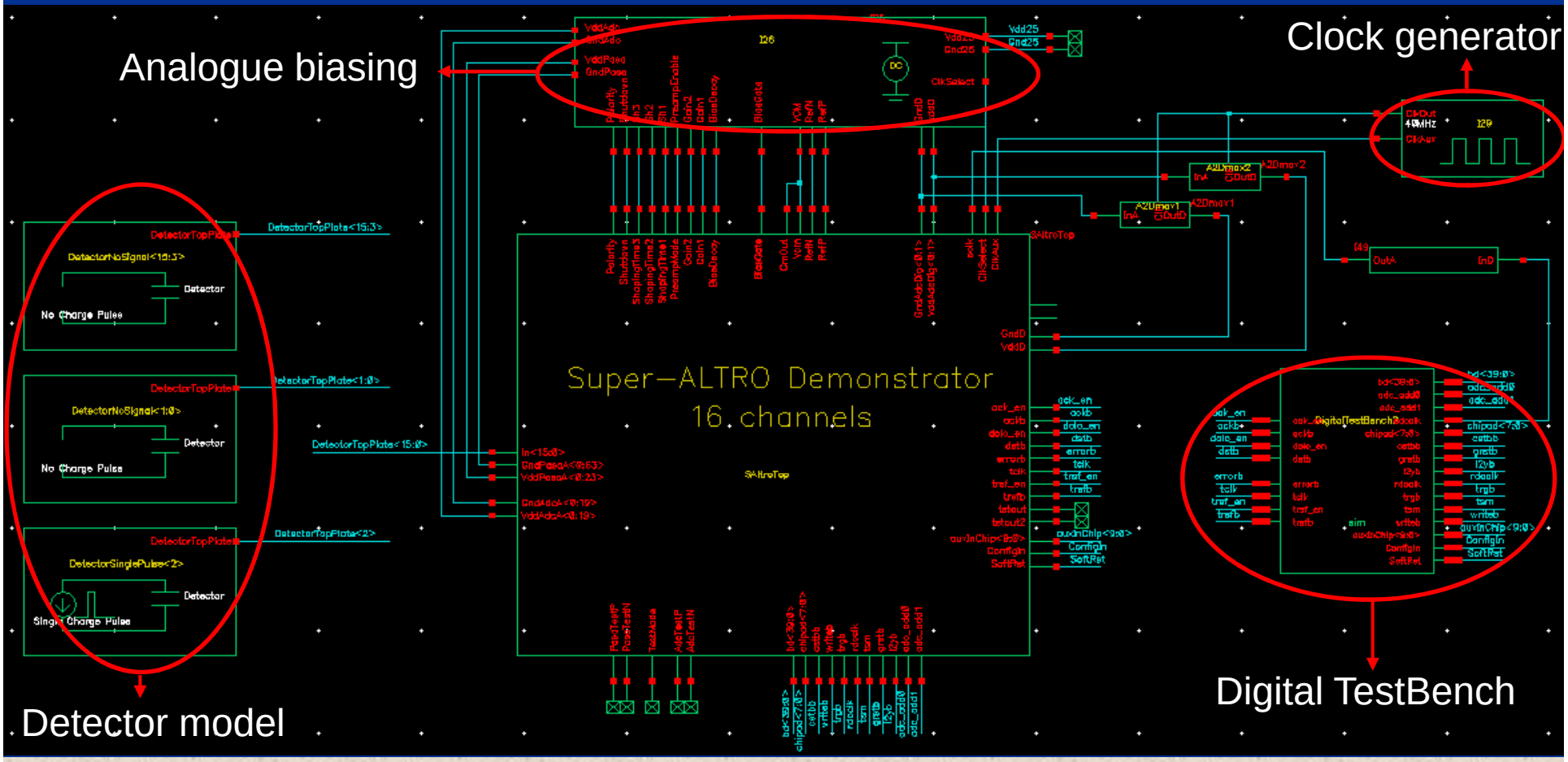


Demonstrator work flow



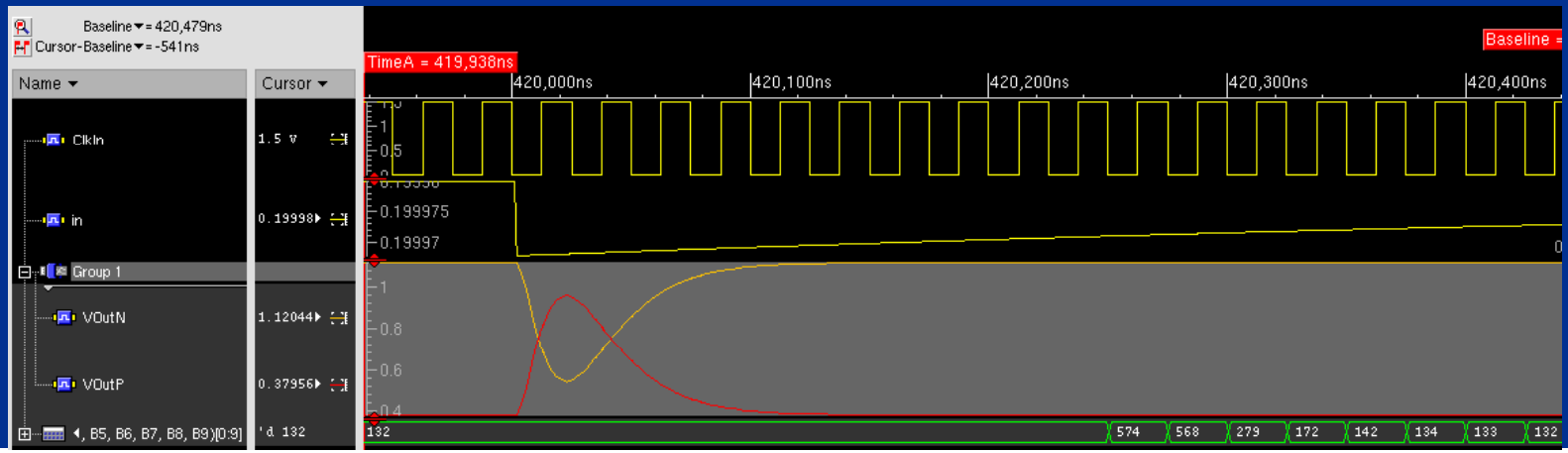
Mixed-mode simulation

- Objective: simulation of the full chain.
- Possible using verilog AMS and verilog descriptions.
- This example uses a very simple digital processing (input - 5 ADC counts).

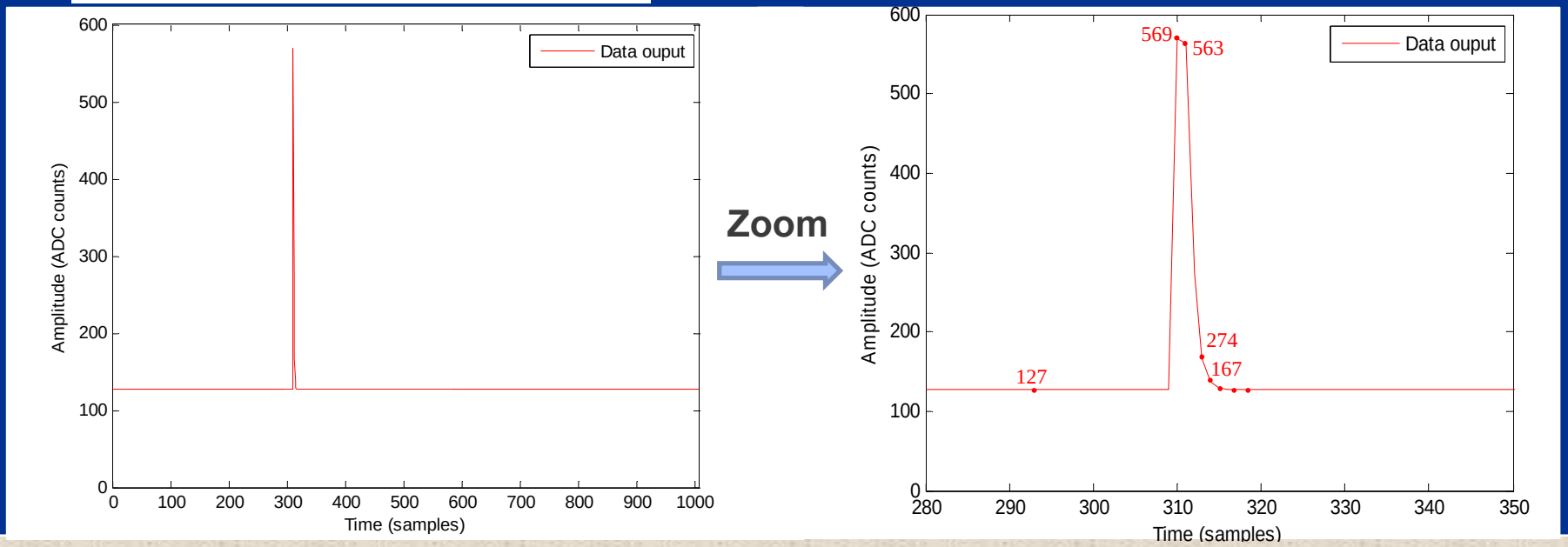


Mixed-mode simulation

- Output from simvision: external sclk, detector current pulse, PASA outputs, ADC output

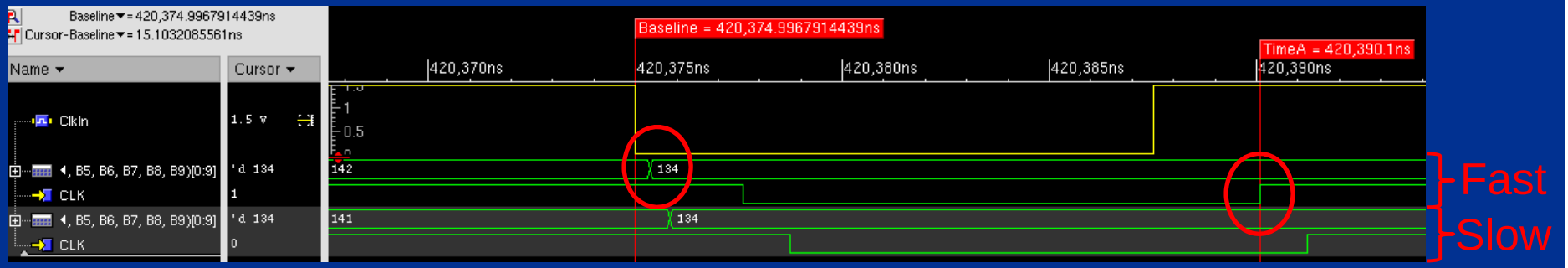


- Readout of one S-ALTRO channel



Mixed-mode simulation

Important issue: check the synchronization between the ADC output and the DP input including corners.



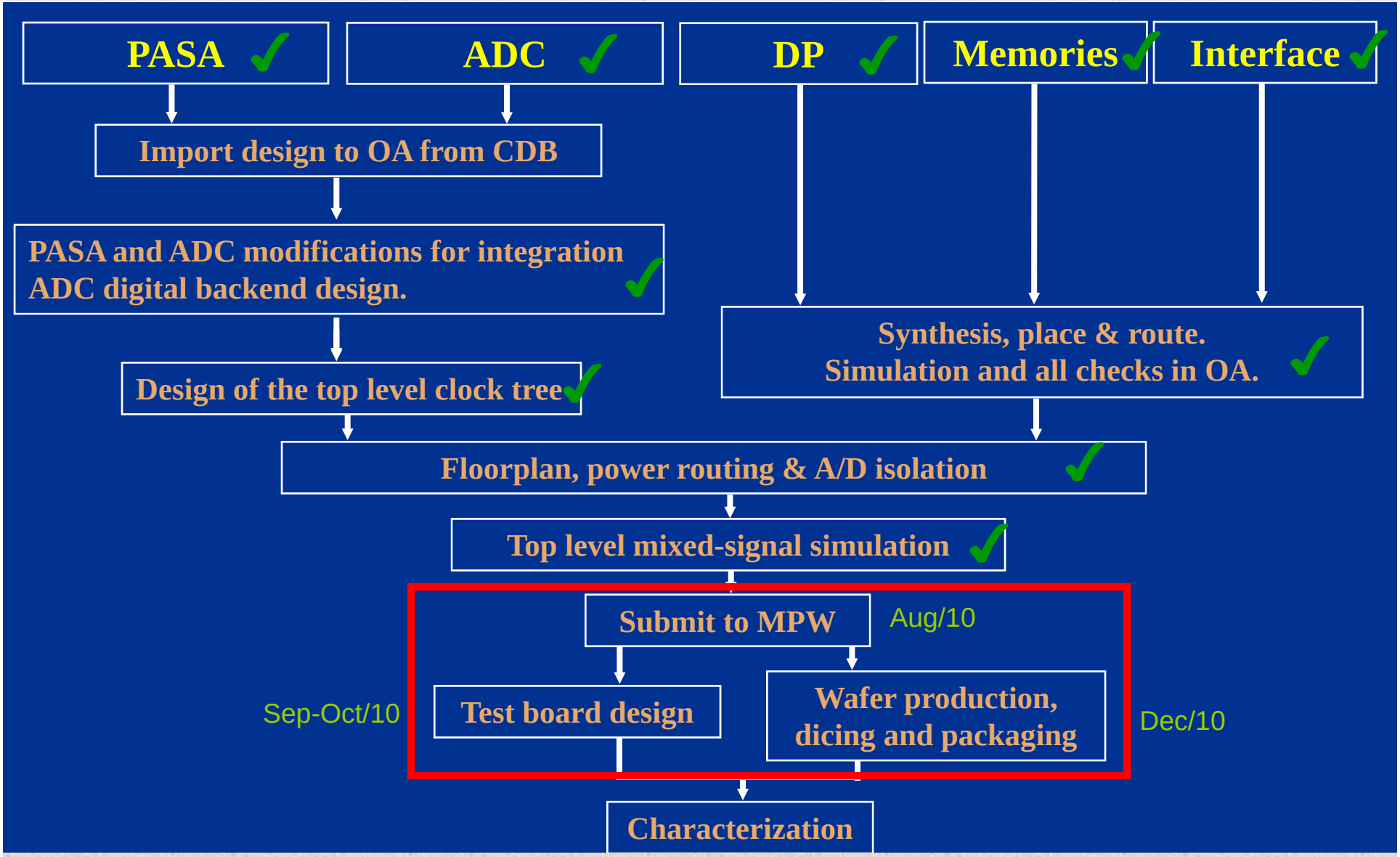
- External sampling clock
- ADC output
- Digital block internal clock register

Fast corner

- ADC output
- Digital block internal clock register

Slow corner

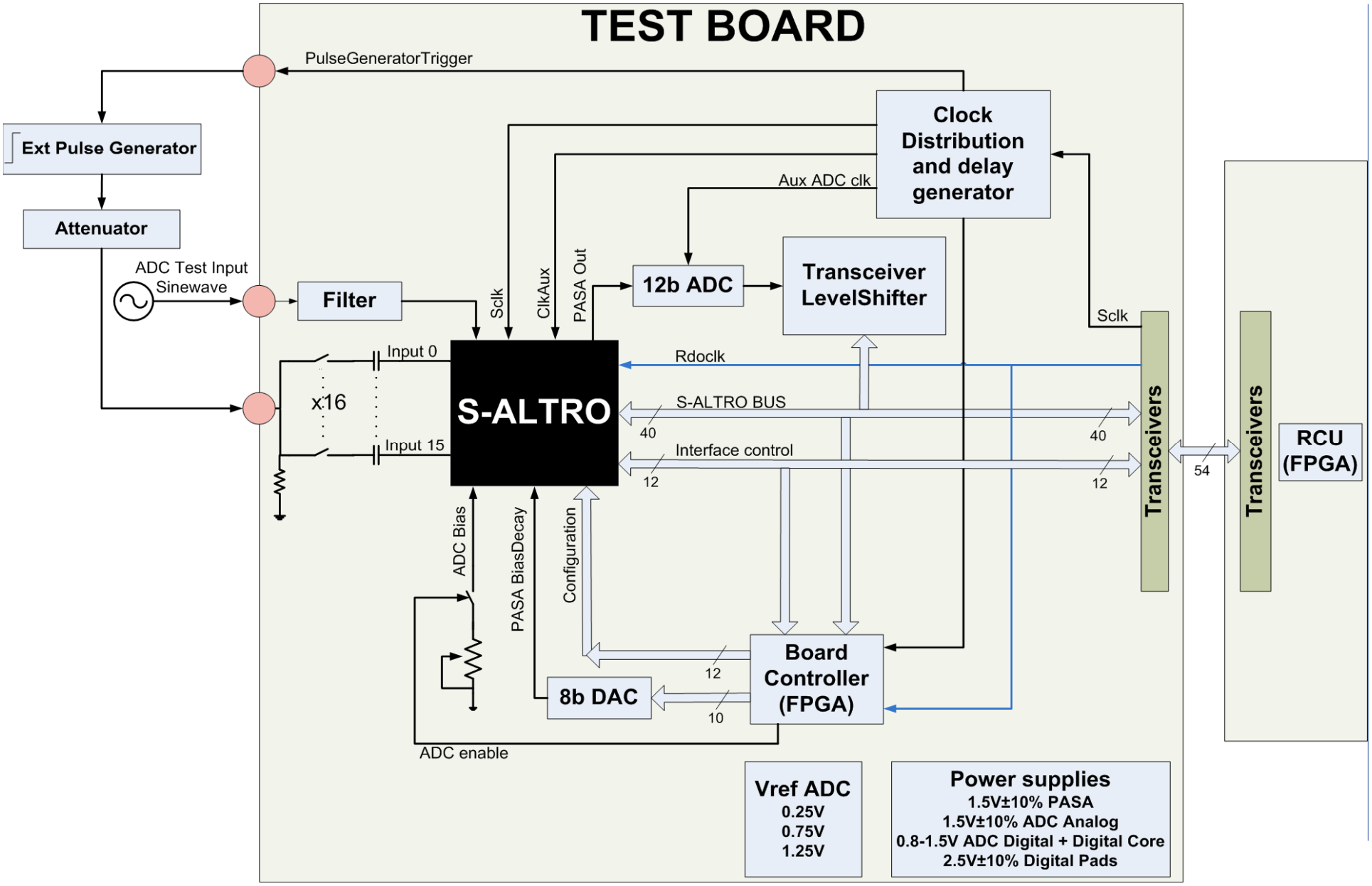
Demonstrator work flow



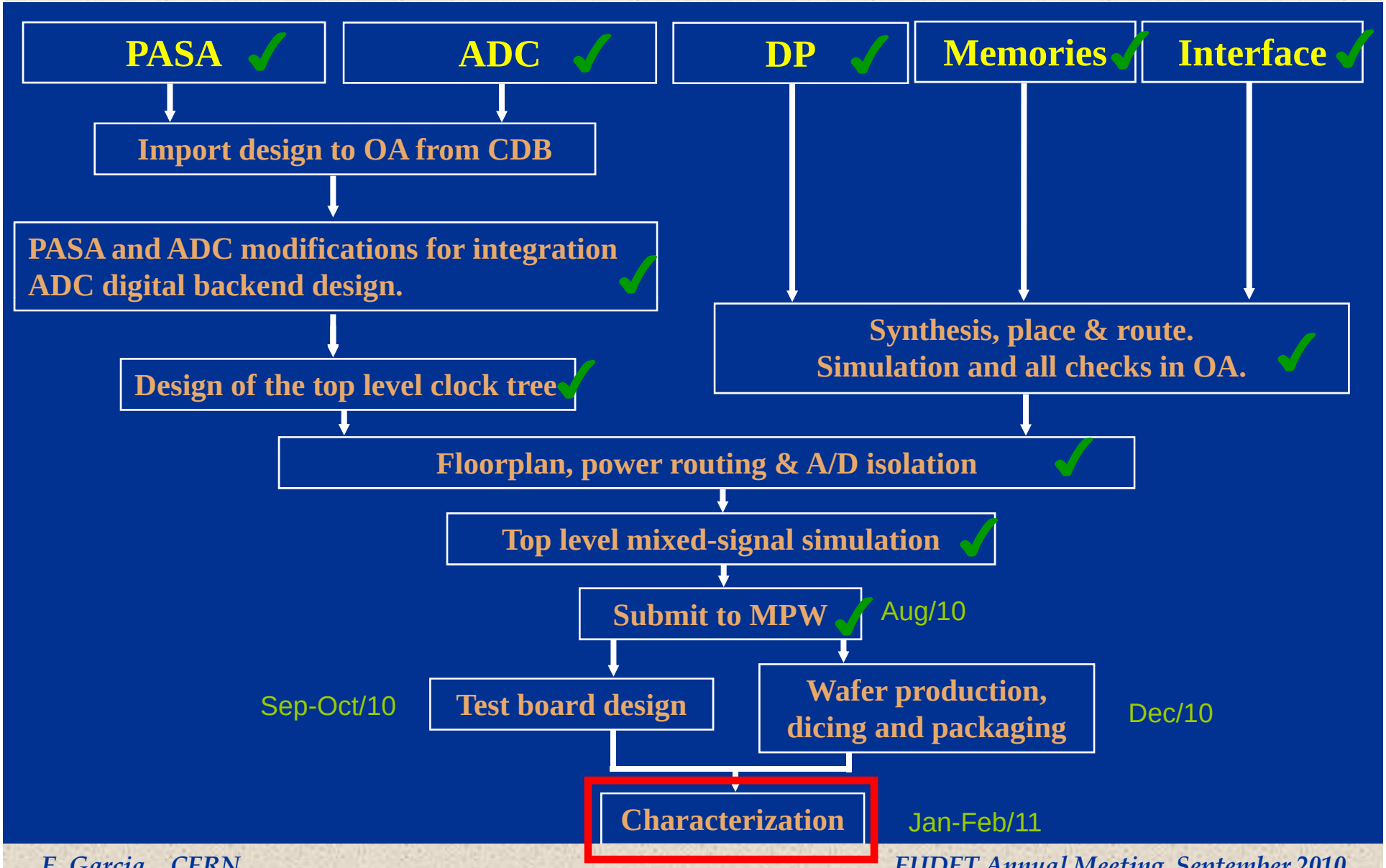
MPW submission

- Internal run at CERN sharing the MPW with other 20 different projects.
- For the moment just few samples will be packaged for characterization. Possibility of purchase 400 S-ALTRO demonstrators. More samples are available from the non fully processed wafers (upon request).
- Package: Thin Quad Flat Pack (TQFP-176), with pin stubs spaced at a pitch of 0.5 mm. The package body dimensions are 24 x 24 x 1.4 mm. The cavity for the silicon die is 12 x 12 mm.

Test board design



Demonstrator work flow



Characterization

- PASA (already characterized in a dedicated ASIC)
  - The S-ALTRO test channel will be used to test the functionality (programmable peaking time, gain) and measure the noise.
  - Check the power consumption with the other blocks disabled.
- ADC (already characterized in a dedicated ASIC)
  - Test the functionality using a sinusoidal input in the test channel.
  - Check the power consumption with the other blocks disabled.
- PASA + ADC
  - Test the functionality using the test channel.
  - Measure the noise & compare with the PASA alone.
  - Check the power consumption of the analog part.

Characterization

- Digital Block
  - Test of the digital functionality.
  - Check the power consumption depending on the filter configuration and core power supply. PASA and ADC will be disabled.

- PASA + ADC + Digital Block
  - Test of the functionality of the full chain.
  - Measure the Noise:
    - Study of the digital switching noise introduced in the analog sensitive part.
  - Check the Power consumption
    - Normal mode.
    - Low power mode (some digital block disabled).
    - Power pulsing.