Front-end and integration of the 16-channel S-Altro Demonstrator

People :

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Eduardo Garcia ….. Data Processing & Control

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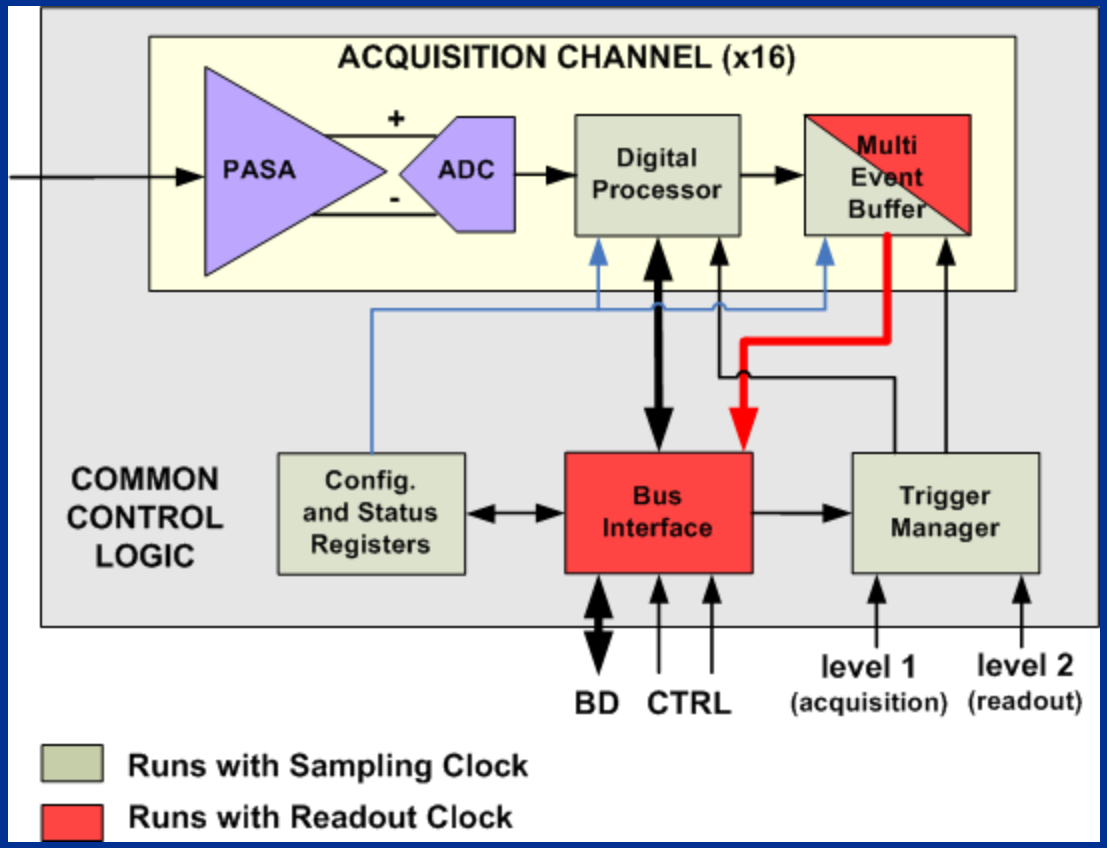
S-Altro architecture



Read-out of gaseous detectors with MWPC, GEM, Micromegas

S-Altro Demonstrator

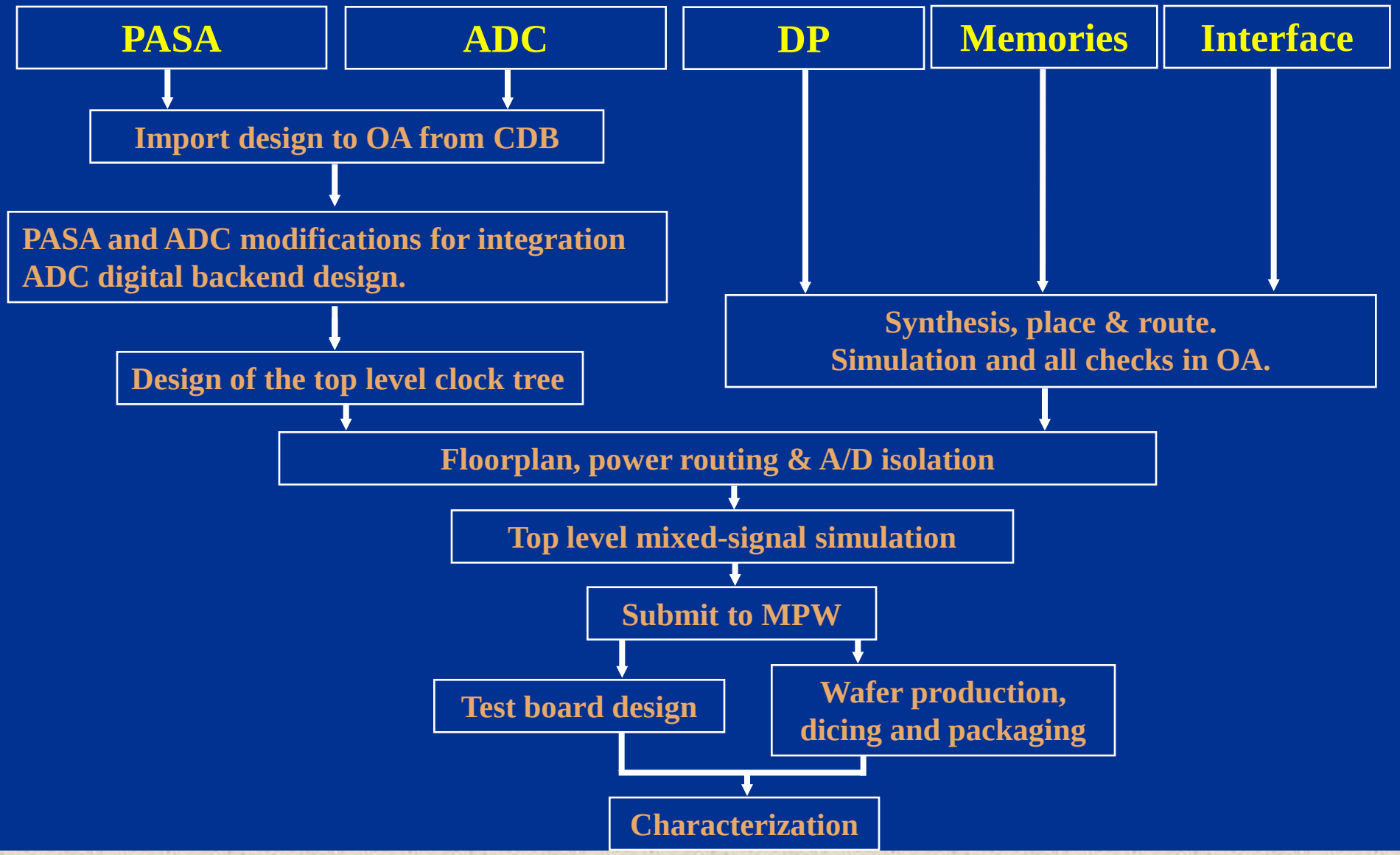
Goal: Integration of a low-noise preamplifier/shaper, an ADC and digital signal processing in a single chip.

Process: IBM 130nm CMOS 8RFDM
Metal stack 3-2-3

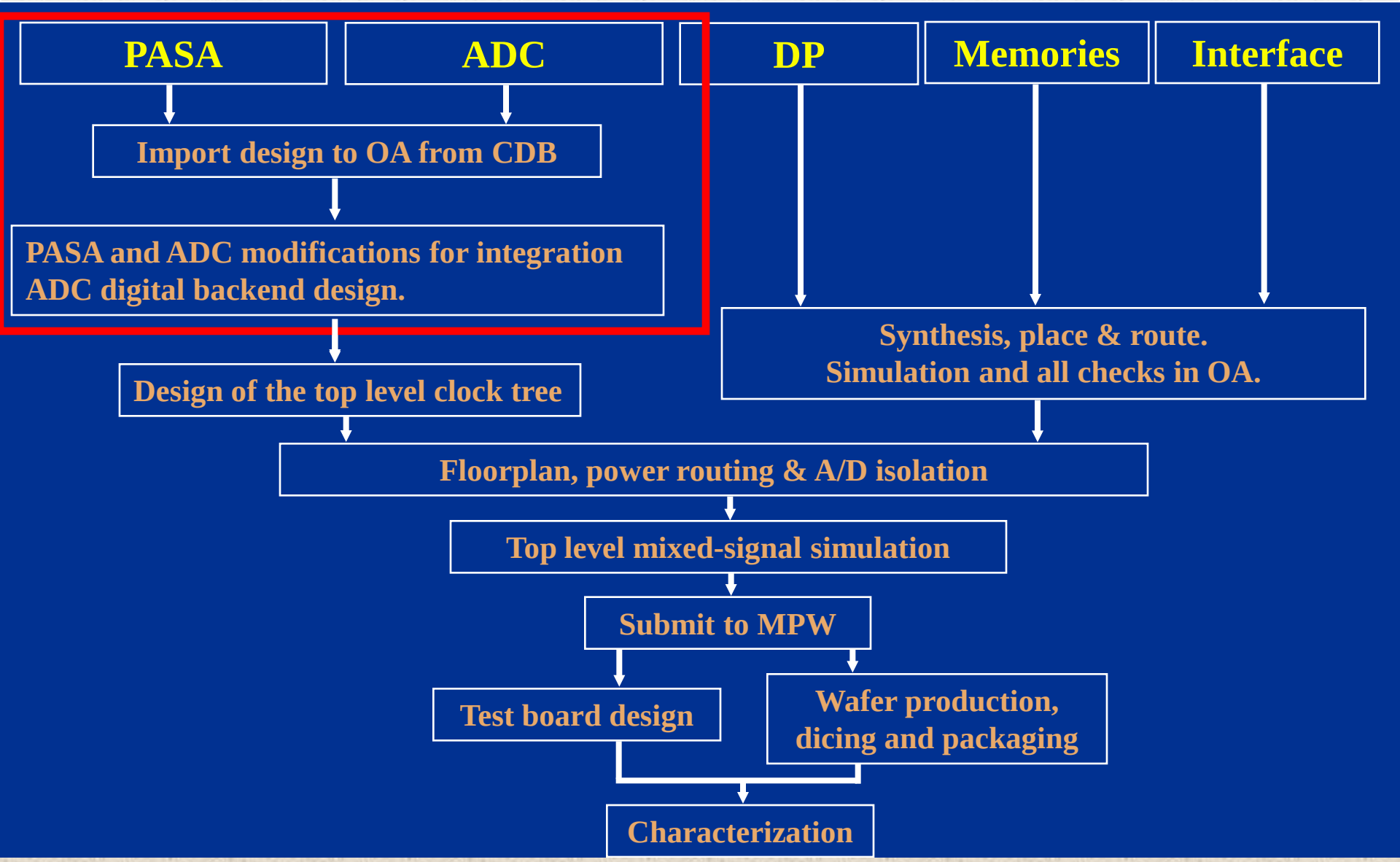
Cadence / VCAD Open Access (OA) design database
➔ Import designs from the "old" CDB database and verify them

Tape-out: CERN MPW, cost \$2K/mm^2

Demonstrator work flow

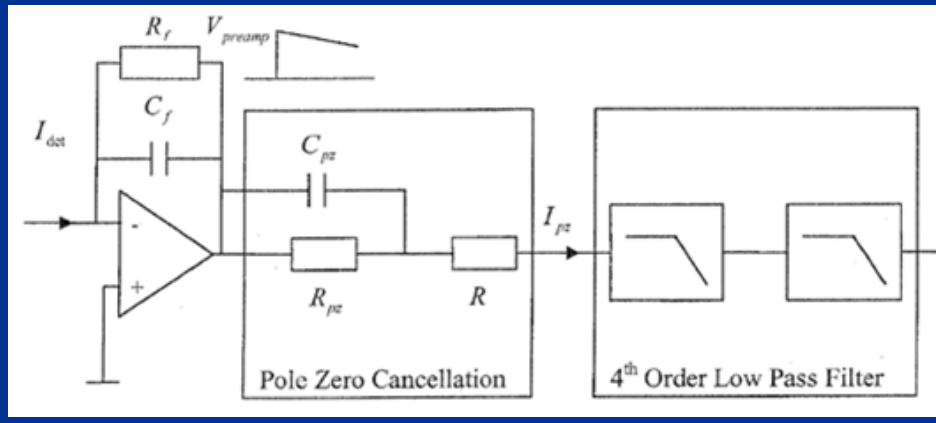


Demonstrator work flow

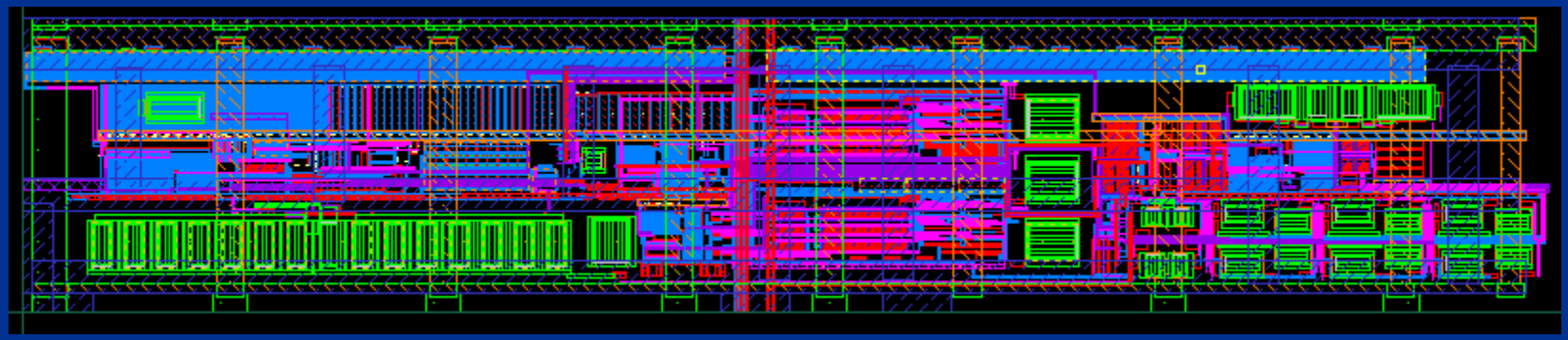


Preamplifier/Shaper

- Single-ended input, differential output
- Programmability options:
  - Polarity switch
  - Shutdown switch
  - Preamplifier enable
  - Gain control (2 bits: 12-27mV/fC)
  - Shaping time control (3 bits: 30-120ns)
  - Bias decay (analog)



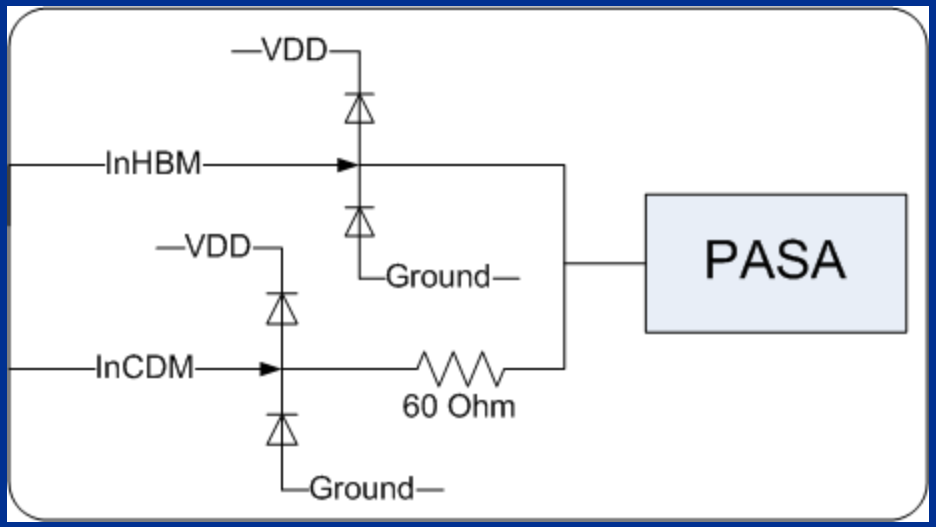
Size: 1100um X 210um **Power: 8.4mW/channel** **Supply: 1.5V**



PASA: ESD protections

Each PASA has two input pads in parallel (only one bonded):

- **Simple double diode protection scheme (Human Body Model)**
- **Structure with series resistor for enhanced protection (Charged Device Model)**

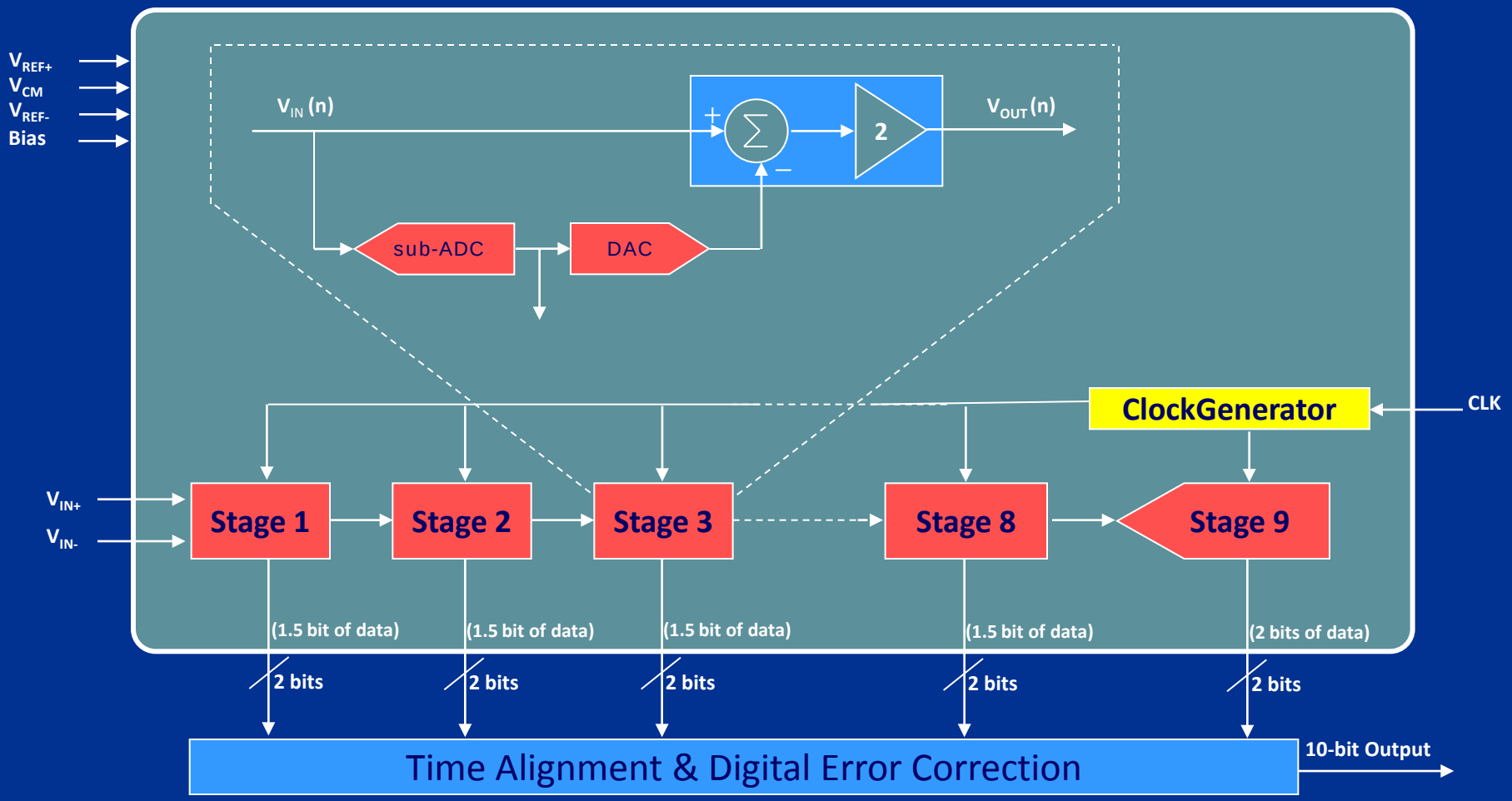


Drawback: the series resistor adds noise to the input signal.

PASA noise: 300e^- @ 10pF detector capacitance

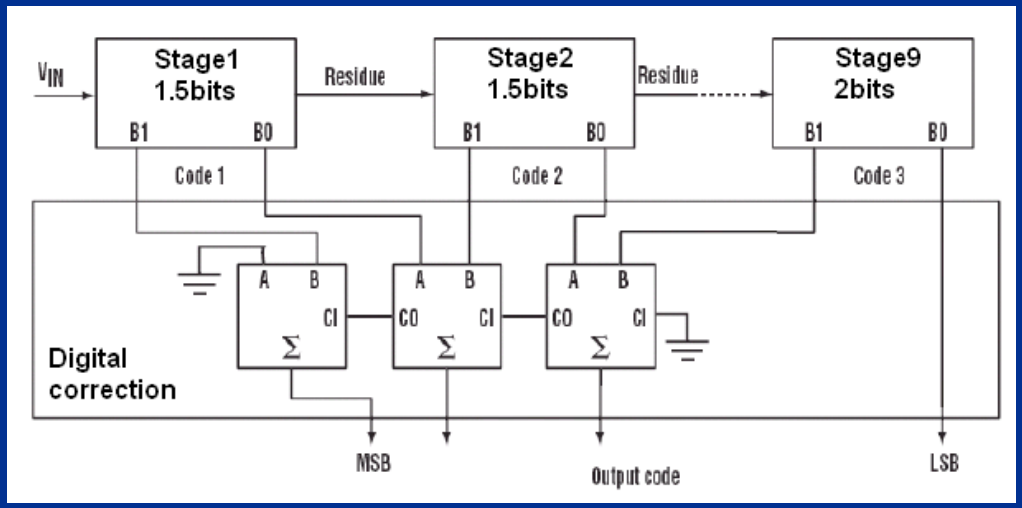
Expected noise increase (simulated): 20-30%

Pipeline ADC



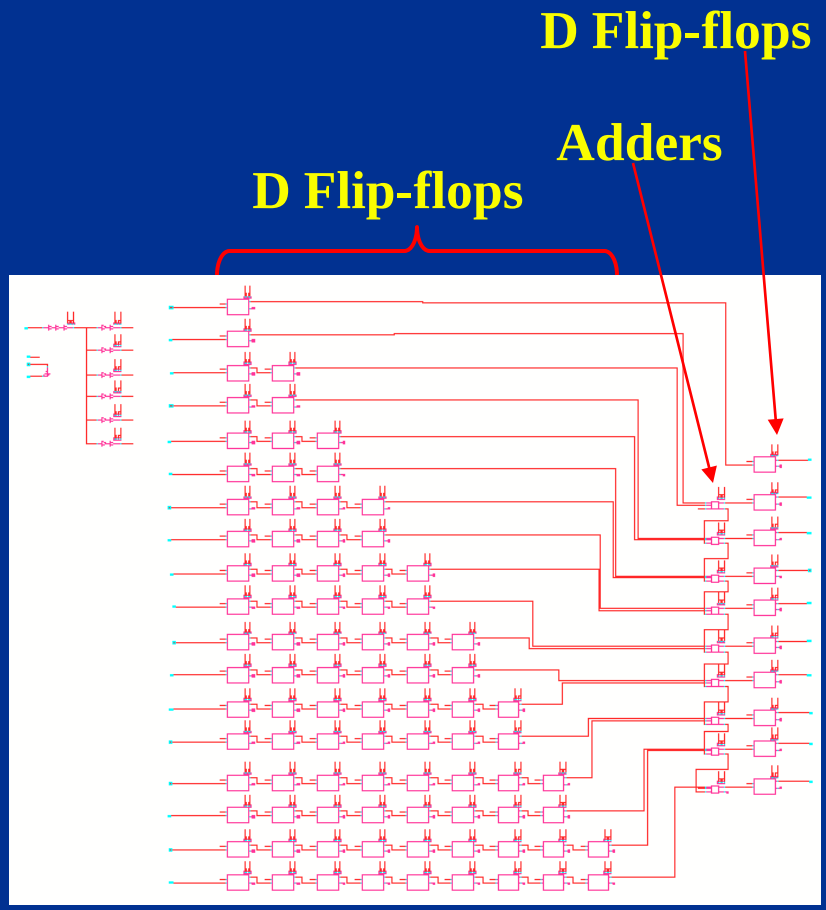
10bit, optimized for 40MHz, 1.5V supply, 34mW power (without stage scaling), 0.7mm^2 area

Digital error correction (redundancy)



18 bits from the 9 ADC stages are reduced to a 10-bit output word.

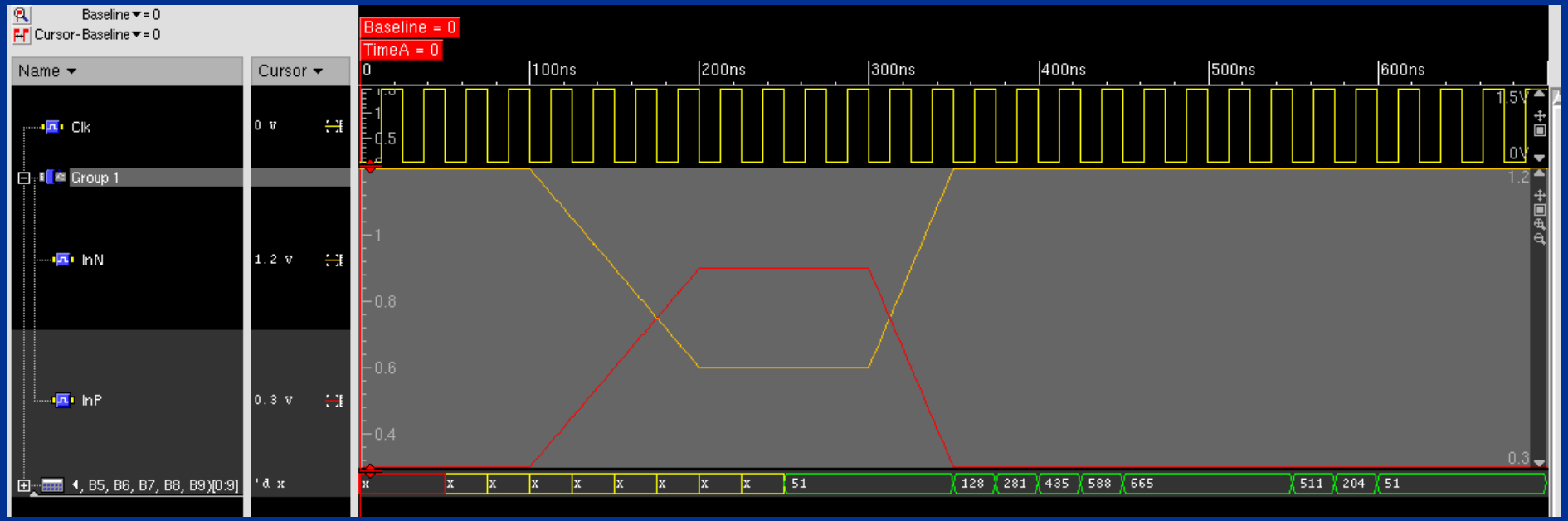
The digital correction is clocked on the falling edge of the clock.



Delays (buffers) not shown

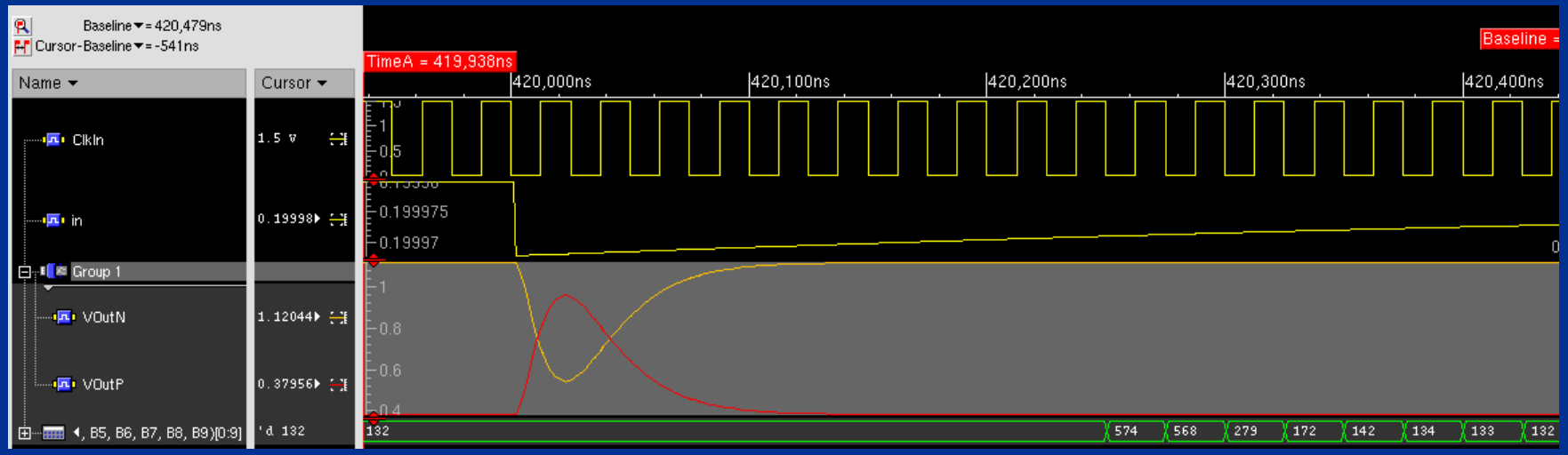
Digital error correction: verification

In order to run chip-level simulations, an analytical Verilog-AMS model has been written and verified for each block.



Arbitrary analog input waveform converted to digital simulated in Spectre (schematic, extracted parasitics, extreme corners and Monte Carlo) and in Verilog-AMS: results correct

Verilog-AMS model

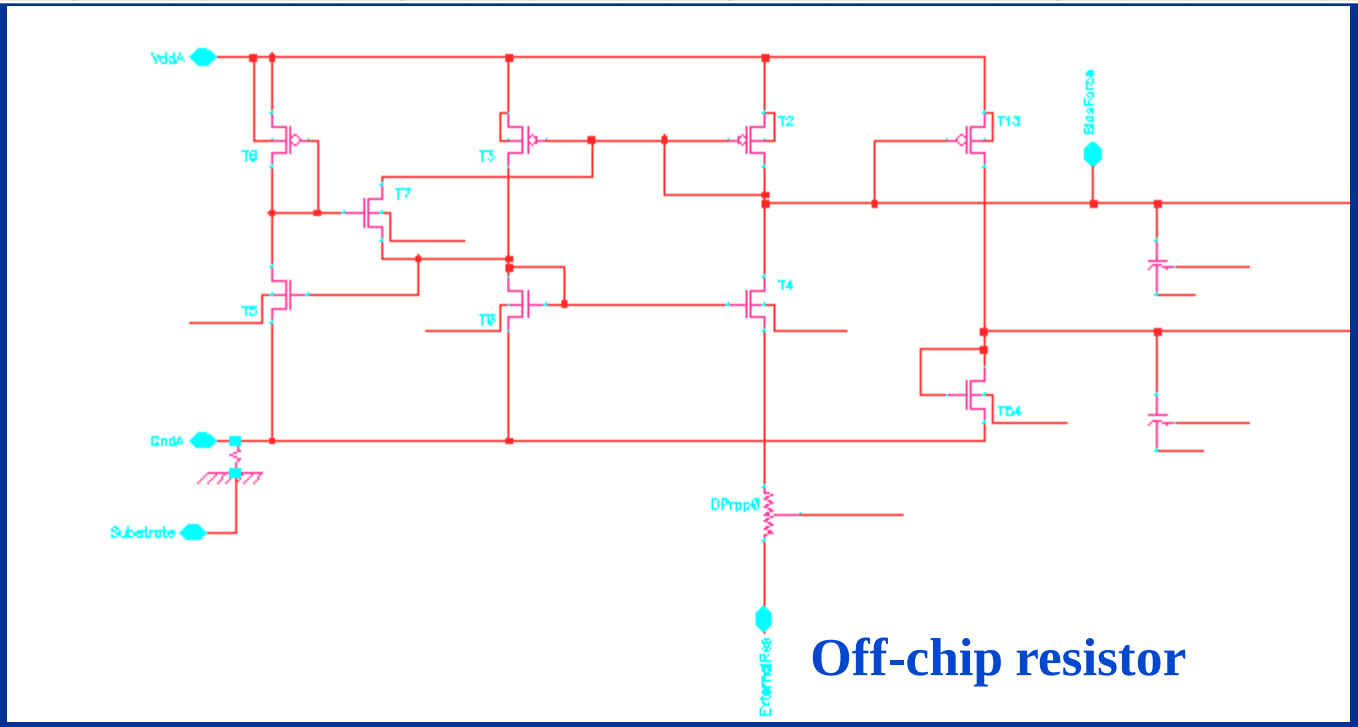


Verilog-AMS model developed for the PASA and the ADC.

PASA: the model produces waveforms similar to the schematic simulations

ADC: the model was verified to produce the same results, with the same latency, as the schematic.

Bias circuitry (beta-multiplier)

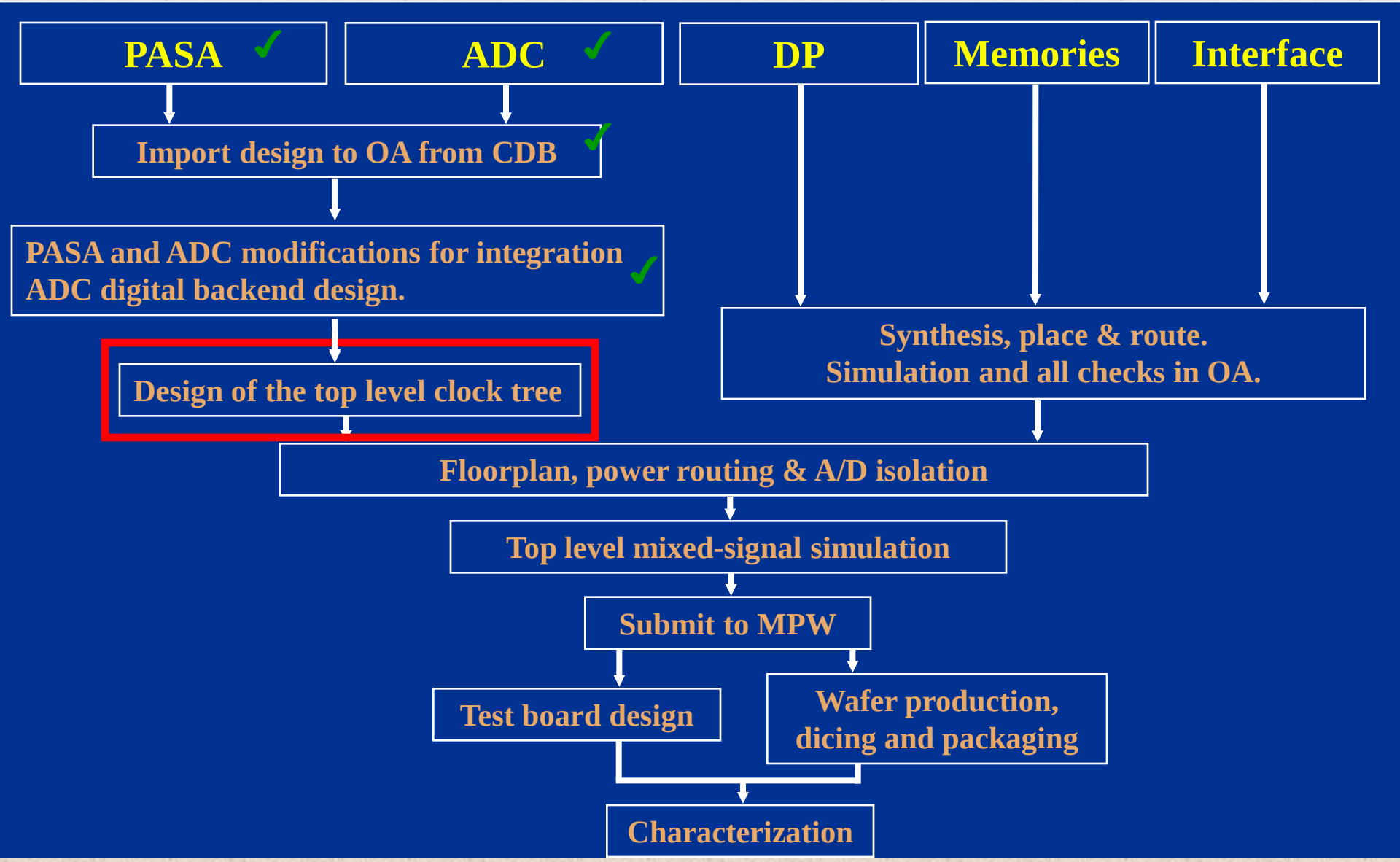


The off-chip resistor is meant to adjust externally the power consumption of the ADC (useful for different sampling frequencies and to test power-pulsing)

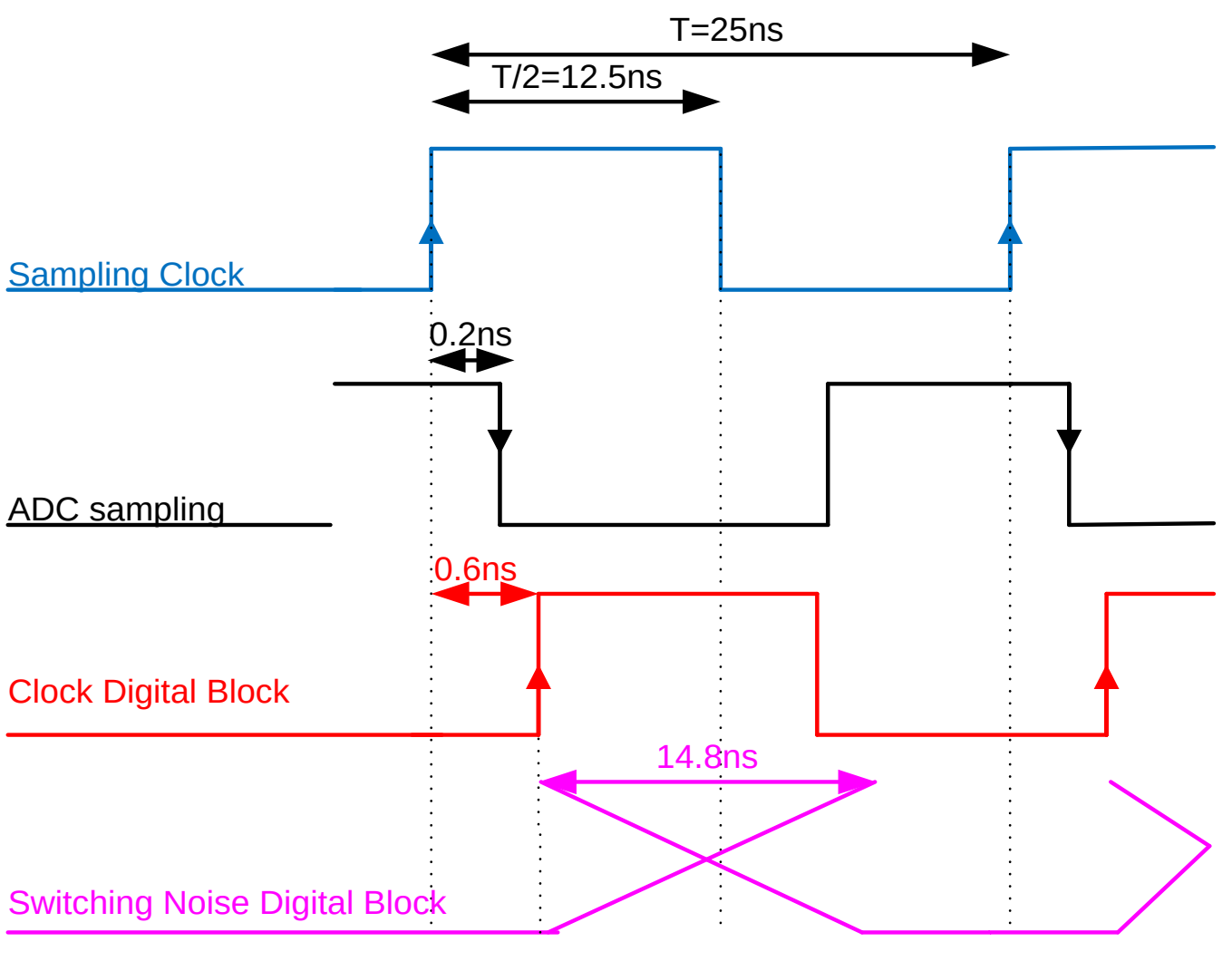
ADC prototype: 1 beta-multiplier per ADC + 1 off-chip resistor per ADC

SAltro: 1 beta-multiplier + 1 off-chip resistor + the BiasReference signal is routed to all channels

Demonstrator work flow

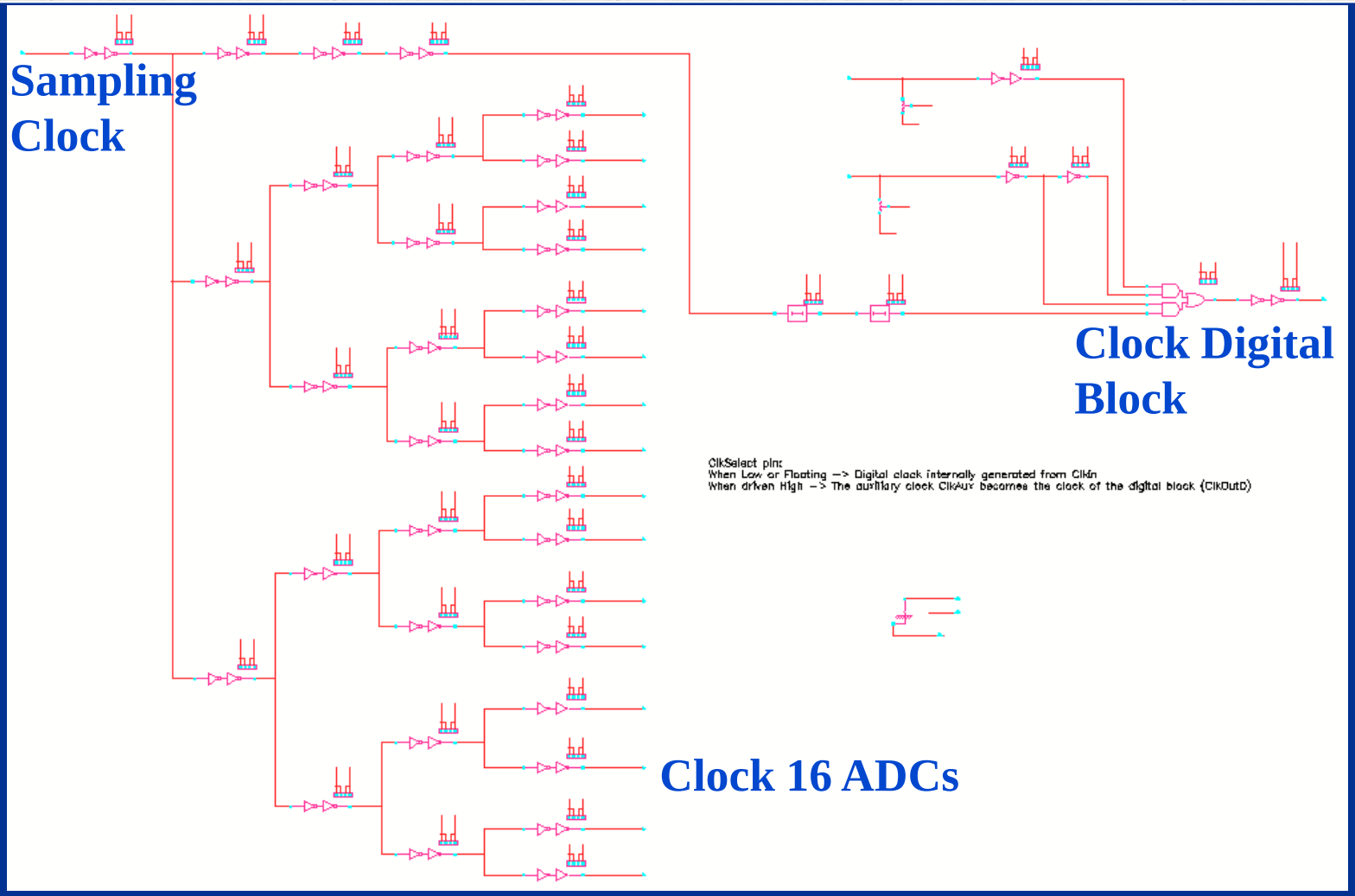


Clocking scheme



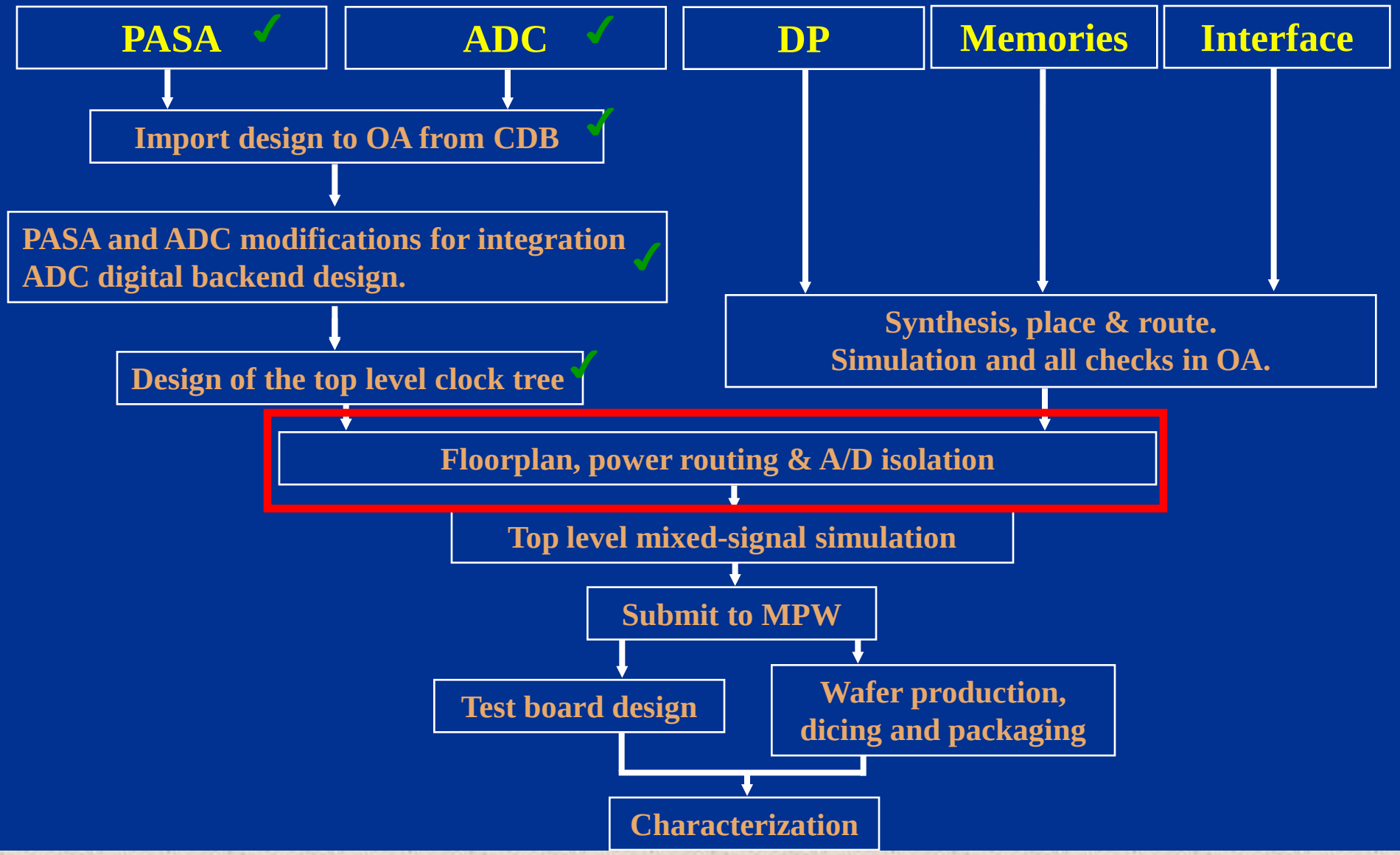
Shown in red shading: part most sensitive to noise

Clock Tree: design

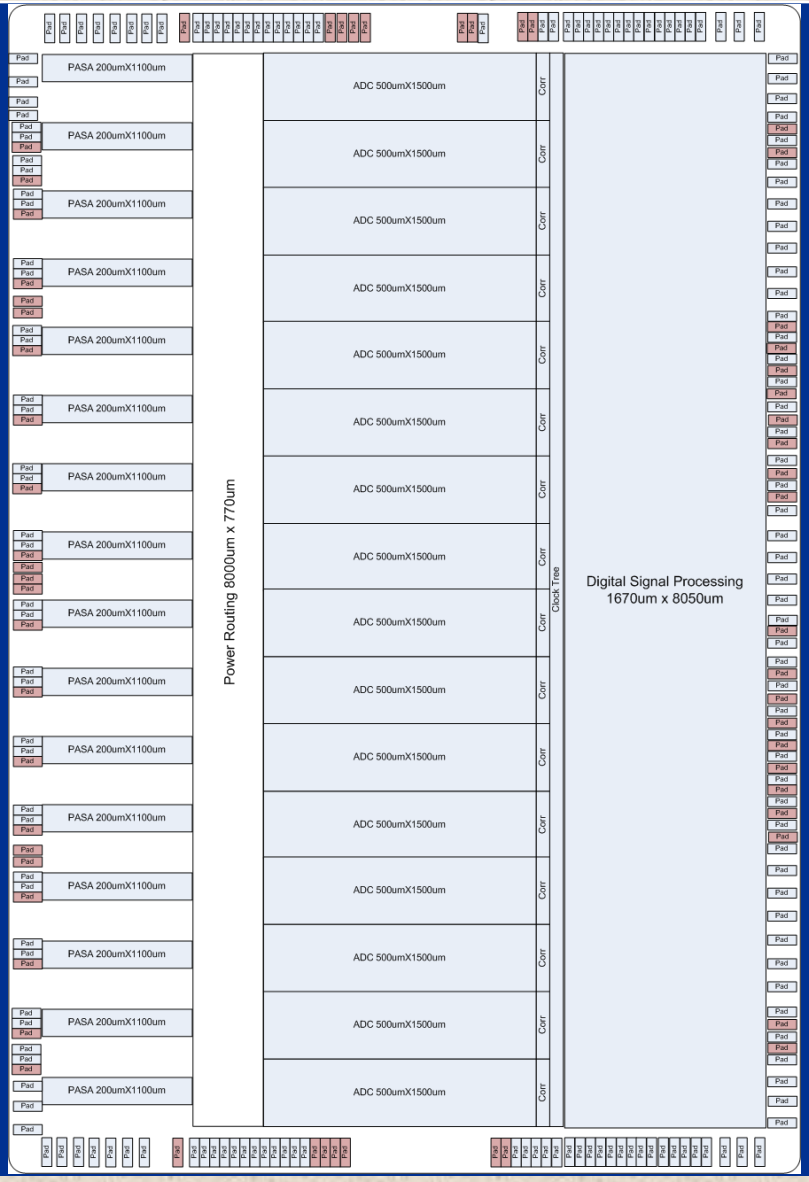


Buffer the clock to the 16 channels, deliver a delayed clock (typical: 600ps) to the digital block. Fully symmetrical structure (also in layout).

Demonstrator work flow



S-ALTRO Demonstrator Floorplan



16-channels:

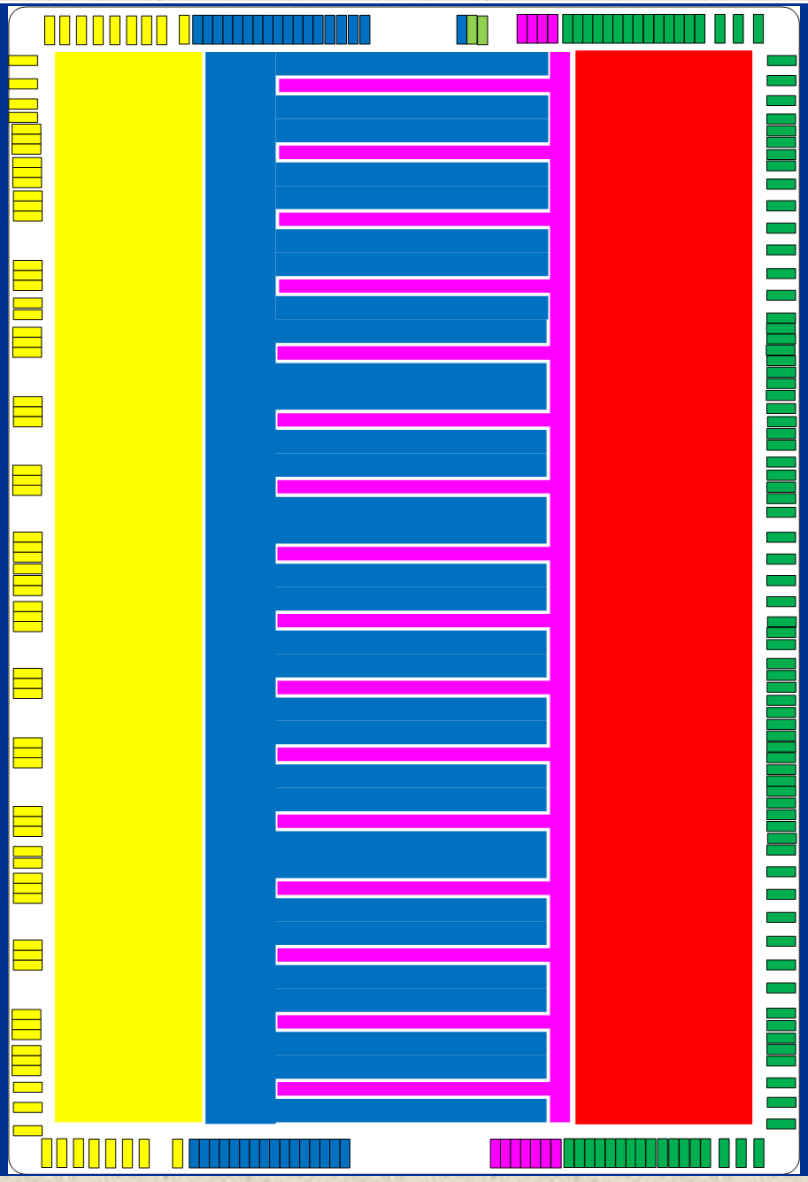
PASA **210um X 1100um**

ADC **500um X 1500um**

Digital Signal Processing
1670um X 8050um

The wide power routing ensures low IR power supply drop (10mV for the ADC)

Power domains



Power domains:

PASA analog

ADC analog

ADC digital

Digital core

Digital Pads

Power supply decoupling capacitors:

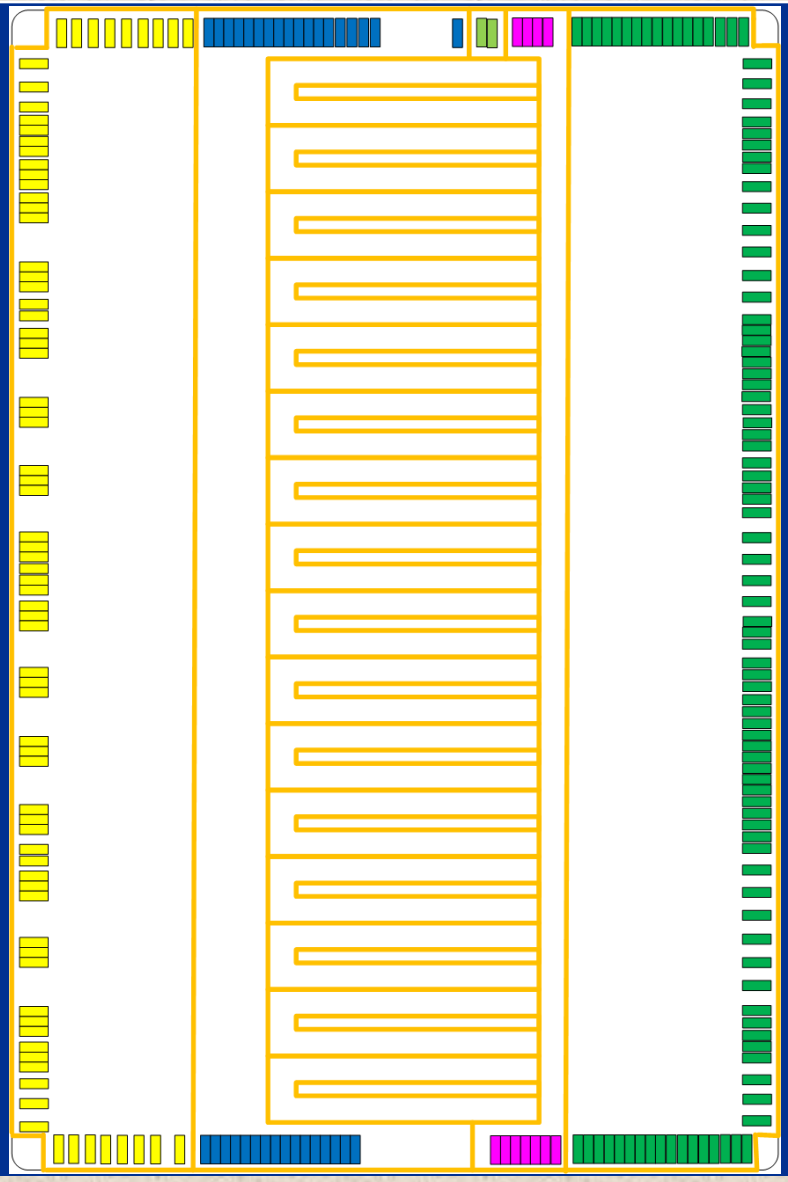
600pF /channel PASA

600pF /channel ADC analog

40pF /channel ADC reference voltages

80pF/channel ADC digital

Substrate partitioning with BFMOAT

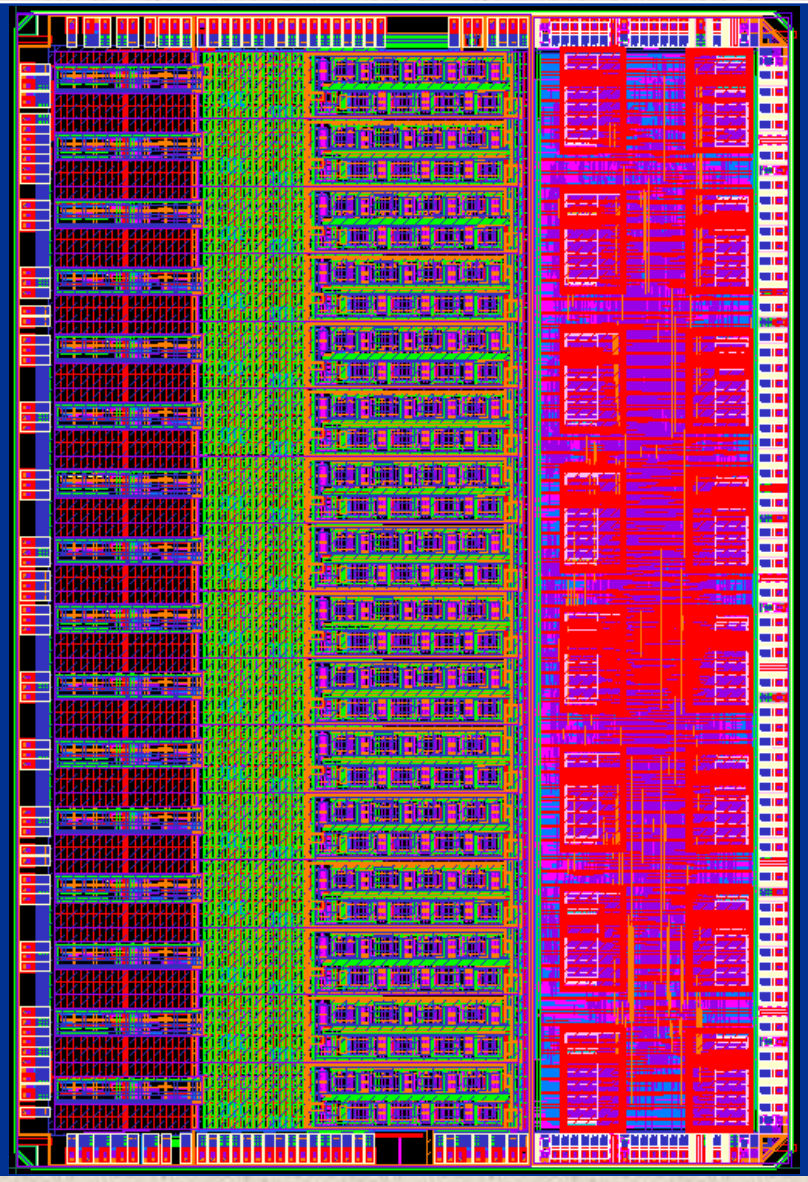


BFMOAT: high resistivity (p^-) substrate region, placed between different power domains to insulate them from each other.

The effective substrate resistance between adjacent regions depends on the width and perimeter of the BFMOAT layer.

NW/P+ guardrings on both sides of the BFMOAT implants.

Layout



Size: 5750um x 8560um
(49.22mm^2)

Demonstrator work flow