



TLU Status and Plans



Outline

- Summary of EUDET TLU experience
- “Pseudo-tagging” trigger mode
- Wish-list
- Plans (AIDA).
- Conclusions.



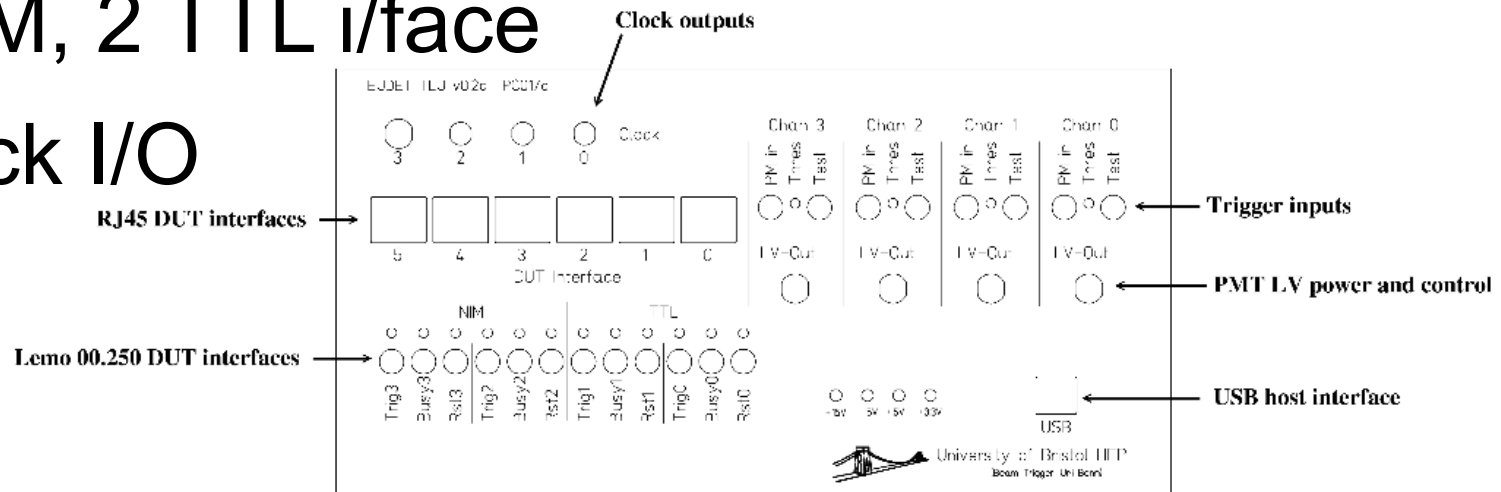
Summary

- TLU aims to provide a common trigger/timing interface to beam telescope
 - Users can integrate in their own labs before beam-test
- Provides time-stamp
 - Currently only for first particle in each telescope frame.



Summary

- TLU v0.2c the last EUDDET TLU model that will be produced.
 - 4 trigger inputs
 - 6 RJ45 DUT i/face
 - 2 NIM, 2 TTL i/face
 - 3 clock I/O





Summary

- TLU widely used:
 - DESY and CERN beam-test areas
 - In “users” labs to prepare for beam time.
 - ~ 15 units produced in total
- Hardware, Firmware, Software work reliably
 - (Subject to suitable definition of reliable)
 - Still some remaining issues.



Pseudo Tagging Mode

- FORTIS DAQ continuously active.
 - DAQ reads out all data.
- FORTIS Readout f/ware modified to record every trigger that arrived.
 - Simple trigger/busy handshake used.
(Trigger looped back to busy at FORTIS)



Pseudo Tagging Mode

- If data transfer to EUDAQ stalls, FORTIS DAQ buffers fill.
 - FORTIS firmware modified to raise “DUT_Clock” line when buffer about to fill
 - TLU firmware modified to veto triggers
 - selectable on DUT-by-DUT basis.
- Can be multiple triggers per frame.
- Could be applied to Mimosa readout.



Wish List

● Suggestions from users

- Extra trigger inputs (J. Velthuis)
- ~ Zero dead-time (P. Colas et. al.)
 - Could be done with existing h/ware & new f/ware
- Timestamp every particle (M. Winter et. al.)
 - Could be done by firmware change on existing h/ware but would benefit from faster FPGA and link
- More TLUs
 - Implies cheaper easier to assemble TLU



Plans

- Base AIDA TLU around a newer CoTS FPGA board.
 - Probably Xilinx SP605 (Spartan 6)
 - Trigger logic clock 200MHz (cf. 50Mhz). Higher trigger throughput.
 - Use hardware “deserializers” to improve TDC
 - Use Gbit/s Ethernet as link to host.
 - Soft-core processor.
- Use work being done for CMS upgrade.
 - e.g communication with host.



Plans

- “Full A-TLU” would look very similar to current model:
 - Six trigger inputs (cf. 4).
 - Fixed threshold discriminator with ADC to correct timing walk.
 - Lower latency ($<10\text{ns}$ cf. $\sim 25\text{ns}$)
 - Keep RJ45 inputs (not an ideal connector, but keep compatibility with EUDET TLU)
 - Keep TTL, NIM I/O.
 - Front-end firmware very similar.



Plans

- “Mini TLU”
 - Use a prototype for new h/ware.
 - Use as lightweight TLU for users to integrate against.
 - Two trigger inputs.
 - Two RJ45 DUT I/O.
 - Single TTL DUT interface (Trigger, Busy, Clk)
 - Use new Xilinx sponsored “FMC” connector.
 - Interface identical to full TLU.



Conclusion

- **EUDET TLU works.**
 - Provides a standard trigger interface to EUDAQ and beam-telescope.
- **AIDA TLU - same DUT interface to as EUDET TLU.**
 - Reduce firmware development time.
 - Reduce s/ware development time.
 - Users won't have to change anything to swap from EUDET to AIDA TLU