TLU Status and Plans

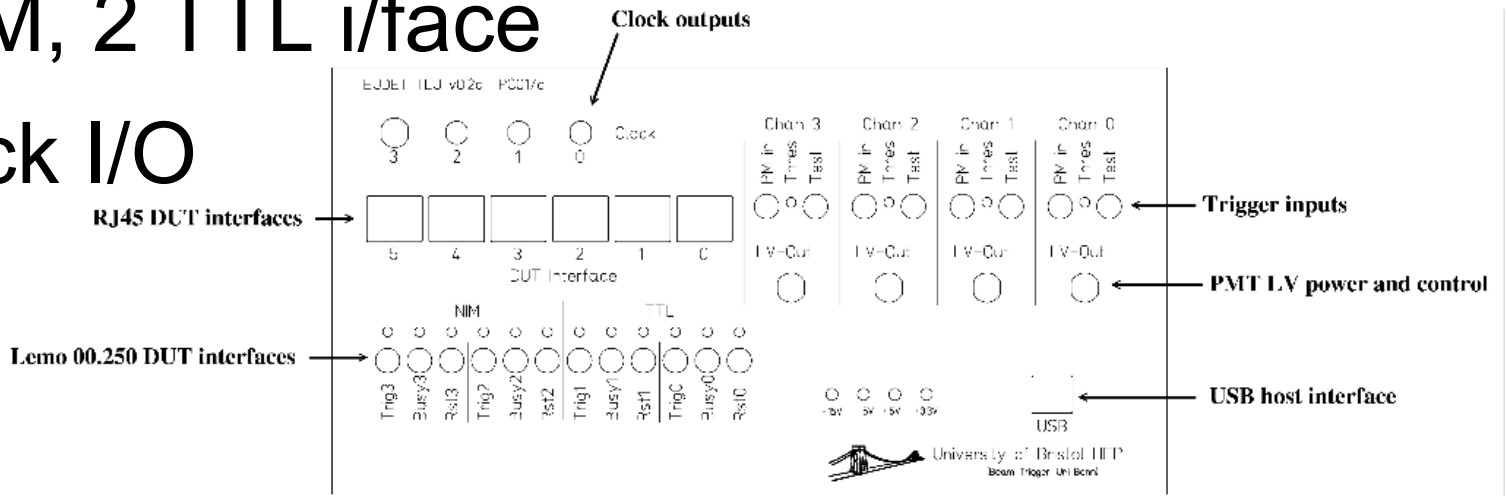
David Cussans, DESY, September 2010

Outline

- Summary of EUDET TLU experience
- Remaining “issues”
- Wish-list
- Plans (AIDA).
- Conclusions.

Summary

- TLU v0.2c the last EUDET TLU model that will be produced.
  - 4 trigger inputs
  - 6 RJ45 DUT i/face
  - 2 NIM, 2 TTL i/face
  - 3 clock I/O



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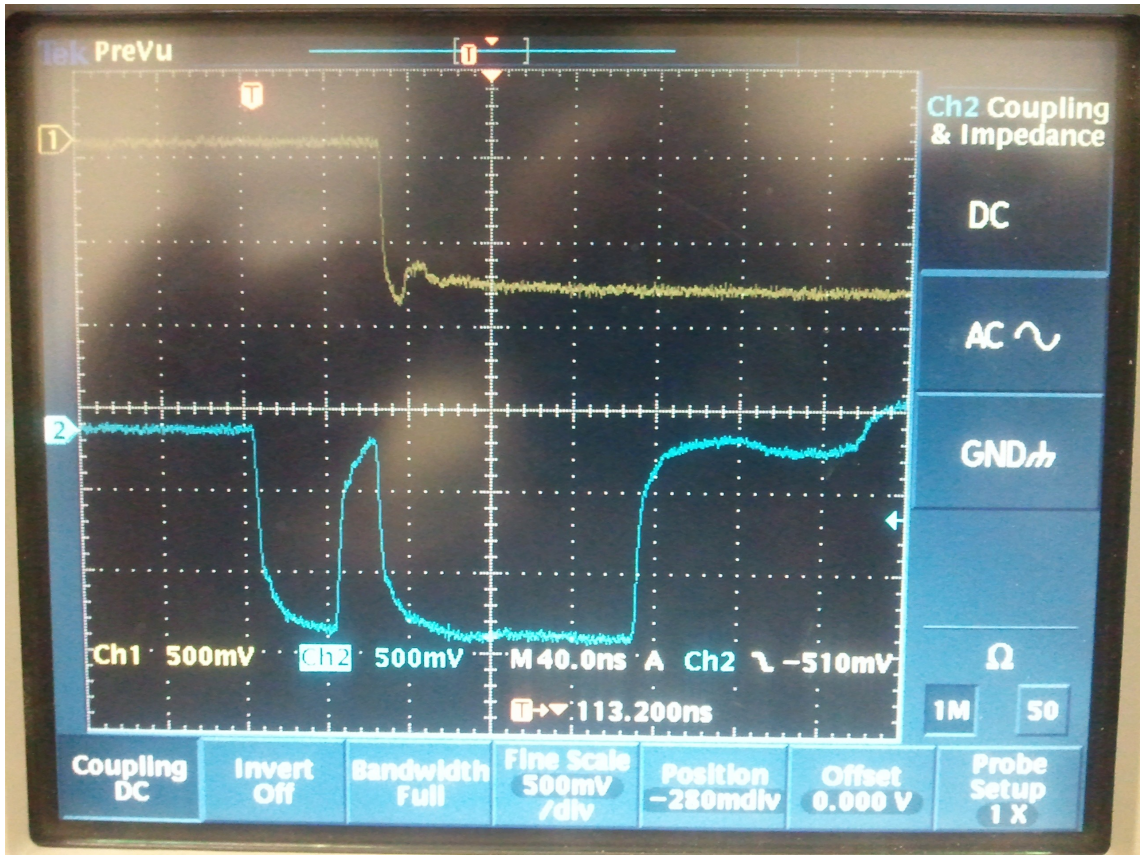
Summary

- TLU widely used:
  - DESY and CERN beam-test areas
  - In “users” labs to prepare for beam time.
  - ~ 15 units produced in total
- Hardware, Firmware, Software work reliably
  - (Subject to suitable definition of reliable)
  - Still some remaining issues.

Remaining Issues

- Asynchronous logic still causing issues:
  - (Thanks to Artem Kravchenko@DESY for this report):



* Blue – TLU Trigger(NIM)
* Yellow – DUT Busy(NIM)

Trigger should stay asserted – not glitch low

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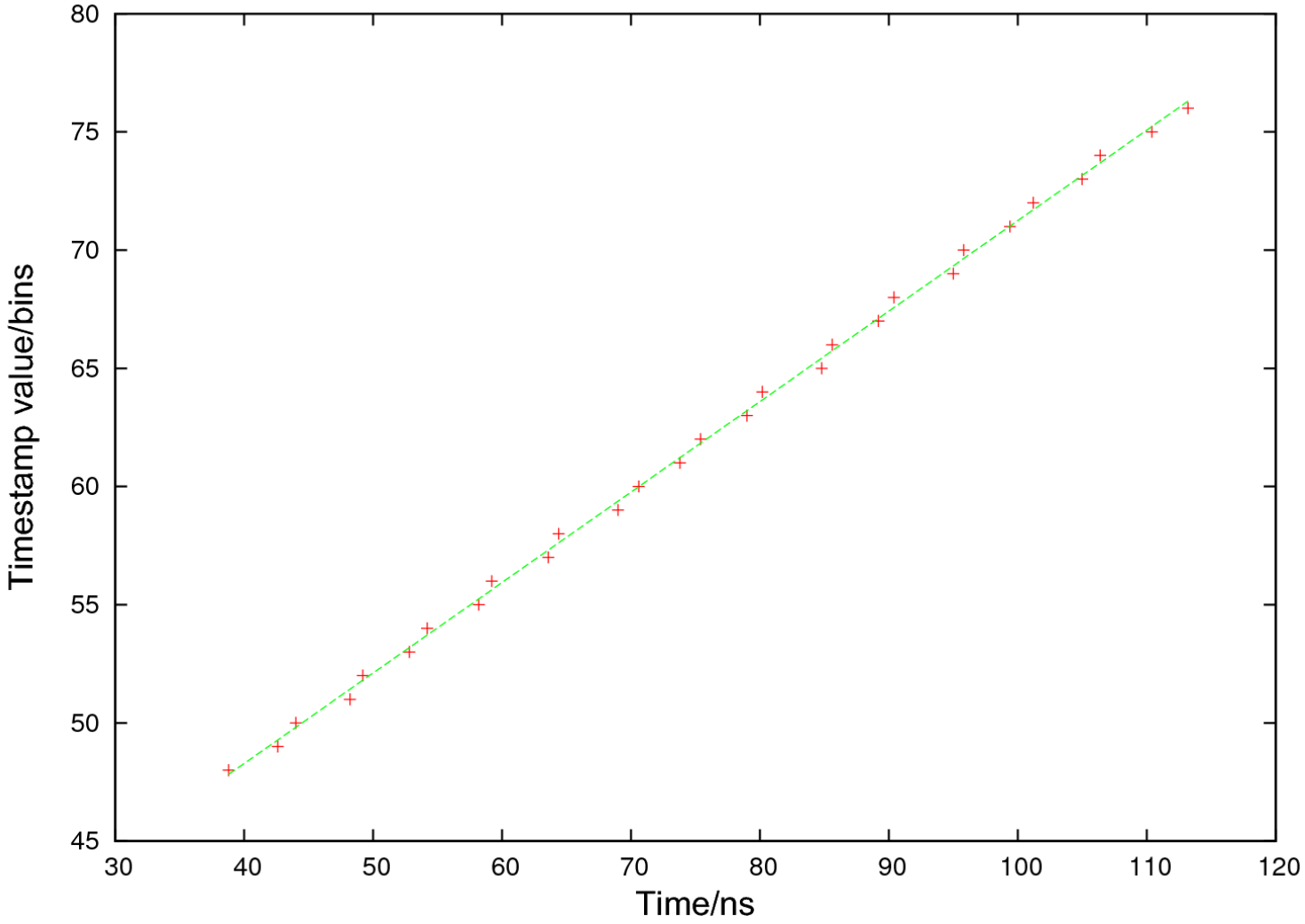
Remaining Issues

- Some features not fully implemented (or if implemented properly debugged).
  - Recording trigger information in timestamp.
  - Adjustment of PMT control voltage.
  - I2C control of clock.
    - Some units need jumpers changing on clock board.

Issues - Timestamps

- Optional “high resolution timestamp” mode in firmware (not compiled in by default). 2.6ns bins
  - With existing FPGA (Xilinx Spartan 3E) difficult to get accurate results
  - Use pulse generator with adjustable delay to measure timestamp vs. delay:

Timestamps vs. Delay



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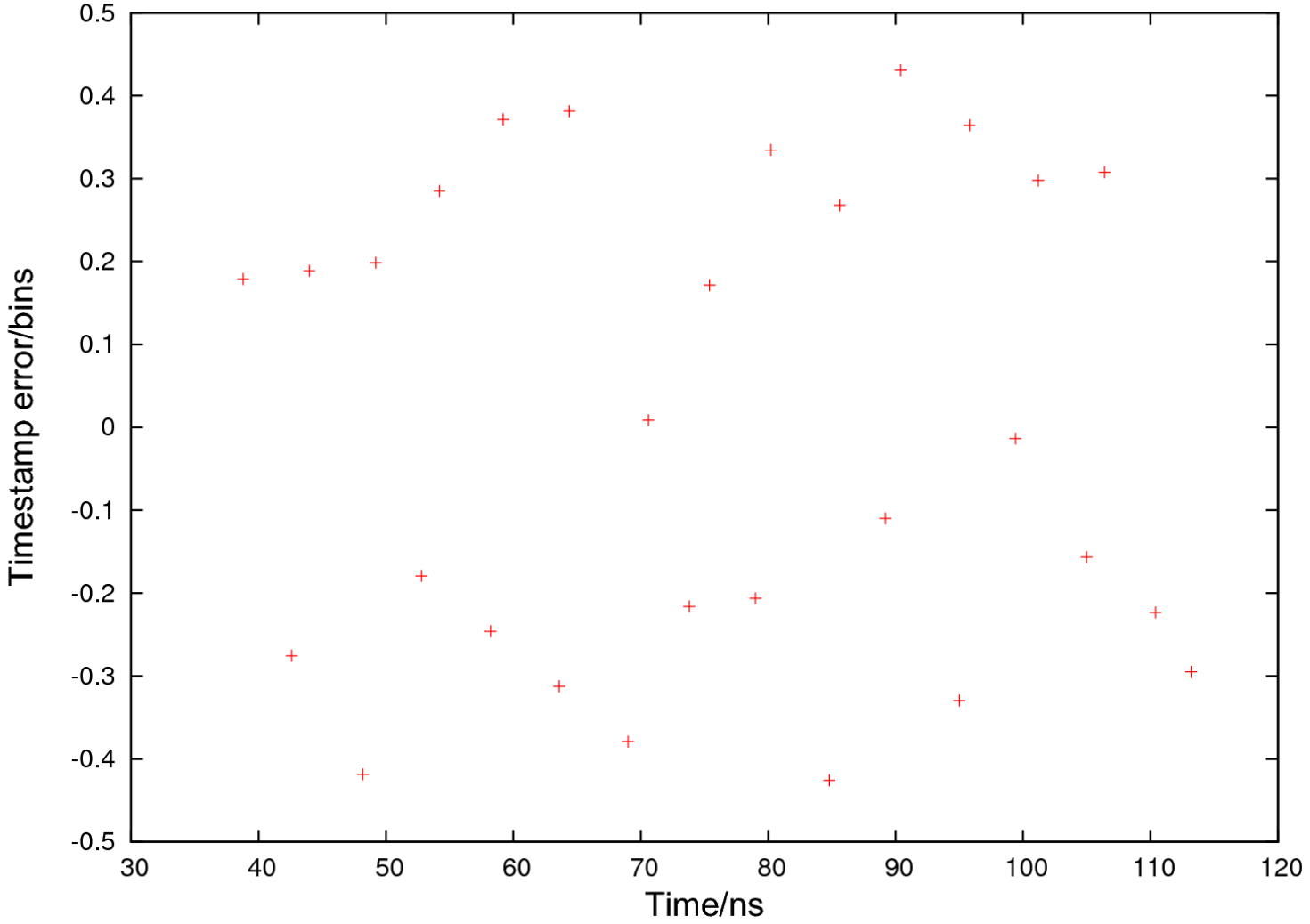
Timestamp Error vs. Delay



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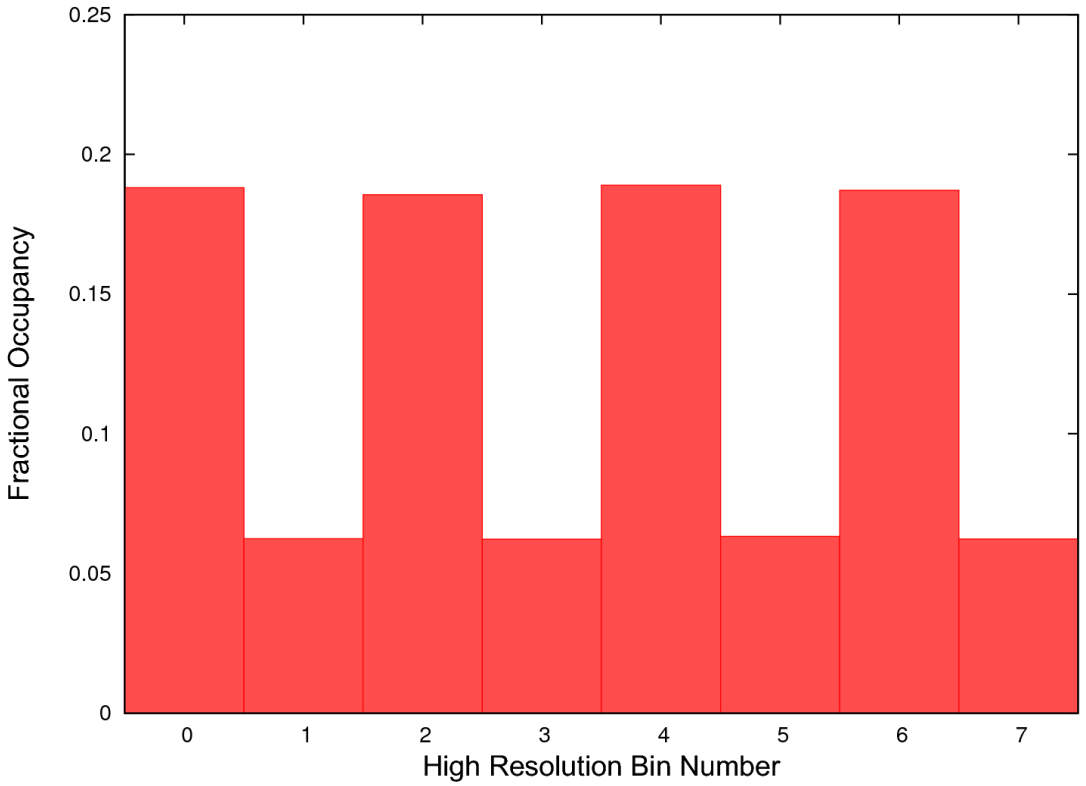
Timestamp – Bin Occupancy

- Random Triggers
- Look at bottom 3 bits.
- 200MHz clk M/Space ratio not 50%



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Pseudo Tagging Mode

- FORTIS DAQ continuously active.
  - DAQ reads out all data.
- FORTIS Readout f/ware modified to record every trigger that arrived.
  - Simple trigger/busy handshake used.

  (Trigger looped back to busy at FORTIS)

Pseudo Tagging Mode

- If data transfer to EUDAQ stalls, FORTIS DAQ buffers fill.
  - FORTIS firmware modified to raise "DUT_Clock" line when buffer about to fill
  - TLU firmware modified to veto triggers
    - selectable on DUT-by-DUT basis.
- Can be multiple triggers per frame.
- Could be applied to Mimosa readout.

Wish List

- Suggestions from users
  - Extra trigger inputs (J. Velthuis)
  - ~ Zero dead-time (P. Colas et. al.)
    - Could be done with existing h/ware & new f/ware
  - Timestamp every particle (M. Winter et. al.)
    - Could be done by firmware change on existing h/ware but would benefit from faster FPGA and link
  - More TLUs
    - Implies cheaper easier to assemble TLU

Plans

- Base AIDA TLU around a newer CoTS FPGA board.
  - Probably Xilinx SP605 (Spartan 6)
    - Trigger logic clock 200MHz (cf. 50Mhz). Higher trigger throughput.
    - Use hardware “deserializers” to improve TDC
  - Use Gbit/s Ethernet as link to host.
  - Soft-core processor.
- Use work being done for CMS upgrade.
  - e.g communication with host.

Plans

- "Full A-TLU" would look very similar to current model:
  - Six trigger inputs (cf. 4).
  - Fixed threshold discriminator with ADC to correct timing walk.
    - Lower latency (<10ns cf. ~ 25ns)
  - Keep RJ45 inputs (not an ideal connector, but keep compatibility with EUDET TLU)
  - Keep TTL, NIM I/O.
  - Front-end firmware very similar.

Plans

- "Mini TLU"
  - Use a prototype for new h/ware.
  - Use as lightweight TLU for users to integrate against.
  - Two trigger inputs.
  - Two RJ45 DUT I/O.
  - Single TTL DUT interface (Trigger,Busy,Clk)
  - Use new Xilinx sponsored "FMC" connector.
  - Interface identical to full TLU.

Conclusion

- EUDET TLU works.
  - Hardware seems to last if not abused (connectors are a weakness). One dead unit
- AIDA TLU - same DUT interface to as EUDET TLU.
  - Reduce firmware development time.
  - Reduce s/ware development time.
  - Users won't have to change anything to swap from EUDET to AIDA TLU