AIDA Meeting

Heidelberg

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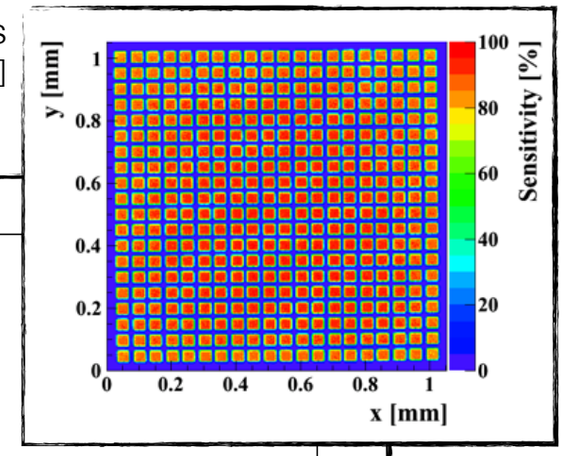
CALICE Work in HD

Test Beam and Data Analysis

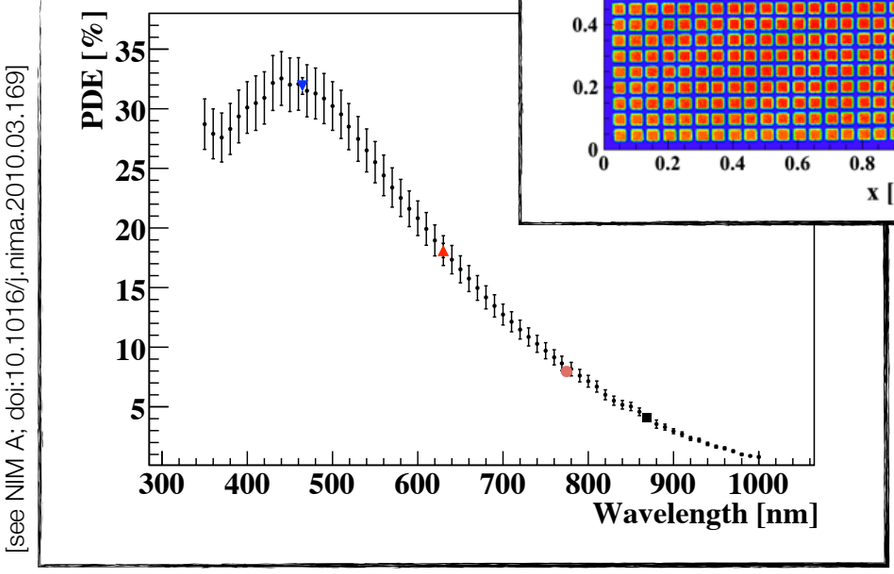
SiPM Characterization
SiPM Simulation
SiPM/Tile Quality Control System

SiPM Readout Electronics
[To be partially financed by AIDA]

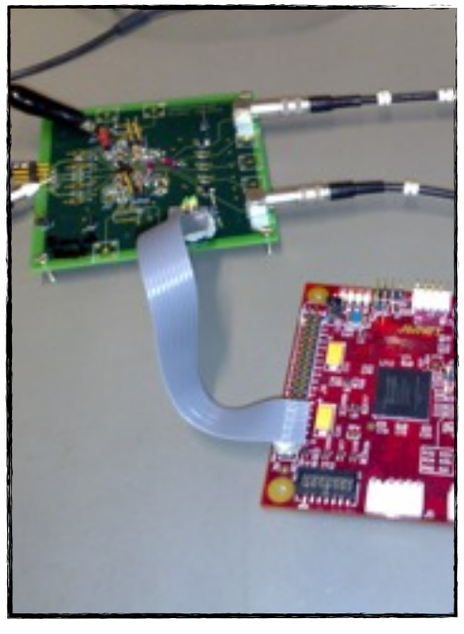
Uniformity Studies
[Sensitivity]



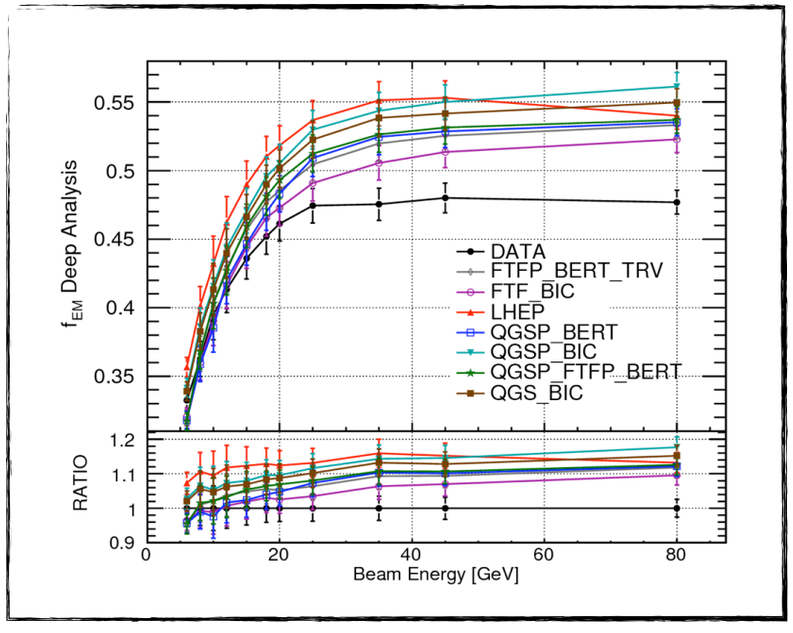
Absolute PDE

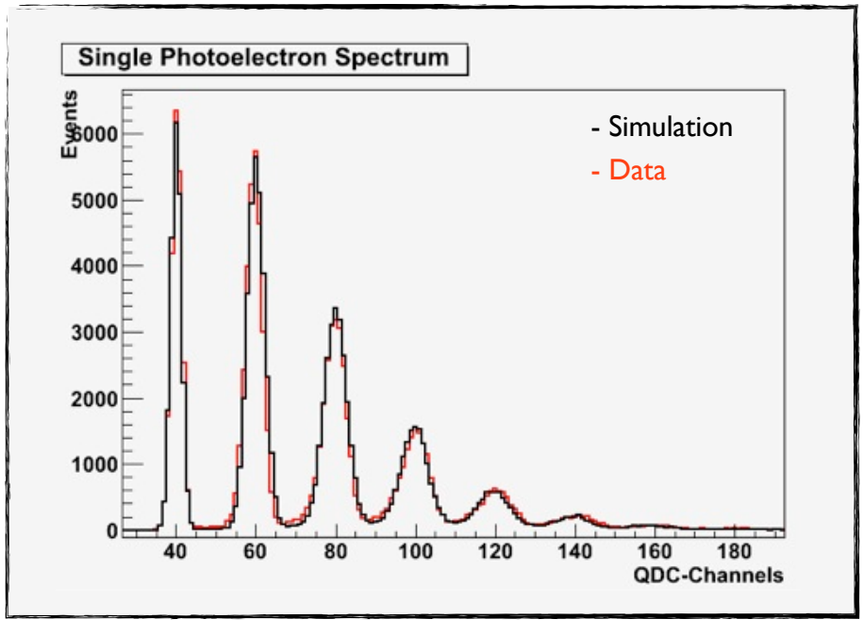


Chip Development



Hadronic Shower Analysis





SiPM Simulation

ASIC Development in HD

Heidelberg:

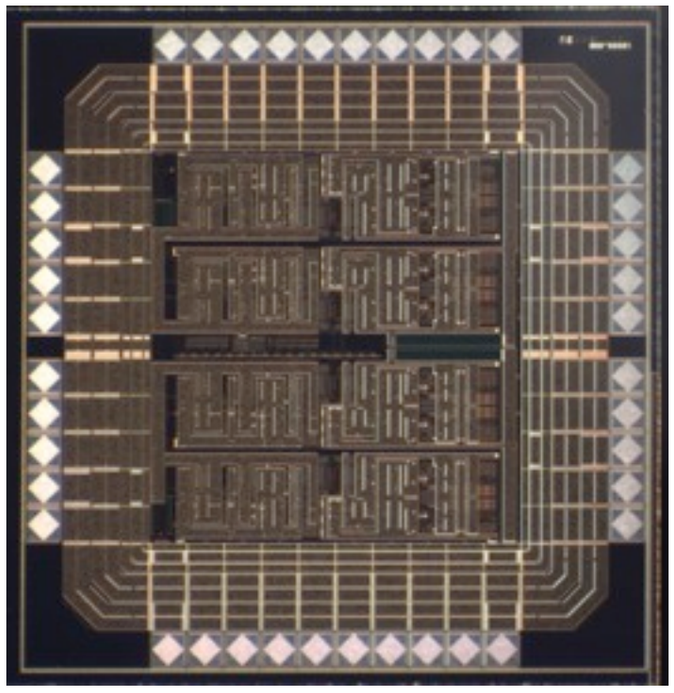
Two test chips produced ...
[financed by Helmholtz-Alliance]

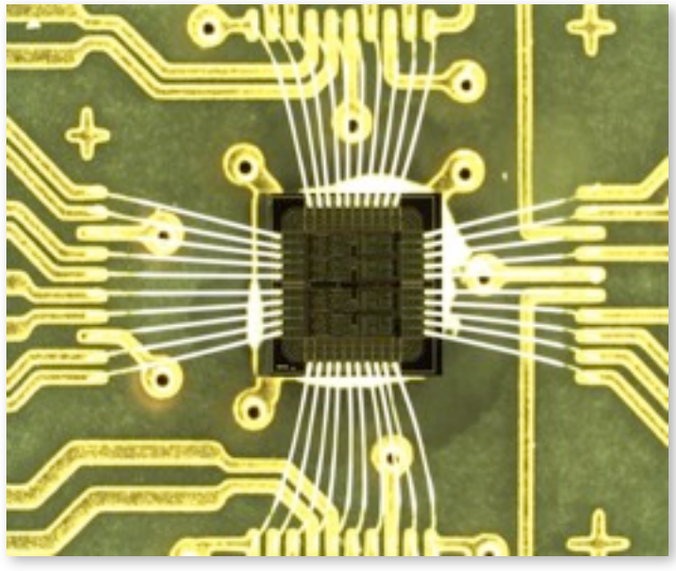
KLauS: Kanäle für Ladungsauslese von SiPMs
[Channels for Charge Readout of SiPMs]

AMS 350 nm CMOS technology; 4 channels;
SPI interface controlled by FPGA; Bias DAC tunable;
High signal/noise ratio [>10, 40 fC signal charge];
Fast trigger available [pixel signal jitter < 500 ps];
Large dynamic range up to 150pC

STiC: SiPM Timing Chip
[Fast Discrimination for ToF]

AMS 350 nm CMOS , 4 channels;
Leading edge & constant fraction trigger;
Bias DAC tunable ~ 1 V; power < 10 mW/channel
Pixel jitter ~300 ps, time of flight capability



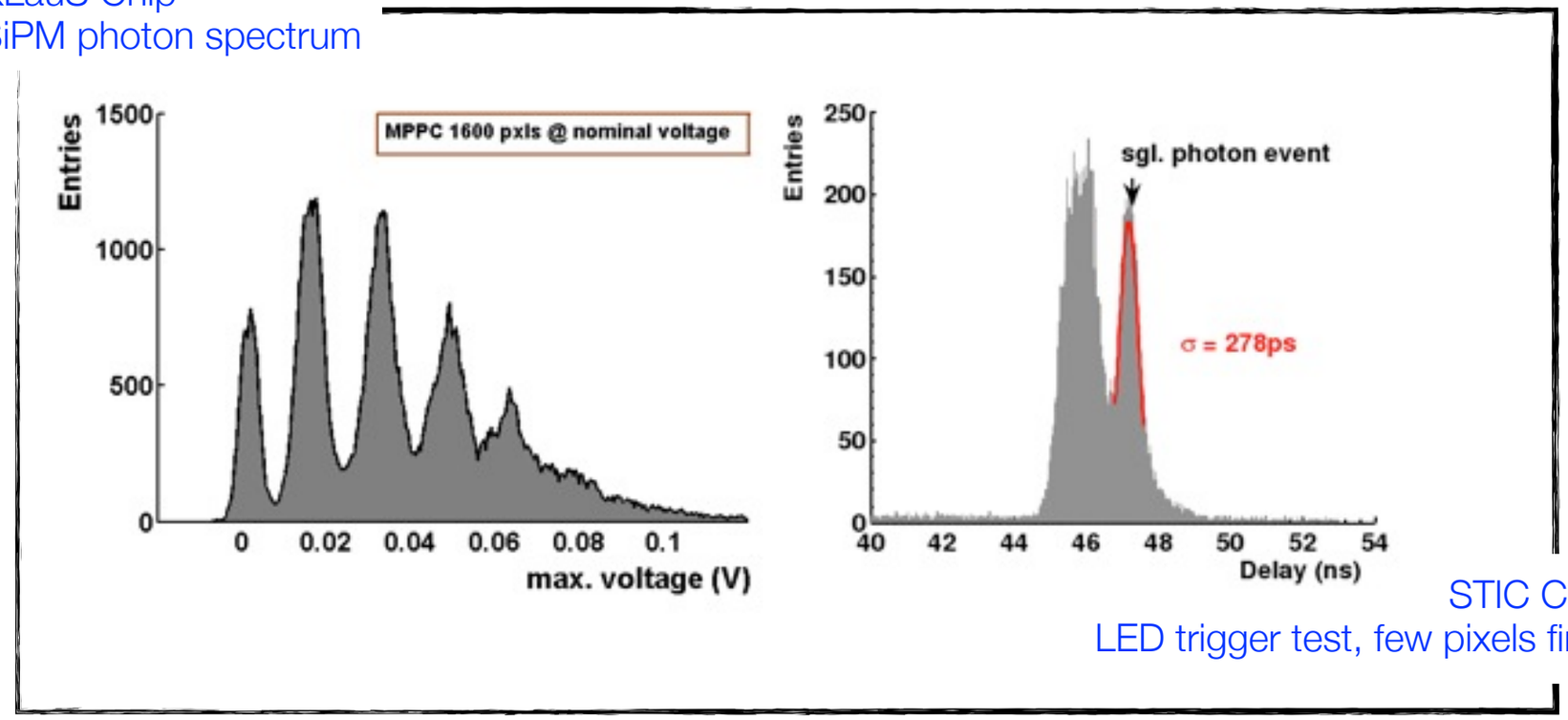


ASIC Development in HD

Performance measurements ...

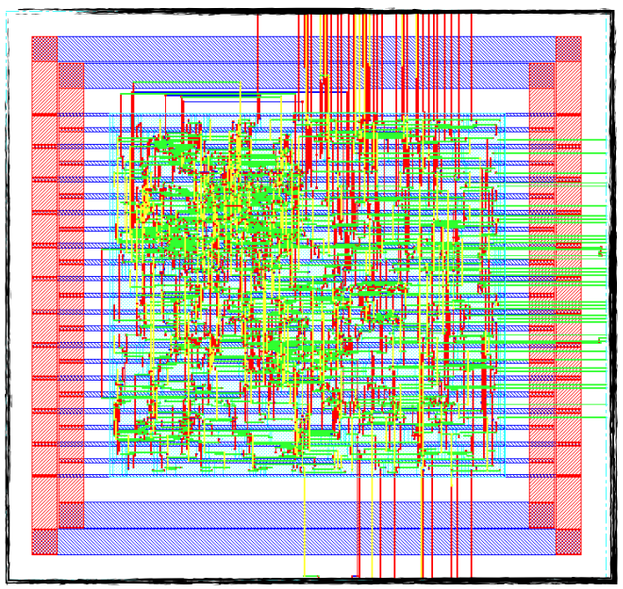
- Noise ...
- Timing ...
- Linearity ...
- Bias Tuning ...

KLauS Chip
SiPM photon spectrum



STIC Chip
LED trigger test, few pixels fired

I²C for KLauS 2.0



Further upgrade plans ...

STiC 2.0:

- Differential readout
- Tunable hysteresis
- ...

KLauS 2.0:

- Power reduction
- Power pulsing
- I²C Interface
- Integration with SPIROC
- ...