

# Omega

## FEV Boards status

N. Seguin-Moreau on behalf of  
Stéphane Callier, Dominique Cuisy, Julien  
Fleury

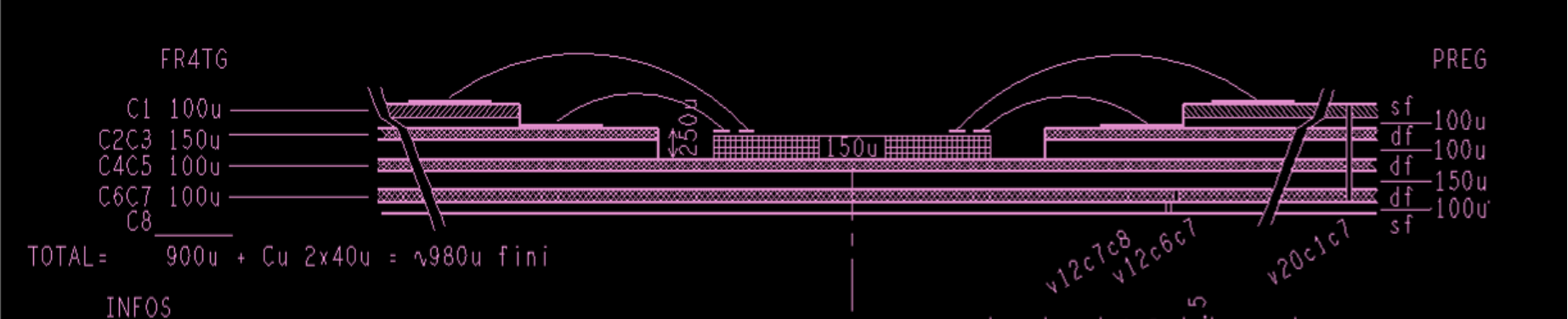
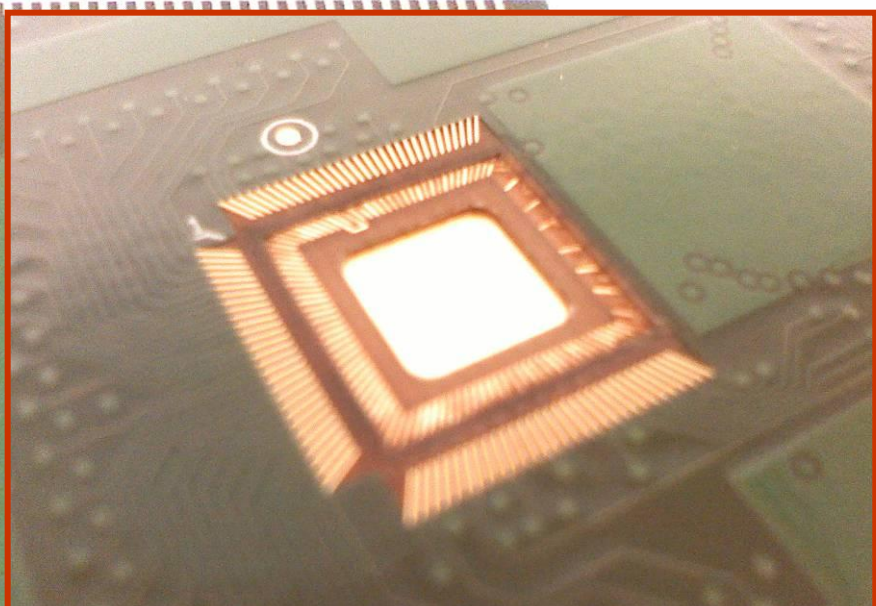
*Orsay MicroElectronics Group Associated*

# Reminder : FEV5 with HARDROC1

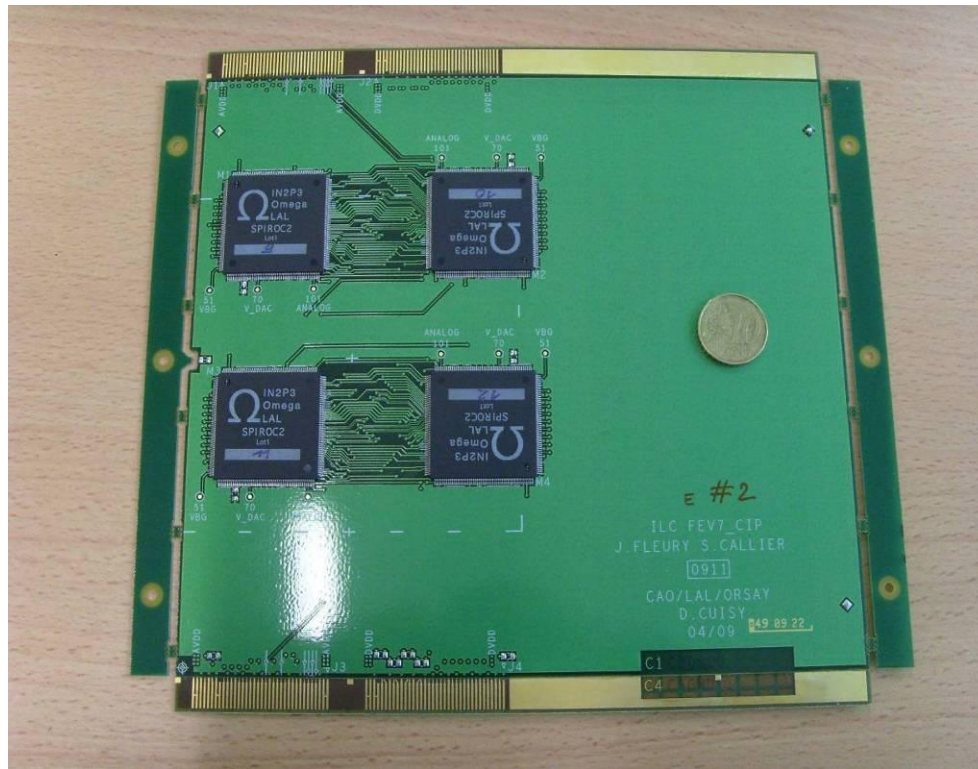


HARDROC1: 240 staggered pads

FEV5: too difficult to manufacture, bad quality of the bonding pads

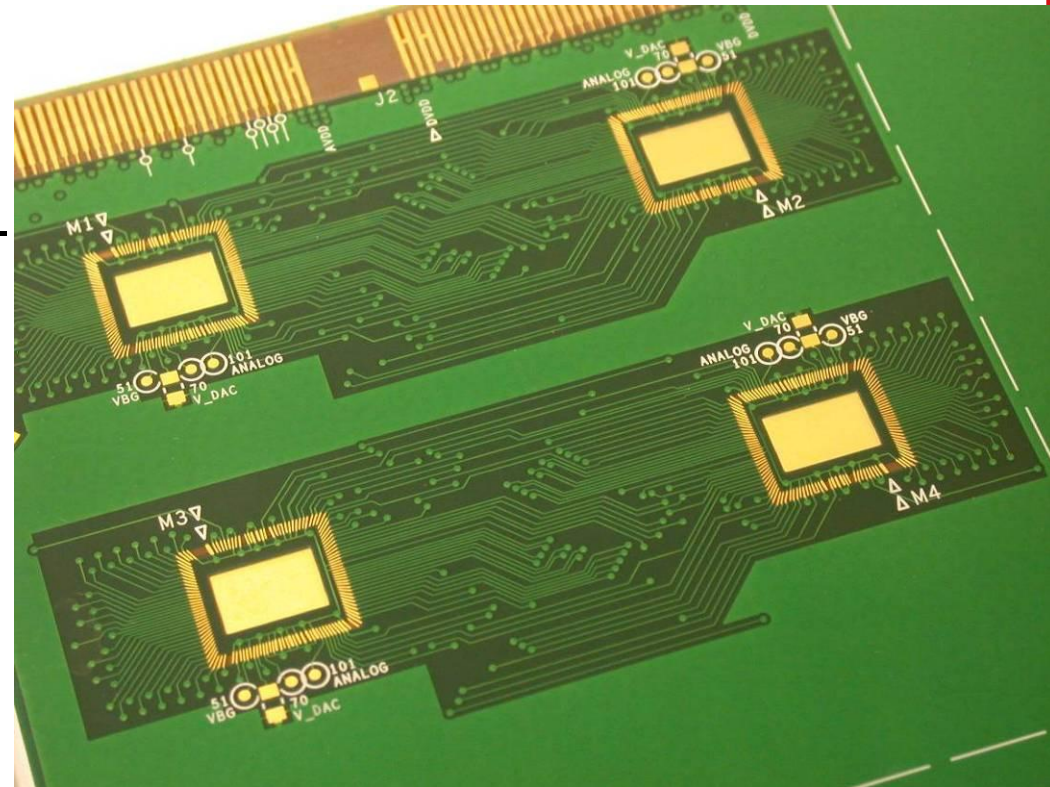


- Easy to manufacture
- Interconnexions tests: performed successfully (P. Cornebise)
- Perfect for DIF debug
- Fits the H structure



- 2 boards are equipped with 1 chip and 1 PCB equipped with 4 chips
- On the board access to :
  - Analogue Output
  - DAC and Bandgap Output
- On the connector, access to :
  - Every common digital line

- Front End Board using Chip-On-Board (spiroc2=208 pads)
- Nearly Identical to Chip-In-Package FEV7
  - Schematics identical
  - Same number of channels
  - Same pinout on Adapter Board/Slab Connector
- Except :
  - Pads connections to chip pins
  - Position of Wafer on the bottom side
  - Thickness: thinner to comply with H alveolar structure

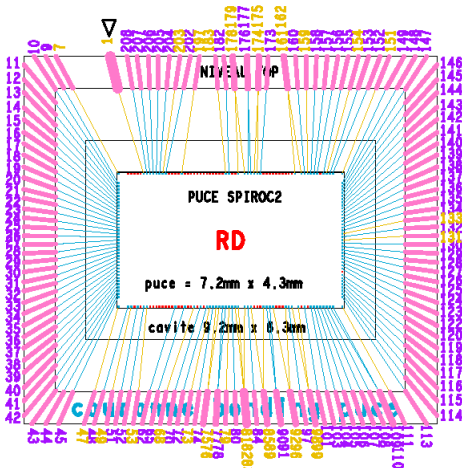


# FEV7 COB: Chip Embedding



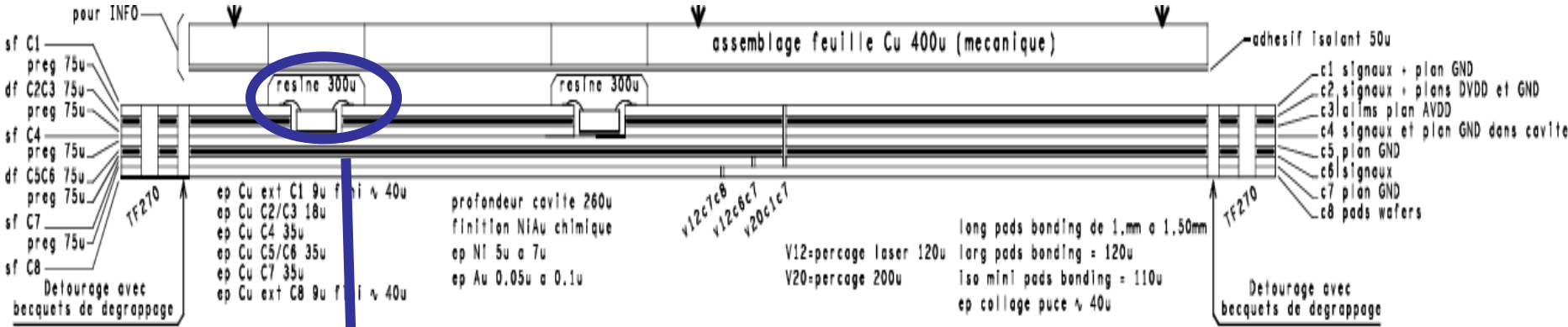
## Pile-up

TOP	GND + Input chip signal
C2	horizontal routing + DVDD + GND
C3	AVDD
C4	GND + vertical routing
C5	GND (pads signal shielding)
C6	pads routing
C7	GND (pads shielding)
BOT	PADS



## 4 drilling sequences :

- Laser C7-C8 120µ filled
- Laser C6-C7 120µ
- Mechanical C1-C7 200µ
- Mechanical C1-C8 (for PCB fastening)



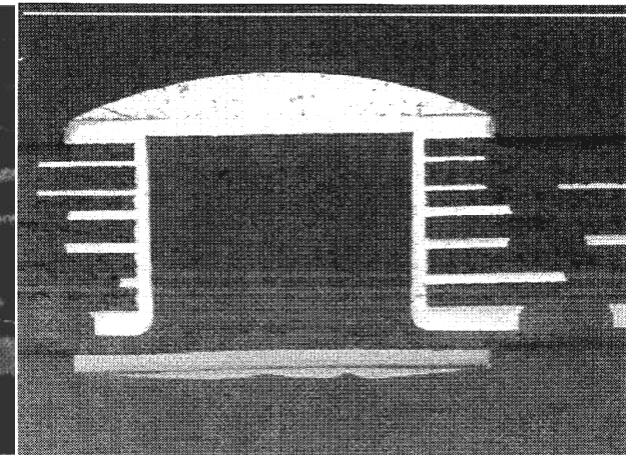
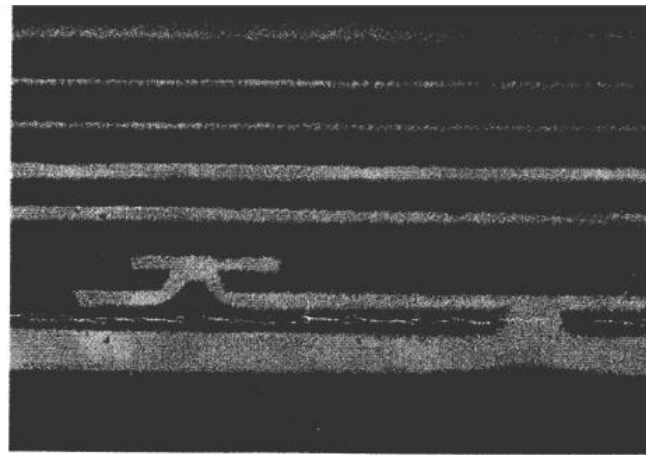
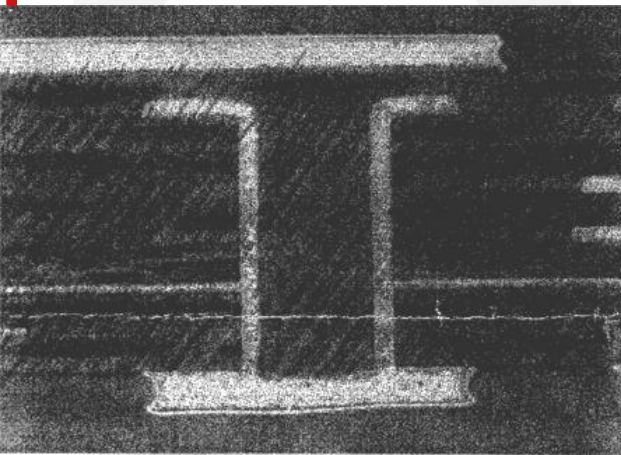
NB: En respectant toutes les epaisseurs (preg et Cu) l'empilage peut etre compose de 3 doubles face C2-C3, C4-C5, C6-C7.

**Resin (300µm)  
for chip protection**

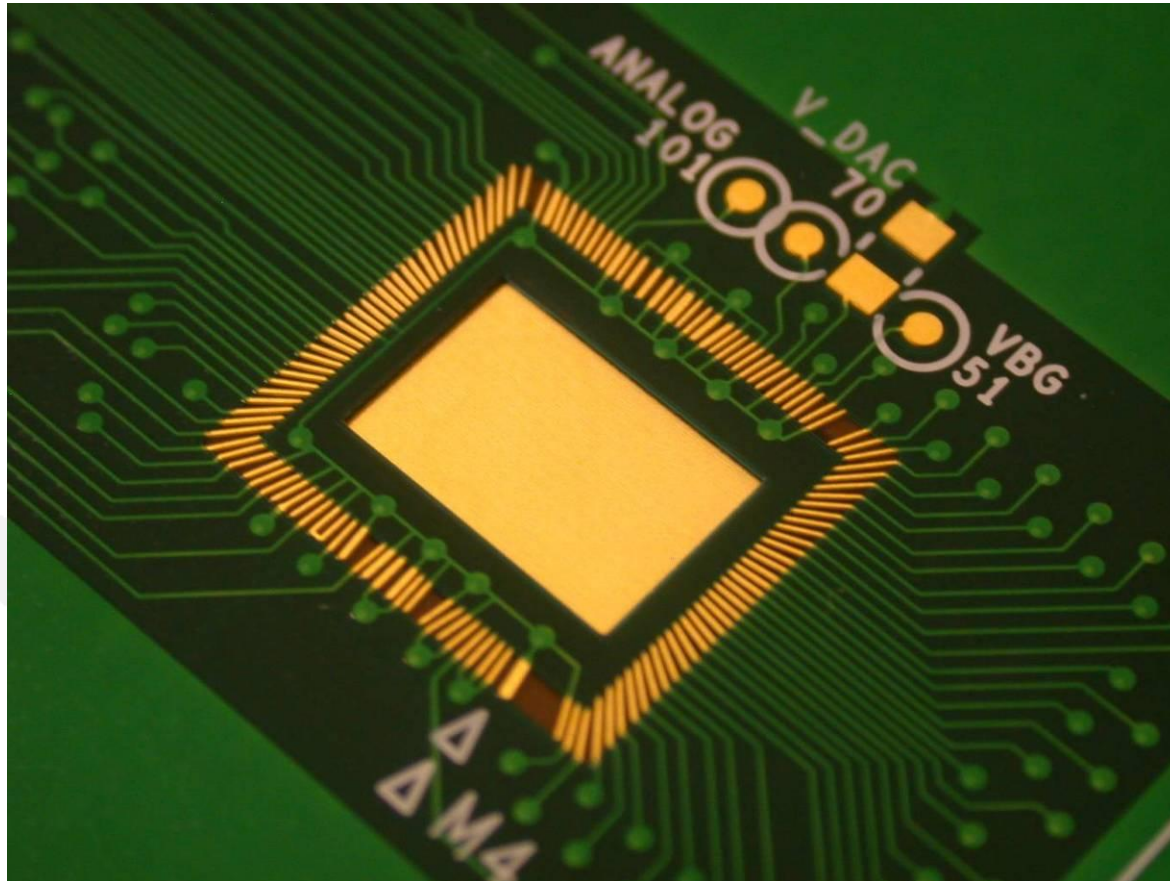
epaisseur totale  $(7 \times 75u) + (2 \times 18u) + (4 \times 35u) + (2 \times 40u) = 781u$

**PCB Thickness  
~781µm**

- 2 Manufacturers :
  - Elvia : 6 PCB received (2 batches)
  - Protechno : 6 PCB received (2 batches)
- Mechanical report :
  - Manufacturers Measurements :
    - 0.83mm Elvia, 0.93 Protechno
  - LLR Measurements :
    - between 0.83 & 0.94 for **both** boards
- Plated Through Hole Cross Section :



- 2 PCB FEV7-COB fully bonded



- We have an official agreement with CERN for free bonding
  - **Reminder : 1830 € for 2 boards (8 chips -> ~800 wires to bound)**
- Still resin pb for chip protection: to be solved
  - We have to keep a low thickness of the cabled PCBs

# FEV7- COB2:

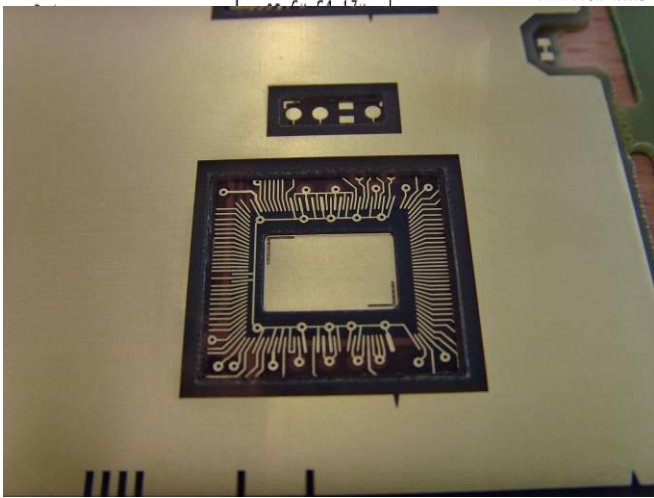
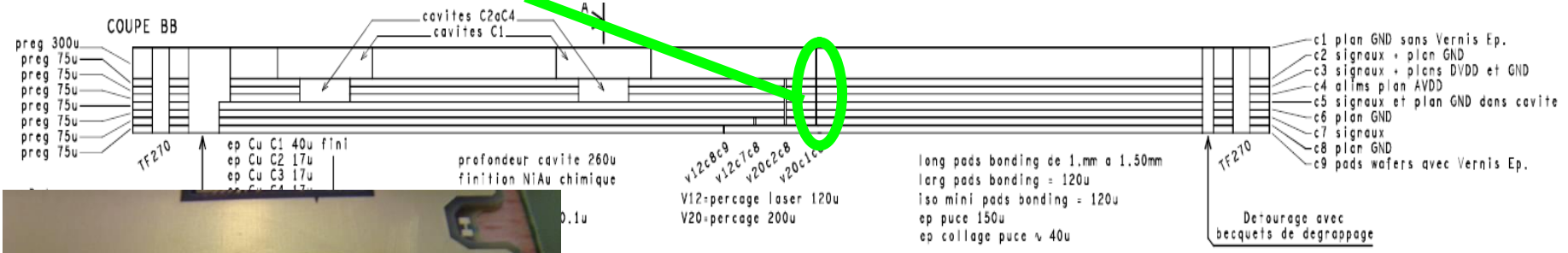


Pile-up: 10 layers

Top	cover layer connected to GND
C2	GND + Input chip signal
C3	horizontal routing + DVDD + GND
C4	AVDD
C5	GND + vertical routing
C6	GND (pads signal shielding)
C7	pads routing
C8	GND (pads shielding)
BOT	PADS

- 4 drilling sequences :**
- Laser C8-C9 120µ filled
  - Laser C7-C8 120µ
  - Mechanical C2-C8 200µ
  - Mechanical C1-C9 (for PCB fastening)

**Drilling sequence**



seur totale max **1100u**

**PCB Thickness 1100 µm**

- No solder mask on TOP layer
  - Fit the H structure, access to the analog signals
  - TOP electrically linked to GND
- => **too difficult to manufacture (same pbs as for FEV5) => FEV8**



# FEV8: Chip Embedding

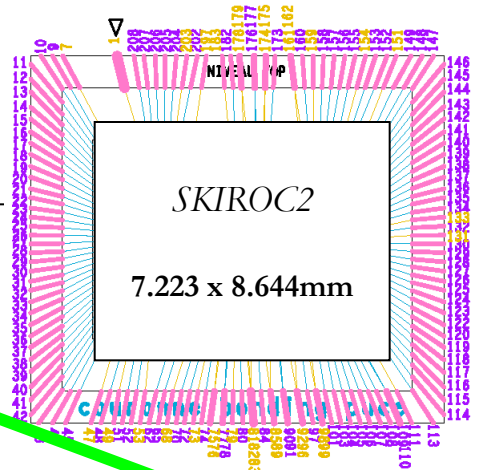


**Pile-up:**

8 layers + **FLOATING** Mechanical interposer on the TOP

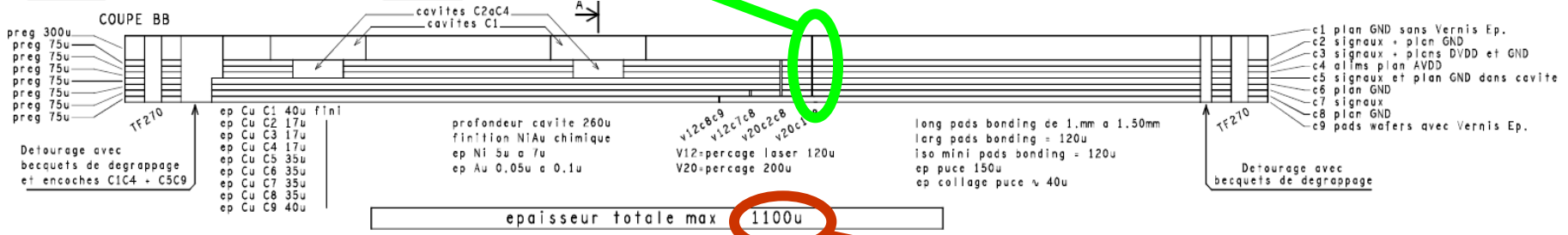
- C1 GND + Input chip signal
- C2 horizontal routing + DVDD + GND
- C3 AVDD
- C4 GND + vertical routing
- C5 GND (pads signal shielding)
- C6 pads routing
- C7 GND (pads shielding)
- C8 PADS

**FEV 8**



- 4 drilling sequences :
- Laser C8-C9 120μ filled
  - Laser C7-C8 120μ
  - Mechanical C2-C8 200μ
  - Mechanical C1-C9 (for PCB fastening)

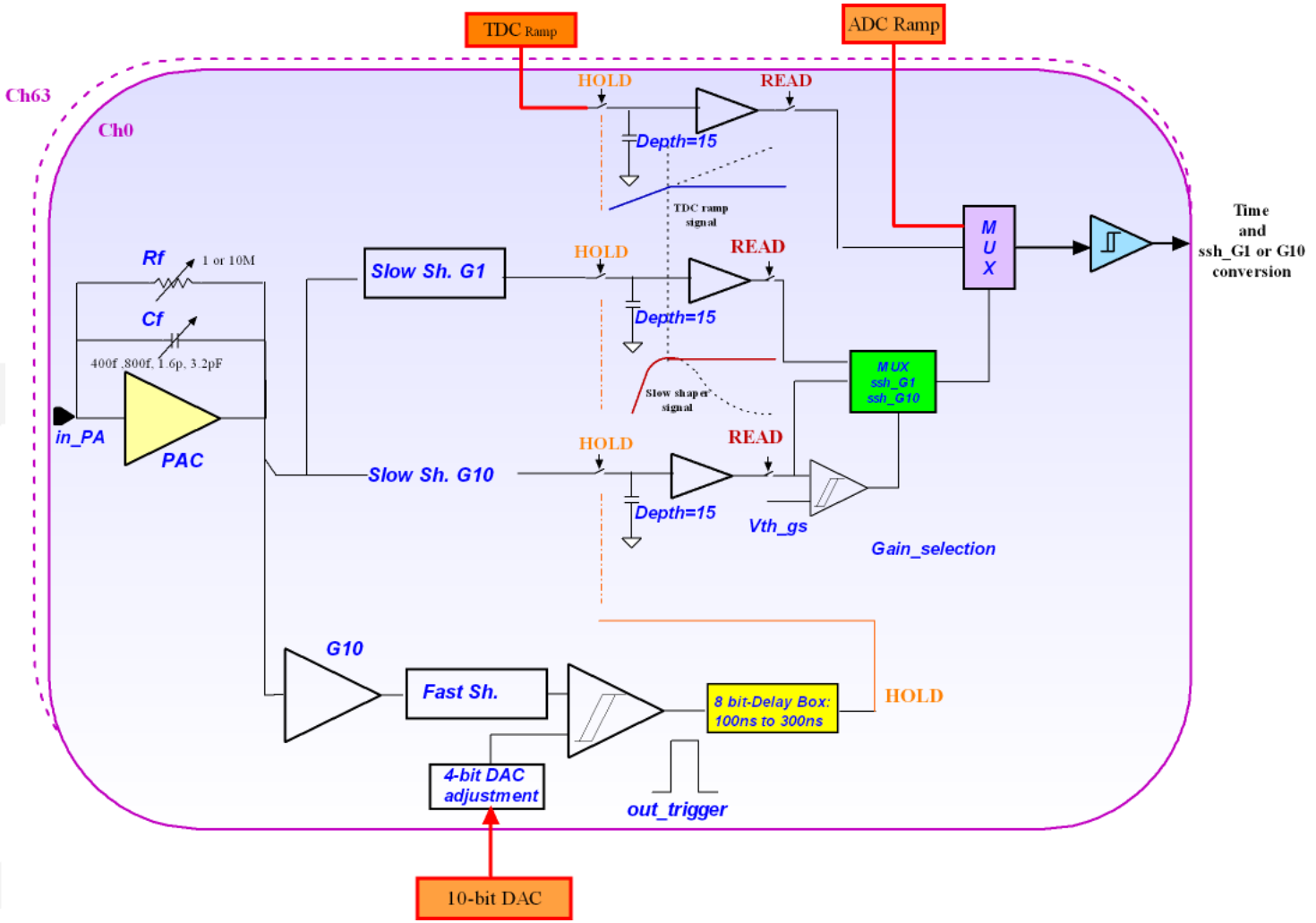
Drilling sequence removed



- PCB currently under design
- Fits the H structure, access to the analog signals
- Currently under design in collaboration with our Korean colleagues
- Will be equipped with SKIROC2 chips

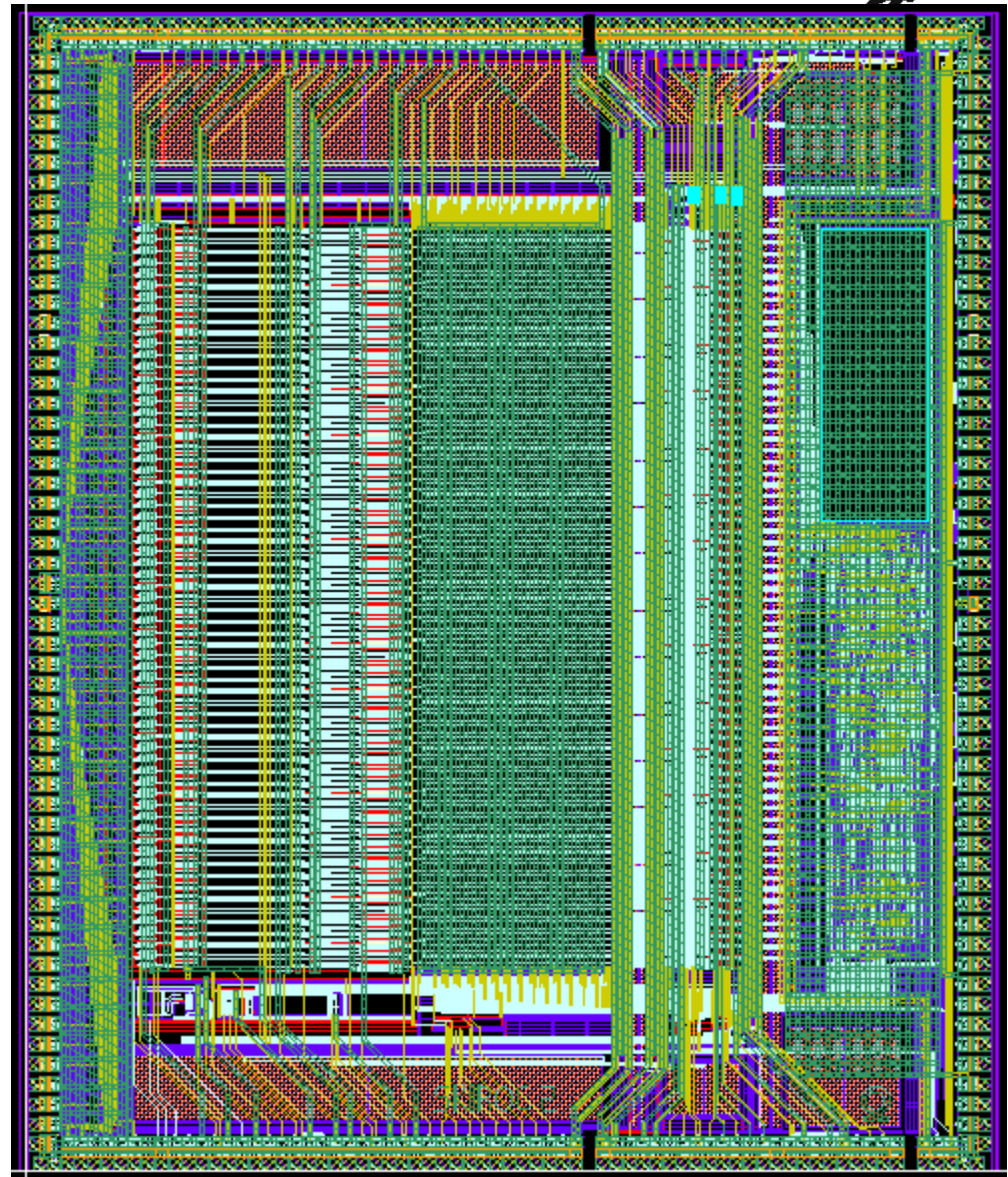
**PCB Thickness 1100 μm**

- 64 inputs, 1/2 Mip to 2500 Mip (keeping the same gain)
- Analogue signal-to-noise ratio : 17 (1500 e<sup>-</sup> noise for 1 MIP)



# SKIROC2 (2)

- Submitted in the prod run (March 2010):
  - 1200 SKIROC2
  - Wafers sent this week to I2A technology (Fremont-USA) for thinning, dicing and packaging)
- 250 pads
  - 3 NC
  - 17 for test purpose only
- A few samples will be packaged in a ceramic 240 pins package to be tested easily on a testboard
- First tests foreseen next October



- No manufacturing critical issue with
  - FEV7-CIP
  - FEV7-COB
- No bonding issue with FEV7-COB for both manufacturers
- Next FEV8 will have 16 Skiroc2 chips
  - 1024 channels on 180 mm x 180 mm board
  - Our Korean colleagues (Sung Kyun Kwan University) should take in charge half of the next FEV8 production
- First tests of packaged SKIROC2 expected in October

# Omega



**BACKUP SLIDES**

*Orsay MicroElectronics Group Associated*

# FEV7 Board(s)

5 mm x 5 mm pads size  
 180 mm x 180 mm wafer size  
 -> 324 pads on a 1/4 board

**36 channel areas**

use of SKIROC2 (36 ch)  
 in SKIROC mode

-> 144 Channels (4 x 36)  
 will be used for Wafer

Characterization

**Chip on Board**

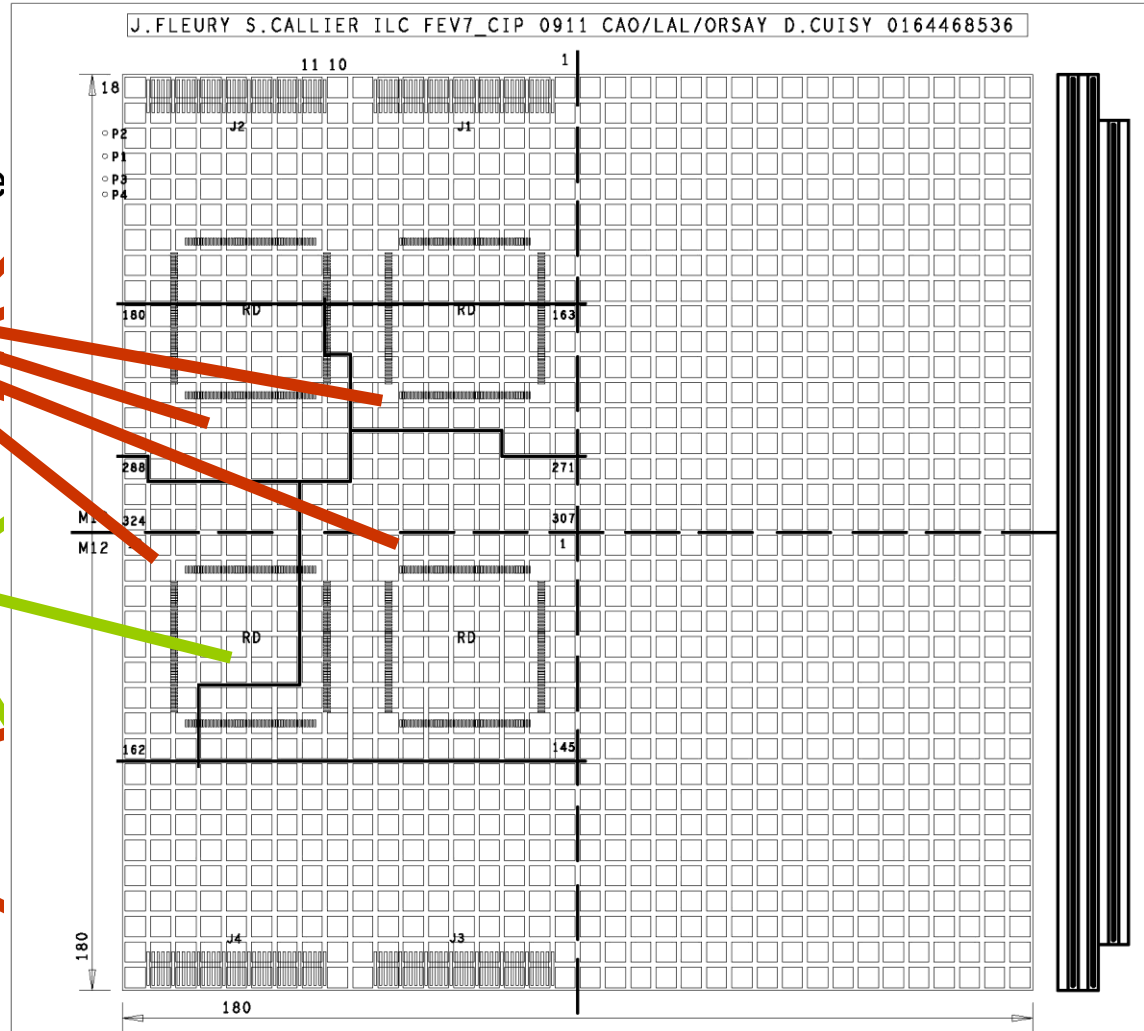
**version**

Why such a board?  
 - Due to the troubles with  
 FEV5 manufacturing

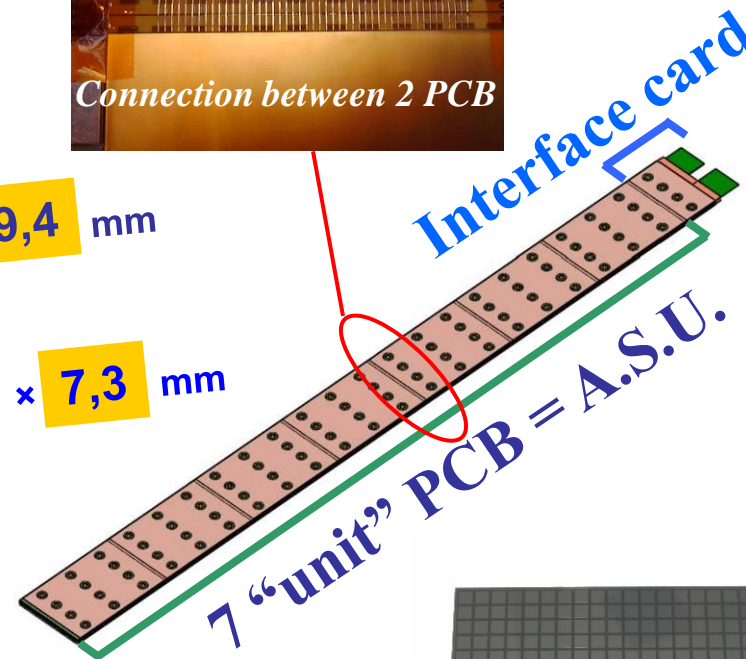
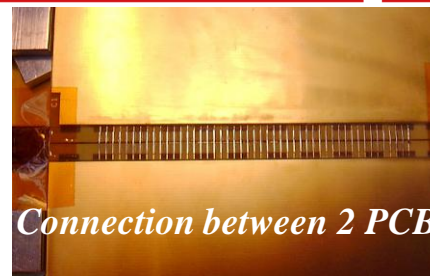
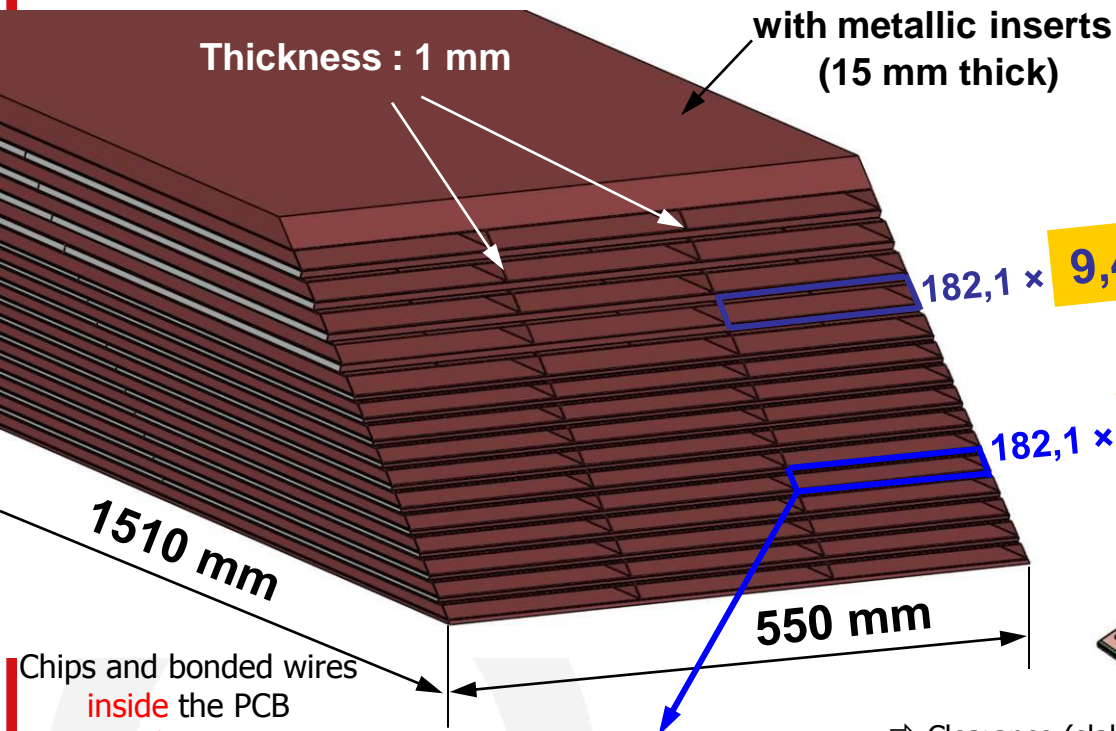
**9 PADS merged**

Purpose :

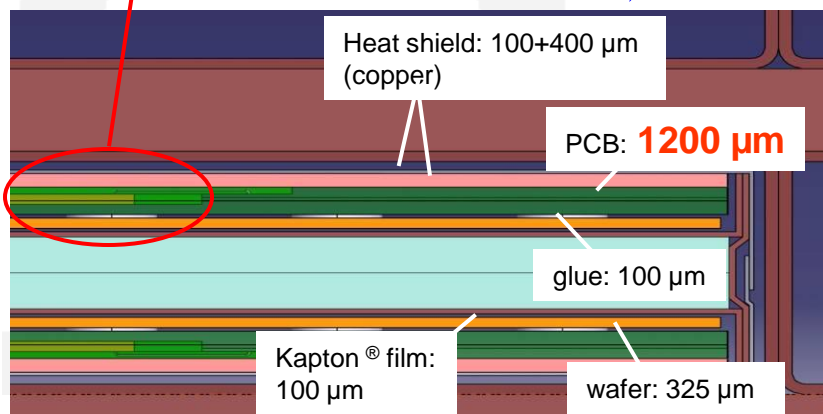
- Interconnexion tests
- Allow SLAB + DIF debug
- Allow mechanical integration



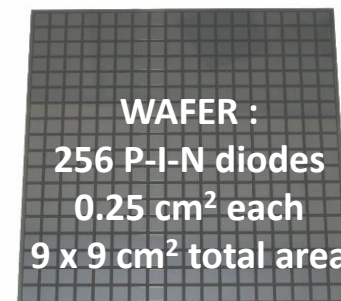
Epaisseur max CI 12/10 CI 8 couches



Chips and bonded wires inside the PCB



- ⇒ Clearance (slab integration) : 500  $\mu\text{m}$
- ⇒ Heat shield : 400  $\mu\text{m}$  ? →
- ⇒ PCB : 1200  $\mu\text{m}$  ? → design possibilities
- ⇒ Thickness of glue : 100  $\mu\text{m}$
- ⇒ Thickness of wafer : 325  $\mu\text{m}$
- ⇒ Kapton<sup>®</sup> film HV : 100  $\mu\text{m}$  ? → tests
- ⇒ Thickness of W : 2100/4200  $\mu\text{m}$  ( 80  $\mu\text{m}$ )



See talk by Remi Cornat

Courtesy :  
Marc Anduze - LLR

- First Step : Electrical tests (continuity / shorts)
- Second Step : Slow Control Loading
- If OK, we can start real tests ! 😊
  - Check all Analogue Channel Outputs
  - Ensure Discriminators, Masks, Calibration Tests Input work accurately
  - ADC Tests
  - Analogue and Digital Measurements
- Then, tests with 2 PCBs  
(-> need interconnection techniques)
- Finally, tests with Wafers  
(-> need of wafer/pcb assembly)

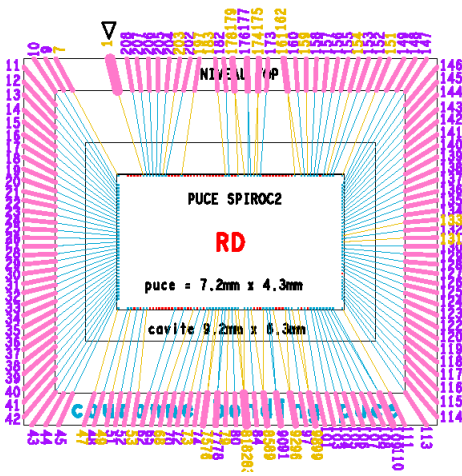


# FEV7 COB2: Chip Embedding



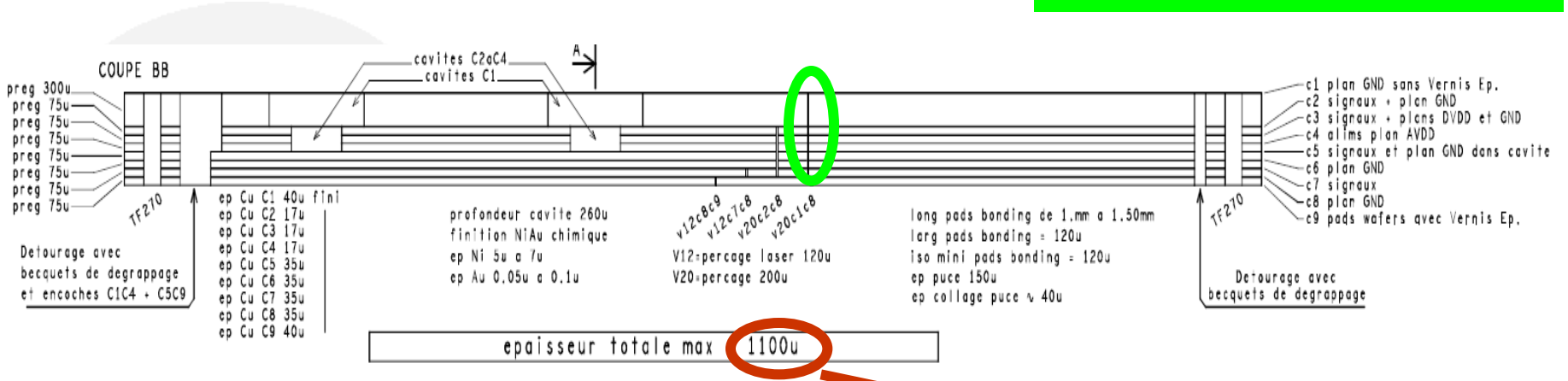
## Pile-up

Top	GND cover layer
C2	GND + Input chip signal
C3	horizontal routing + DVDD + GND
C4	AVDD
C5	GND + vertical routing
C6	GND (pads signal shielding)
C7	pads routing
C8	GND (pads shielding)
BOT	PADS



## 5 drilling sequences :

- Laser C8-C9 120μ filled
- Laser C7-C8 120μ
- Mechanical C2-C8 200μ
- Mechanical C1-C8 200μ
- Mechanical C1-C9 (for PCB fastening)



**PCB Thickness 1100 μm**

# FEV7\_COB Prices



FEV7_COB 0901	XXXXXX	QTE 10	QTE 50	QTE 100	OUTILLAGE	QTE 10 TOTAL HT
APPARATUS						
ELVIA	03--06	2774	10140	19890	850	3621
PROTECNO	27--05	4400	13400	25100	521	4921
ELCO	19--05	5230	15050	21800	1130	6360
PHOTOCHEMIE	02--06	10290	30800	61600	614	10904
EXCEPTION	X	X	X	X	X	X
ATLANTEC	X	X	X	X	X	X
CERN	22--04	4700	X	X	660	5370
le 03/06/09 D.CUISY CAO/LAL/ORSAY						

- FEV7-CIP & FEV7-COB board manufactured by 2 companies to ensure successful result
- FEV7-COB2 prices

FEV7_COB2 09xx	XXXXXX	QTE 10	QTE 50	QTE 100	OUTILLAGE	QTE 10 TOTAL HT
ELVIA	29--10	3325	12980	26240	900	4225
PROTECNO	23--10	13000			600	13600
le 30/10/09 D.CUISY CAO/LAL/ORSAY						

- We have lost 1 manufacturer !!

# Engineering run

- **Reticle size : 18x25 mm<sup>2</sup>**

- 50-55 reticles/Wafer
- 25 wafers needed

- **Final arrangement:**

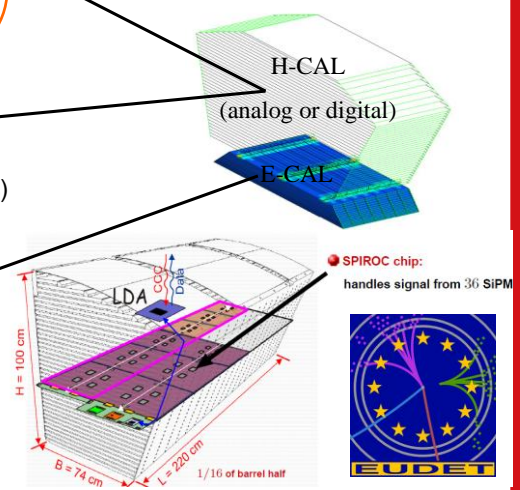
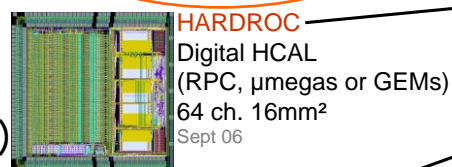
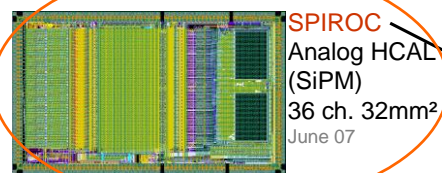
- **« Calice » chips produced:**

- **7 Hardroc 2b** => ~9000 chips
- **1 Spiroc 2a** => ~1200 chips
- **1 Spiroc 2b** => ~1200 chips
- **1 Skiroc 2** => ~1200 chips

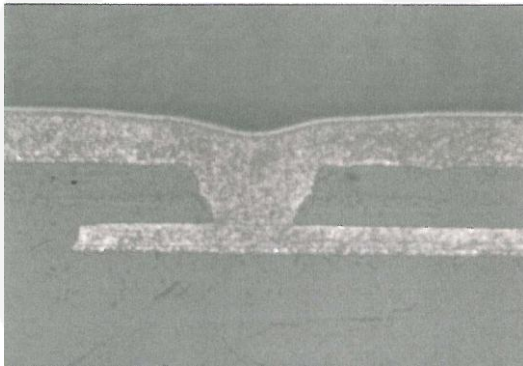
- **Additional chips produced:**

- 1 Spaciroc : JEM EUSO experieiment
- 1 Maroc 3 : for PMT readout
- 3 Spiroc 0 (SPIROC « light » version)
- => **cost reduction** for CALICE

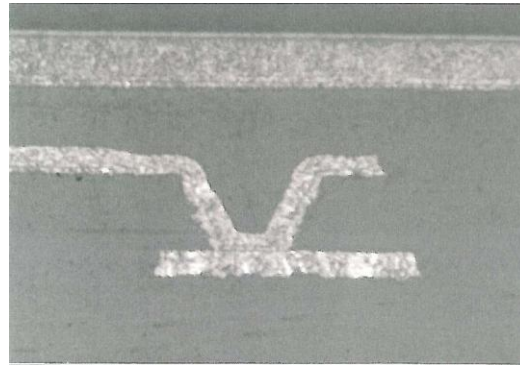
- **Production run launched last week**



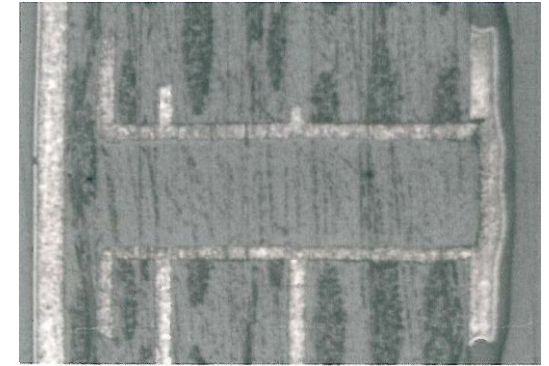
- 2 Manufacturers :
  - Elvia : 10 PCB received
  - Protechno : 10 PCB received
- Manufacturers report :
  - Thickness Measured : 0.90mm to 1.00mm (0.96 desired)
  - Metal minimum thickness on vias : 25 $\mu$ m
- Plated Through Hole Cross Section :



Blind via (C7-C8)



Buried via (C6-C7)



Mechanical (C1-C7)