# AHCAL Electronics.

## status and open issues

Mathias Reinecke

CALICE ECAL/AHCAL - EUDET electronics and DAQ - AIDA

DESY, July 5th to 6th, 2010

HELMHOLTZ GEMEINSCHAFT

CALICE Calorimeter for ILC

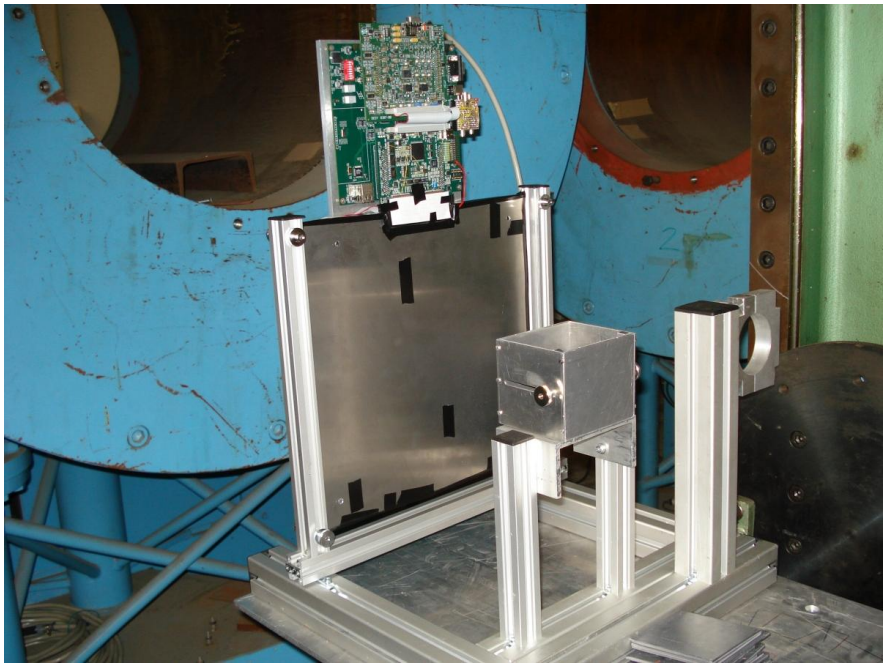
EUDET

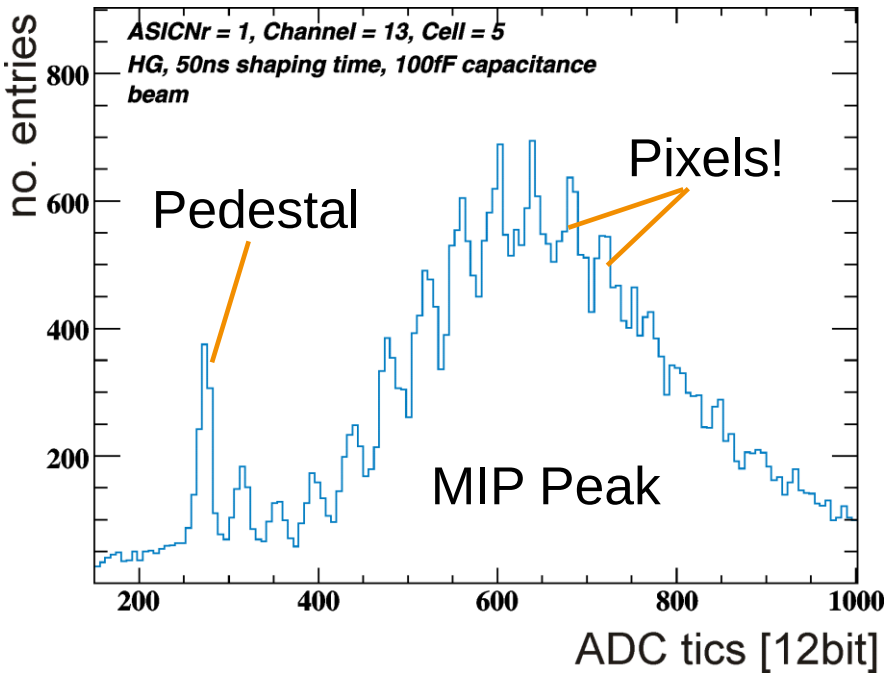
DESY

# Outline

- Status Electronics / Hamburg Activities
  - Testbeam Setup (HBU_II)
  - Laboratory Setup (HBU_I)
- Next Generation (Full Layer EUDET Module)
  - Status Redesigns Boards (DESY)
  - LED Systems for Calibration
  - Tiles
- Status DAQ / Discussion about CALICE DAQ
- Conclusion

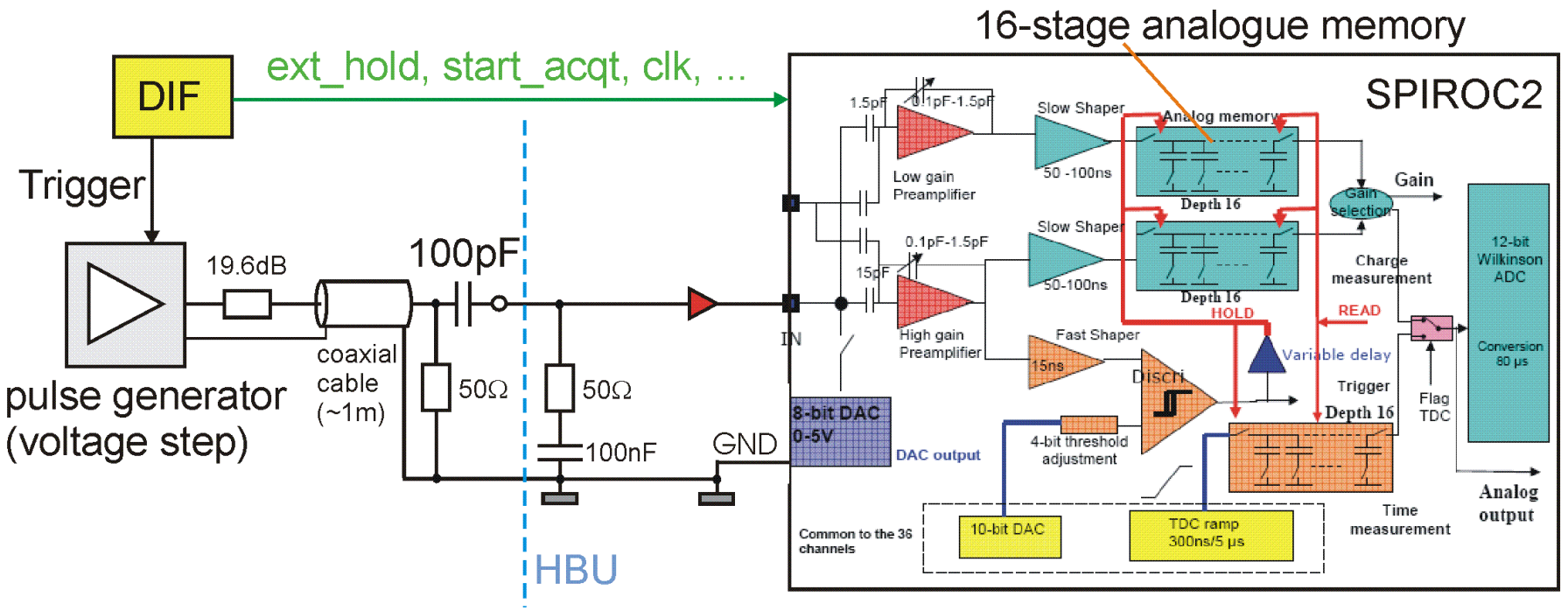
# DESY Testbeam Setup – HBU_II





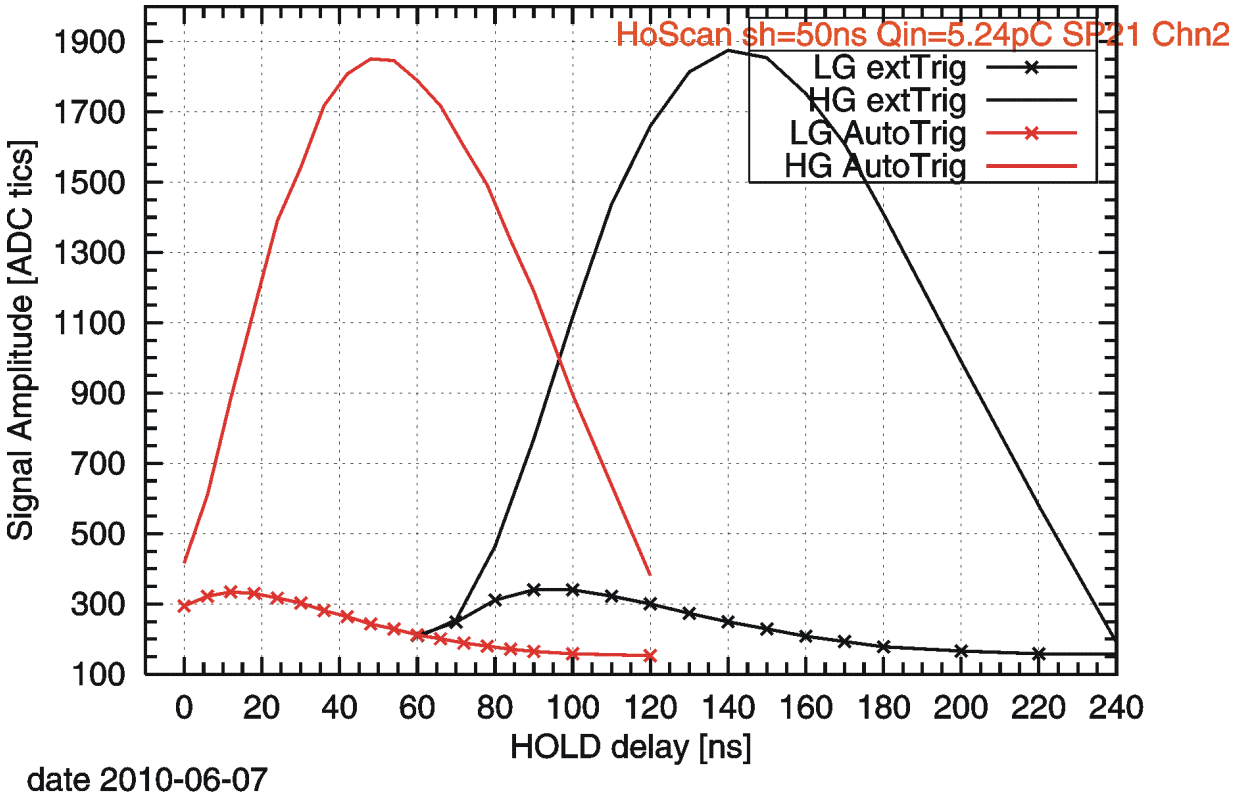

- DESY 6GeV electron Testbeam operation: Setup optimization, Channel-wise calibration with MIPs: **Mark Terwort**
- Integrated LED System, uniformity studies / optimiz.: **Julian Sauer**
- For detailed results on both: **See Julian's talk**

# Charge Injection Setup – HBU_I in laboratory



# SPIROC2 HOLD Scans – Internal Trigger (Autotrigger)

‘Autotrigger’: Most important operation mode for SPIROC2 => ‘ILC mode’

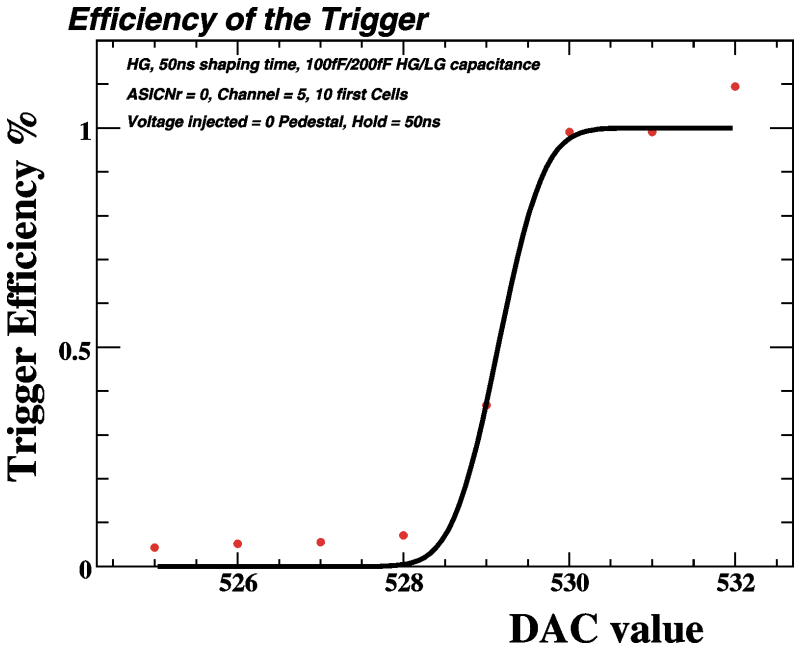


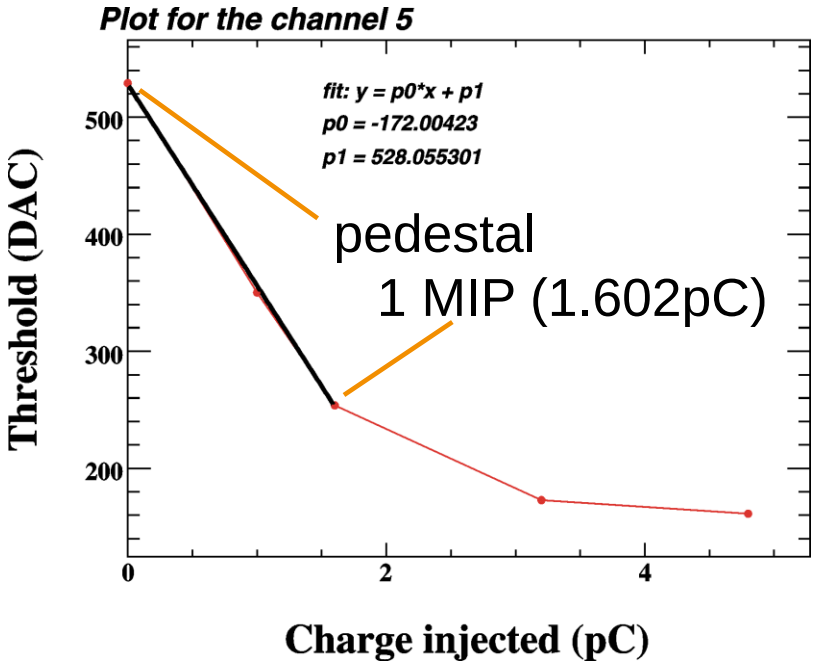

Autotrigger hold delay: 2ns per 6-bit-tic in slow control data.

Results for Autotrigger agree with the external trigger results.

# Autotrigger Threshold Adjustment

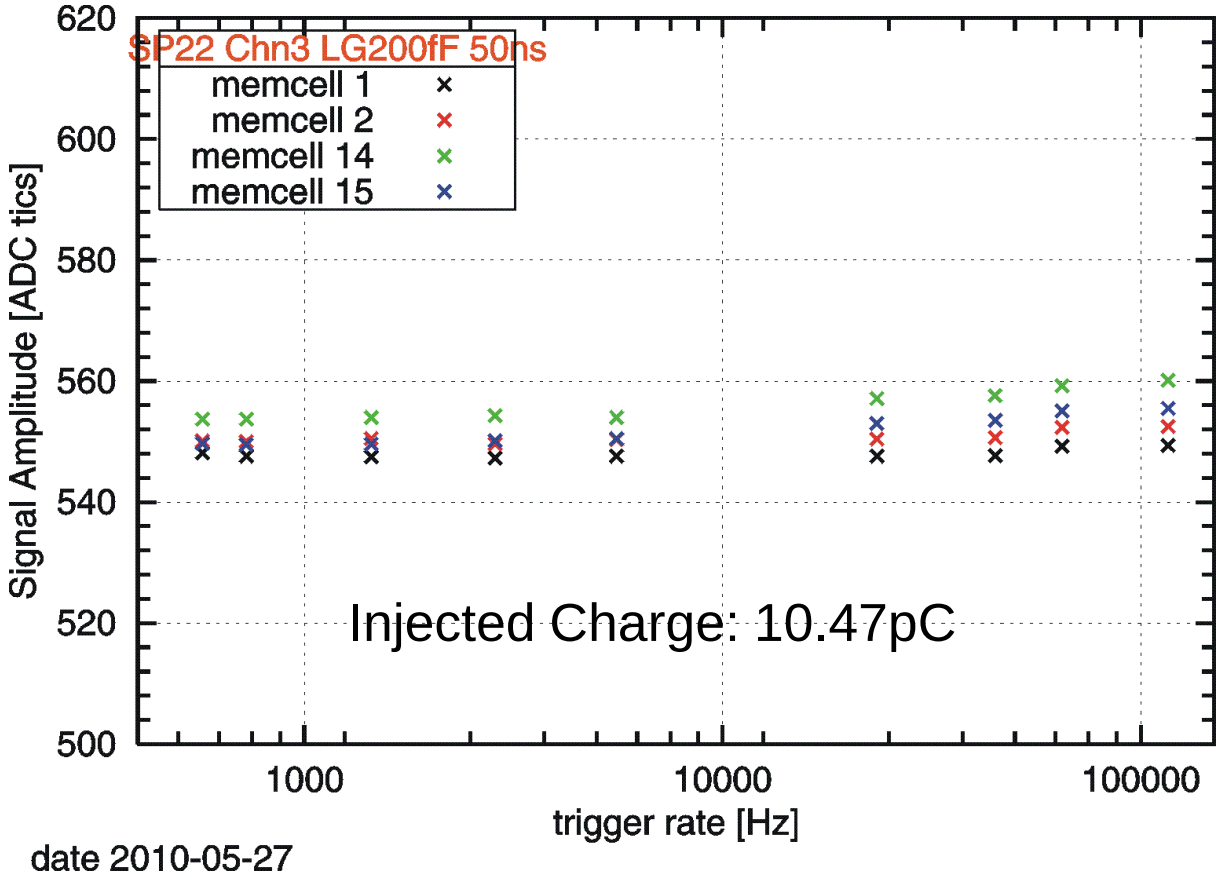
Autotrigger studies (e.g. threshold definition) currently ongoing.
Tests/studies/analysis are performed by Jeremy Rouene.




**~172 DACtics / pC**

# Rate dependency (SP22, LG, small input charge)

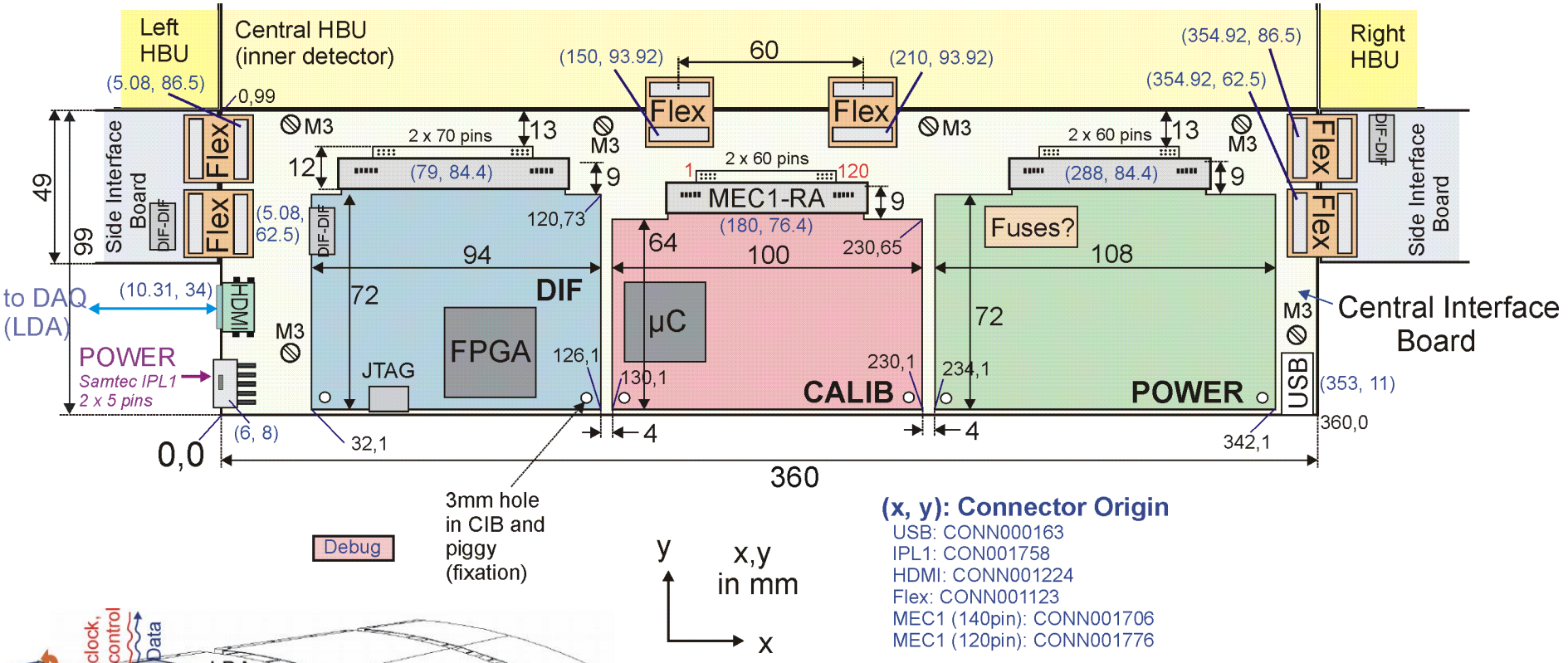



*signal on memcell1 is stored the longest time.*

No signal loss during storage in analogue memory can be observed!

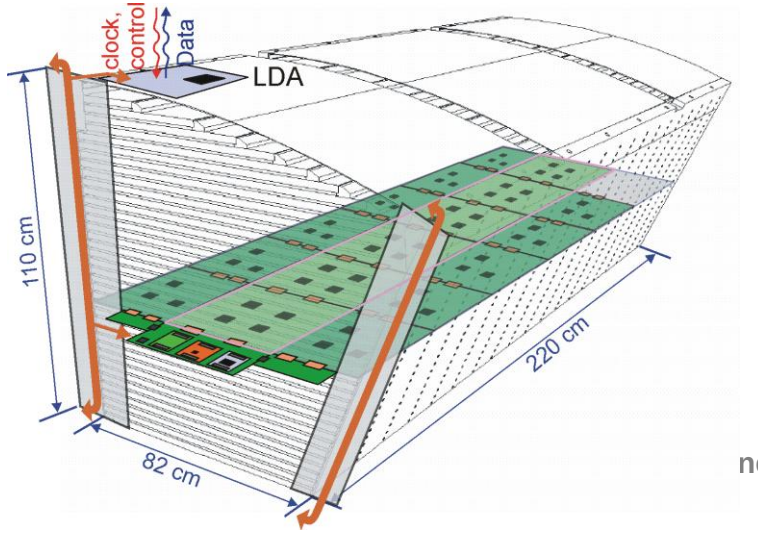
**More results on SPIROC2 tests in "electronics/DAQ" session (there are quite some unknown effects that need clarification).**

# New generation's modules



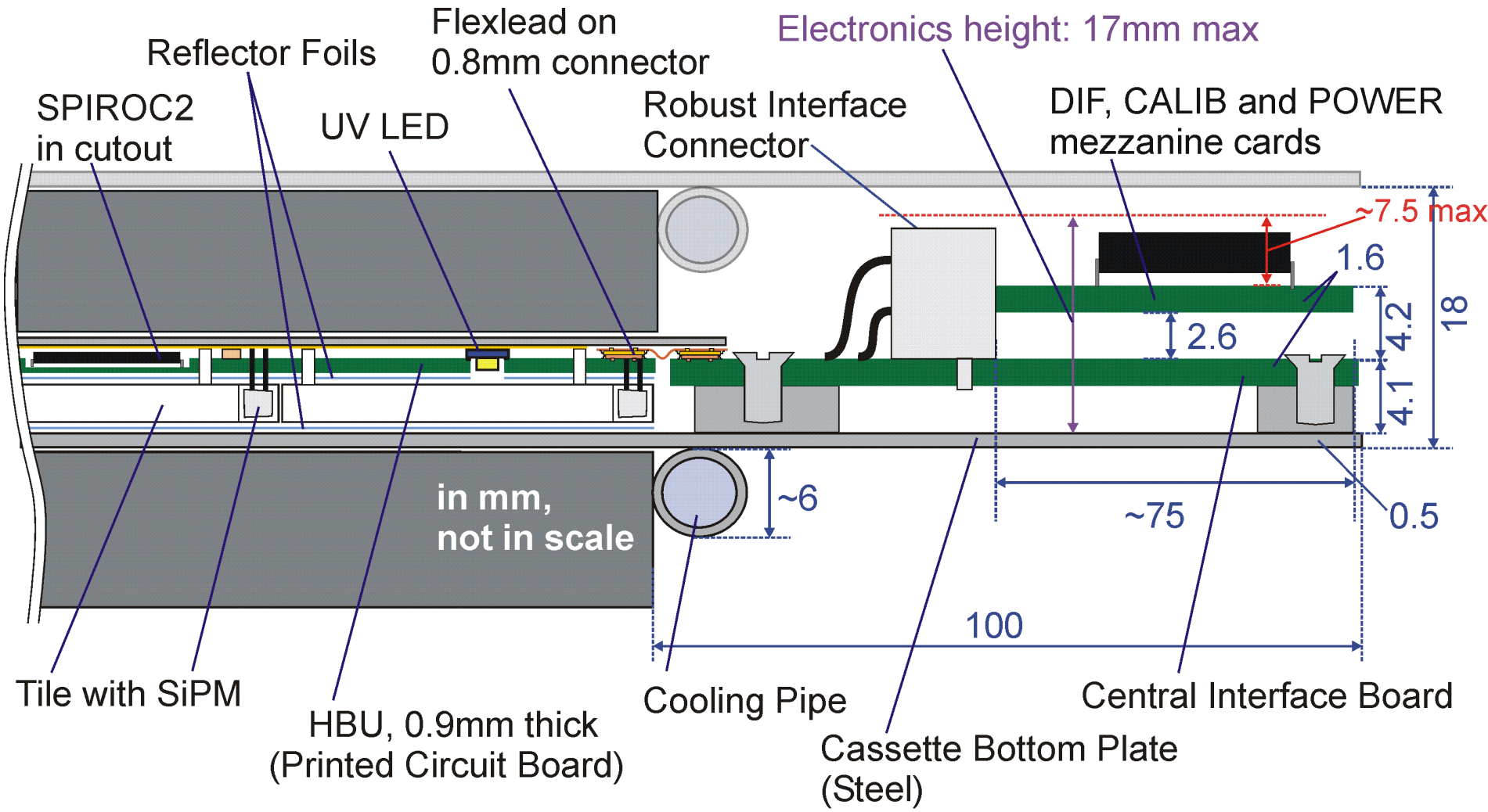

**(x, y): Connector Origin**

USB: CONN000163
IPL1: CON001758
HDMI: CONN001224
Flex: CONN001123
MEC1 (140pin): CONN001706
MEC1 (120pin): CONN001776




Designs to be done:
CIB, SIB, DIF, CALIB2, POWER2,
HBU2, (Flexleads)

# AHCAL Layer – Cross Section (Height Limitations)




**Compliant with Steel and Tungsten options.**

# Status Redesigns

| | DIF | CALIB2 | POWER2 | HBU2 | CIB | SIB | Flexleads |
|---|---|---|---|---|---|---|---|
| concept dev., circuit design | X | X | X | X | X | X | X |
| schematic entry | NIU | X | X | X | X | X | X |
| Layout | NIU | X | X | X | X | X | X |
| Production | NIU | X | X | X | X | X | X |

X done

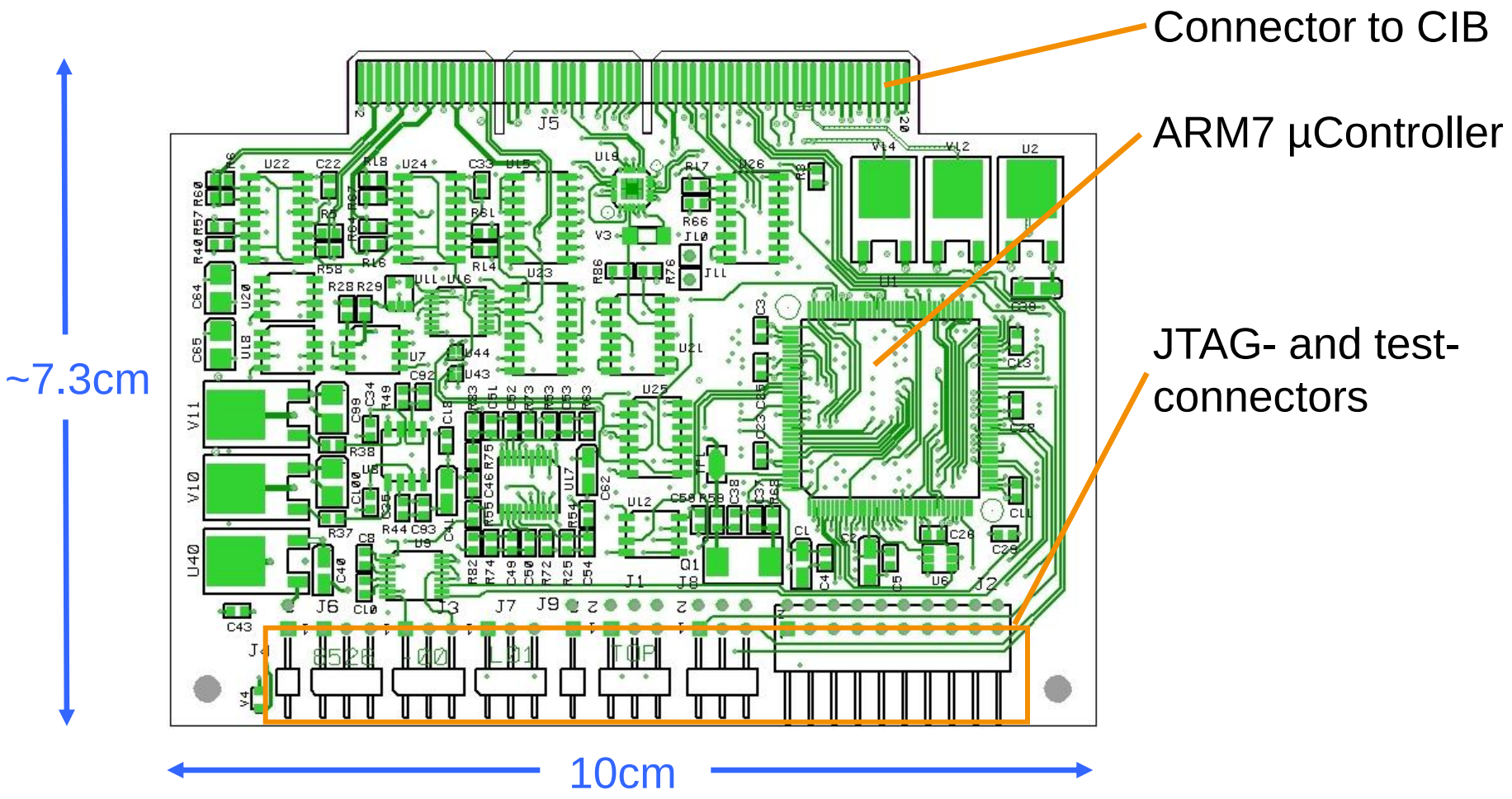
X in preparation

X not started yet

- Most critical part: HBU2 (depends still on results from ASIC tests, input from Wuppertal and Prague, complex PCB production).
- SIB is not needed for layer module => delayed.
- all modules needed for EUDET layer-module.

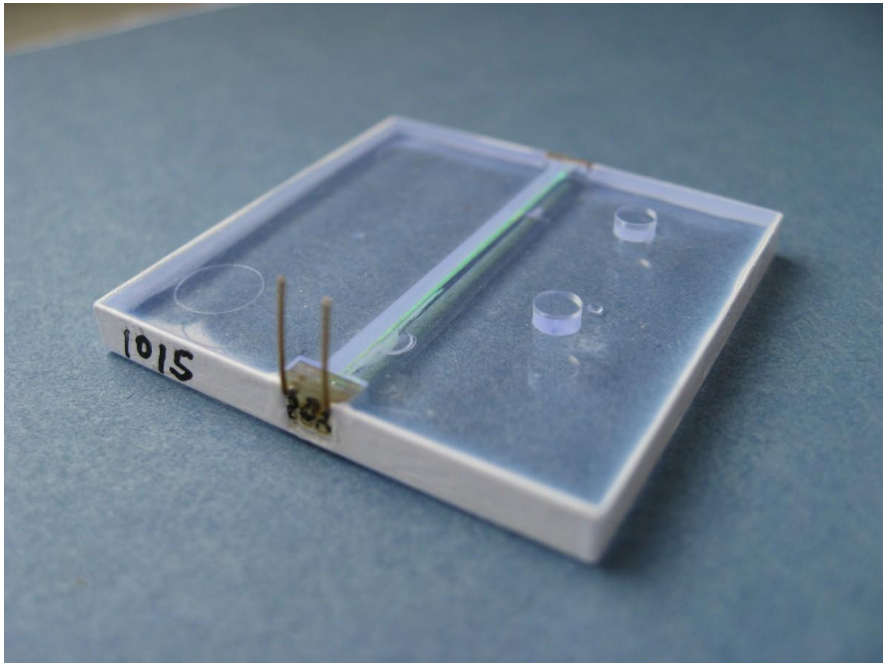
*DESY Redesigns:*
*M. Zeribi, H. Wentzlaff, M. Reinecke*

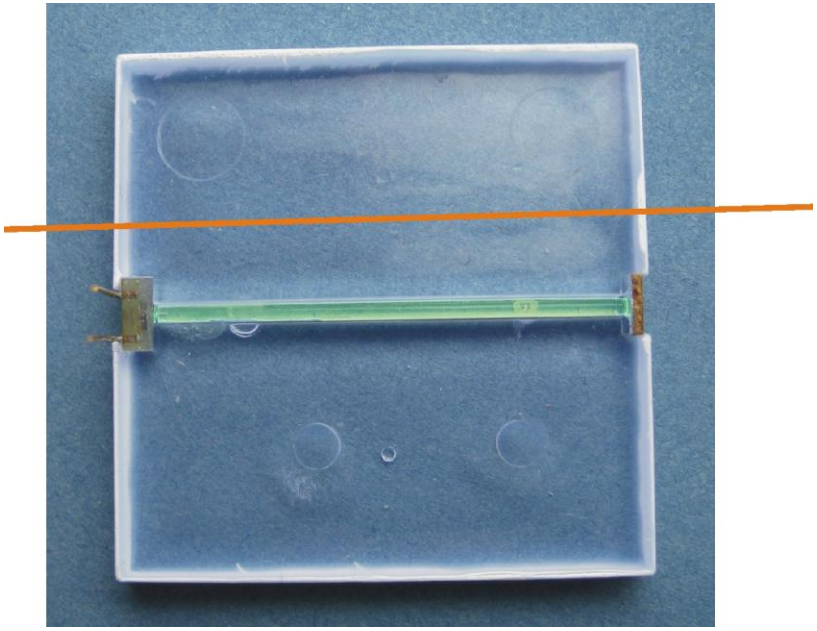
# CALIB2 module (in production)



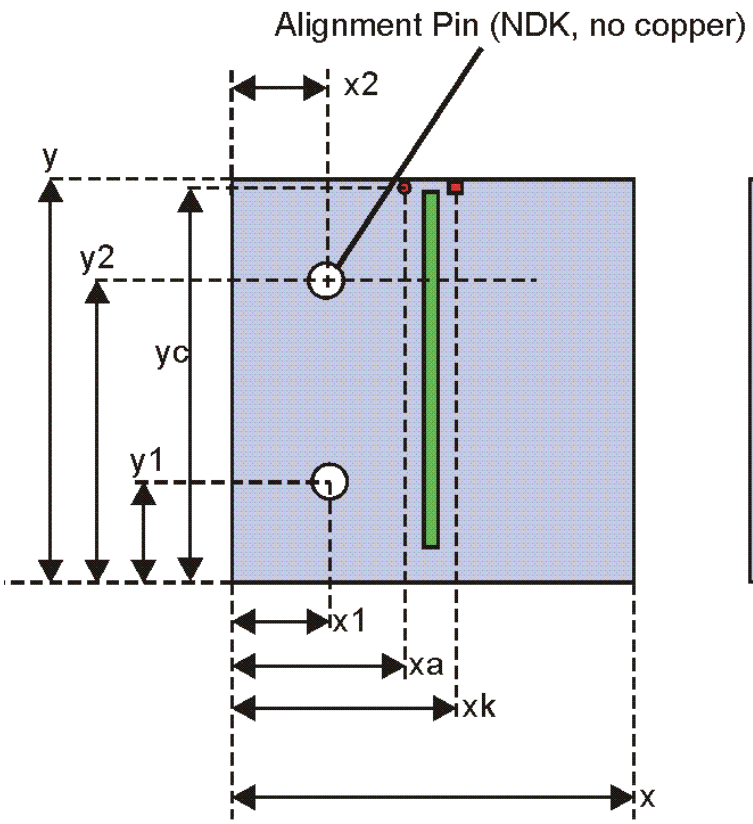
# EUDET Tiles

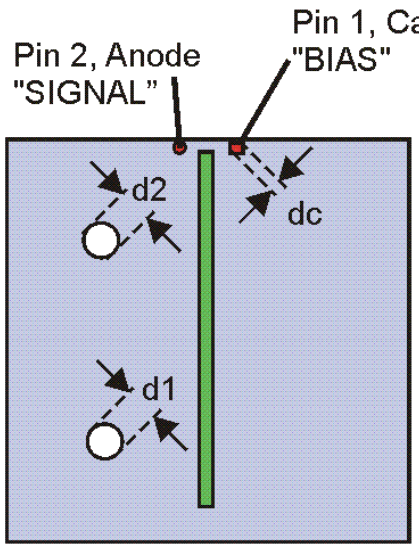
The first 50 have arrived from ITEP in Hamburg – Thank You!!!

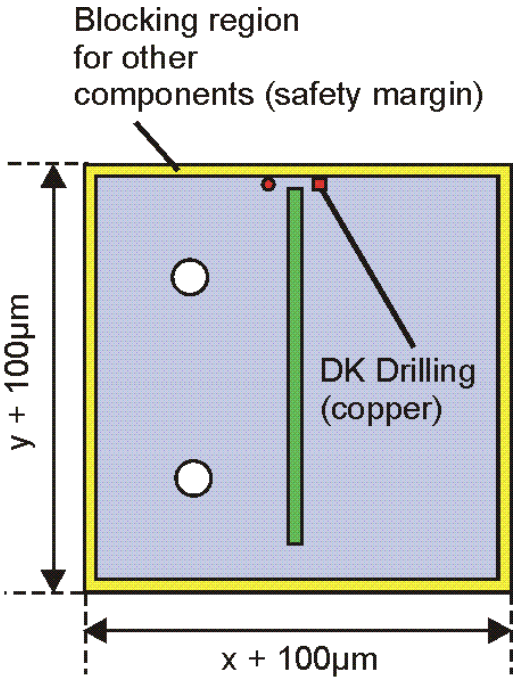


# EUDET Tiles - Dimensions




**Nominal tile distance: 100 µm**

Tile will be plugged to the PCB's bottom side.
View here: Looking from top 'through' the PCB to the tile's top side.

# EUDET Tiles – Definition for HBU redesign

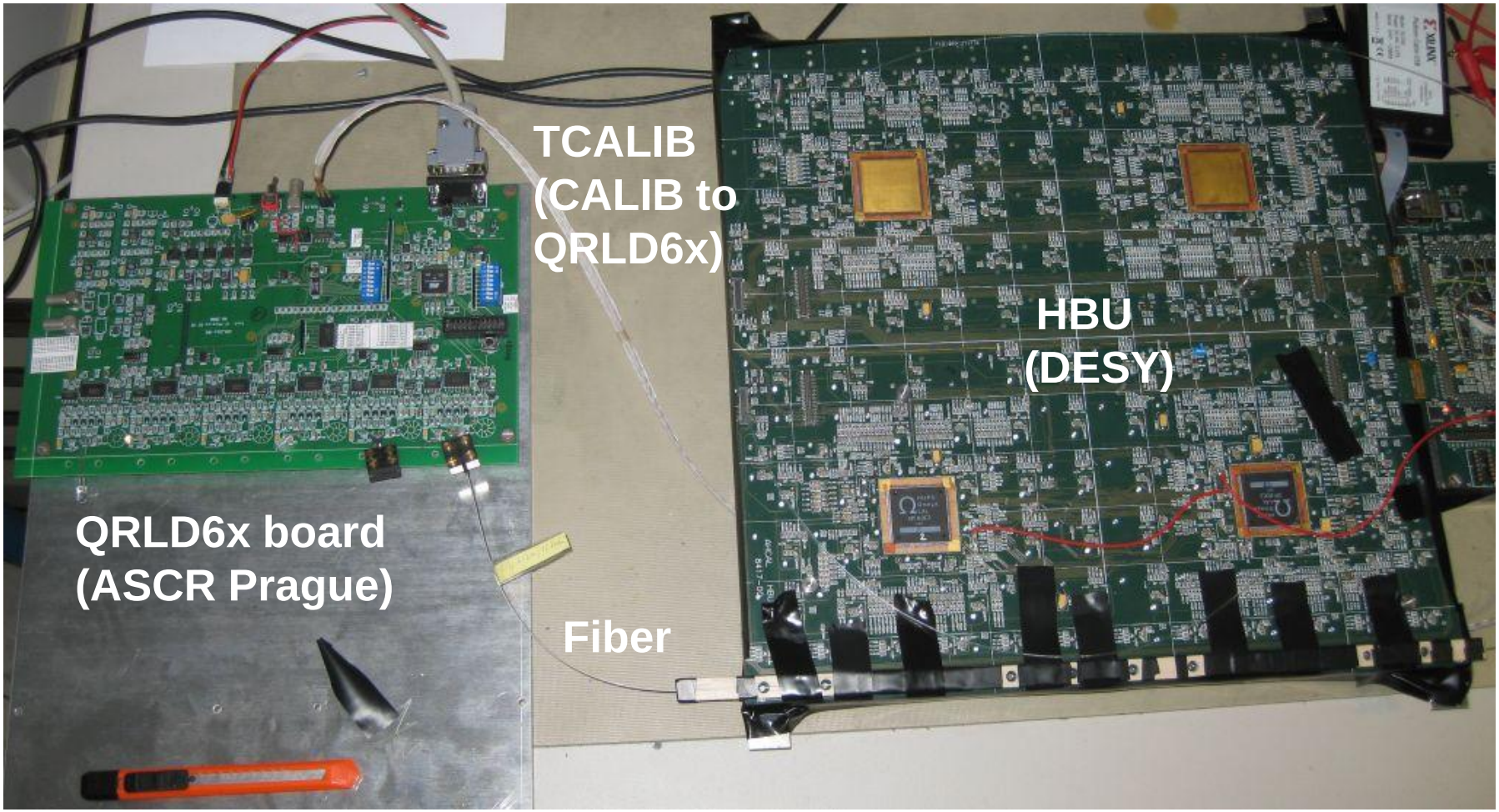
| dimension | value (mm) | remark |
|---|---|---|
| x | 30.05 | including passivation (white border) |
| y | 30.05 | including passivation (white border) |
| x1 | 7.58 | average value from 50-tiles-measurement |
| x2 | 7.61 | average value from 50-tiles-measurement |
| y1 | 7.59 | average value from 50-tiles-measurement |
| y2 | 18.59 | average value from 50-tiles-measurement |
| xk | 16.22 | xpd = xa-xk = 2.49mm |
| xa | 13.73 | xpd = xa-xk = 2.49mm |
| yc | 29.9 | y minus half SiPM pin width.<br>SiPM pin width = 0.3mm |
| d1 | 2.55 | Loose Fit. Alignment Pin Width = 2.5mm |
| d2 | 2.55 | Loose Fit. Alignment Pin Width = 2.5mm |
| dc | 0.75 | Compensates all mechanical tolerances.<br>SiPM Pin Width: 0.3mm |
| green fiber | width: 1mm | only for clarity (not needed for HBU design) |

- If dimensions of tile-series production differs from this table, the tiles won't fit into the HBU.
- New strategy for dimension-checking: **See Karsten Gadow's talk!**

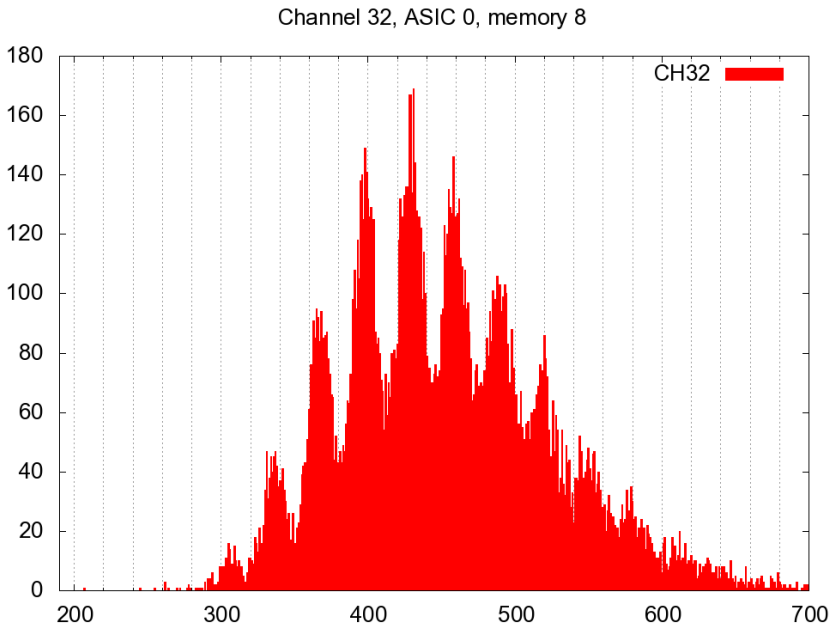


DESY

# LED Calibration Systems I – ASCR Prague



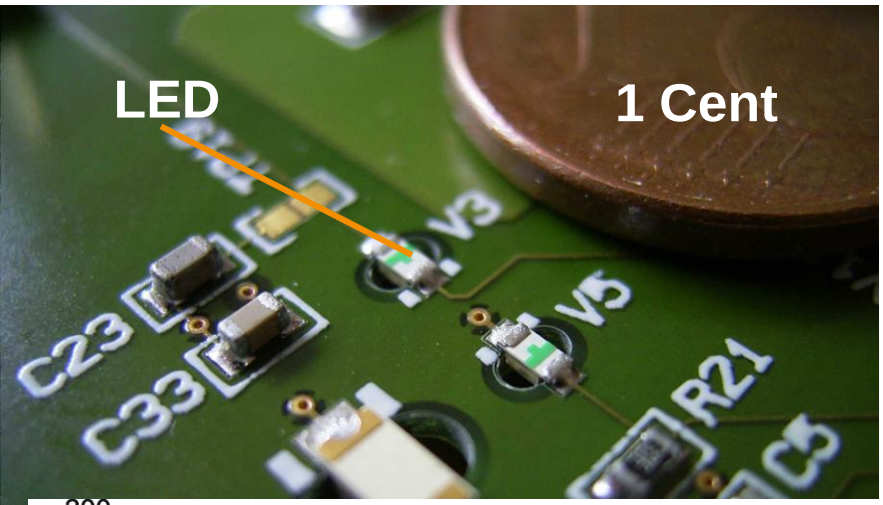
# LED Calibration Systems I – ASCR Prague

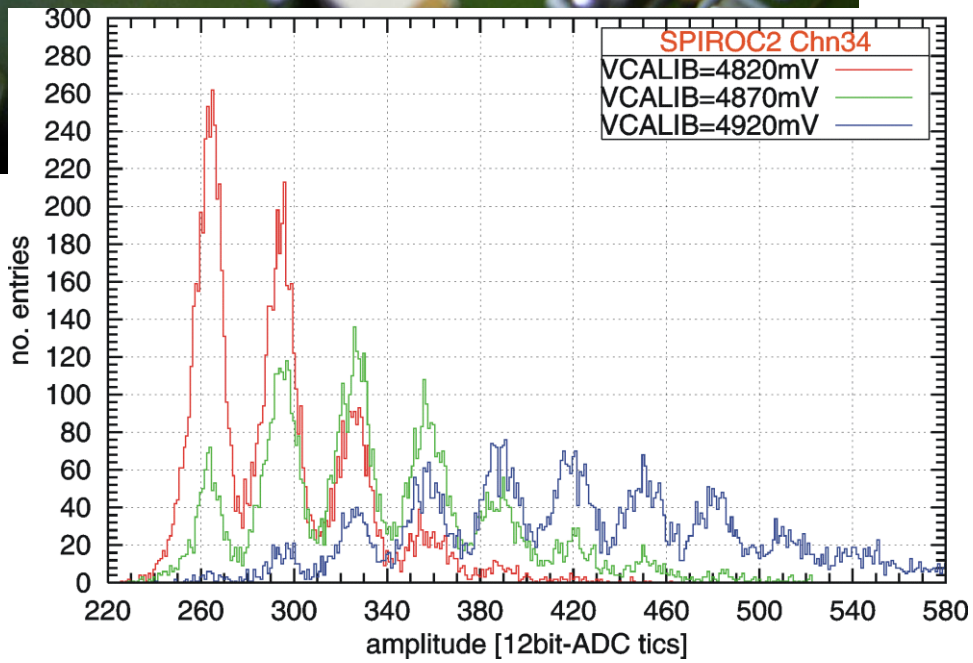



- Dynamic range under investigation.
- HBU2 will have room for 3 fibre rows
- CALIB2 triggers the QRLD6x
- Problems: fiber routing, channel uniformity, dynamic range

See next talk!!

# LED Calibration Systems II – DESY + Uni Wuppertal




- LED uniformity under investigation (see Julian's talk).
- Wuppertal recommended new LED driving circuit and new LED type with lower spread in output.
- HBU2 will contain solder parameter field in order to adjust LED power per channel.
- Problems: LED light output spread, dynamic range (saturation)

# AHCAL DAQ – currently still Labview and USB

- CALICE DAQ integration still not scheduled
  - hardware missing (e.g C&C to LDA, not all LDA outputs work)
  - DAQ operation/firmware: LLR did great progress, but parallel development does not make sense.
- DIF firmware structure/block definition within DIF task force
  - first step for CALICE DAQ integration
  - AHCAL DAQ runs with specified command set.
- AHCAL layer module cannot really run with USB DAQ – data taking is too slow.
- See talks from Matthew, Remi and Vincent about DAQ status/schedules. Discussion about DAQ integration strategy necessary in my opinion.

# Conclusions and Outlook

- 2 prototype setups running in parallel in Hamburg: testbeam & lab.
- redesigns are ongoing, but are delayed by ongoing system tests and a bottleneck in layouter menpower resources.
- CALICE DAQ integration strongly delayed due to situation in UK.
- LED calibration system development ongoing with 2 options.