

Omega

Status report on SPIROC chips

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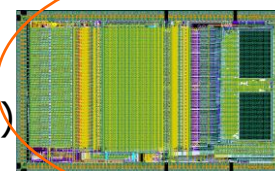


mardi 6 juillet 2010

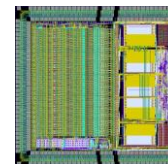
Orsay MicroElectronic Group Associated

Engineering run

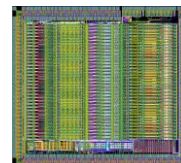
- **Reticle size : 18x25 mm²**
 - 50-55 reticles/Wafer
 - 25 wafers needed
- **Final arrangement:**
 - **« Calice » chips produced:**
 - **7 Hardroc 2b** => ~9000 chips
 - **1 Spiroc 2a** => ~1200 chips
 - **1 Spiroc 2b** => ~1200 chips
 - **1 Skiroc 2** => ~1200 chips
 - **Additional chips produced:**
 - 1 Spaciroc : JEM EUSO experiement
 - 1 Maroc 3 : for PMT readout
 - 3 Spiroc 0 (SPIROC « light » version)
=> **cost reduction** for CALICE
- **Production run launched in March**
- **Wafers sent to packaging last week**
- **Chips delivery expected => end of July**



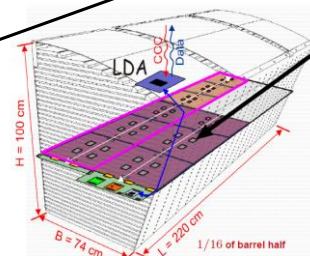
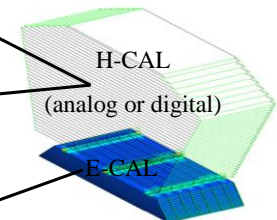
SPIROC
Analog HCAL
(SiPM)
36 ch. 32mm²
June 07



HARDROC
Digital HCAL
(RPC, μ megas or GEMs)
64 ch. 16mm²
Sept 06



SKIROC
ECAL
(Si PIN diode)
36 ch. 20mm²
Nov 06



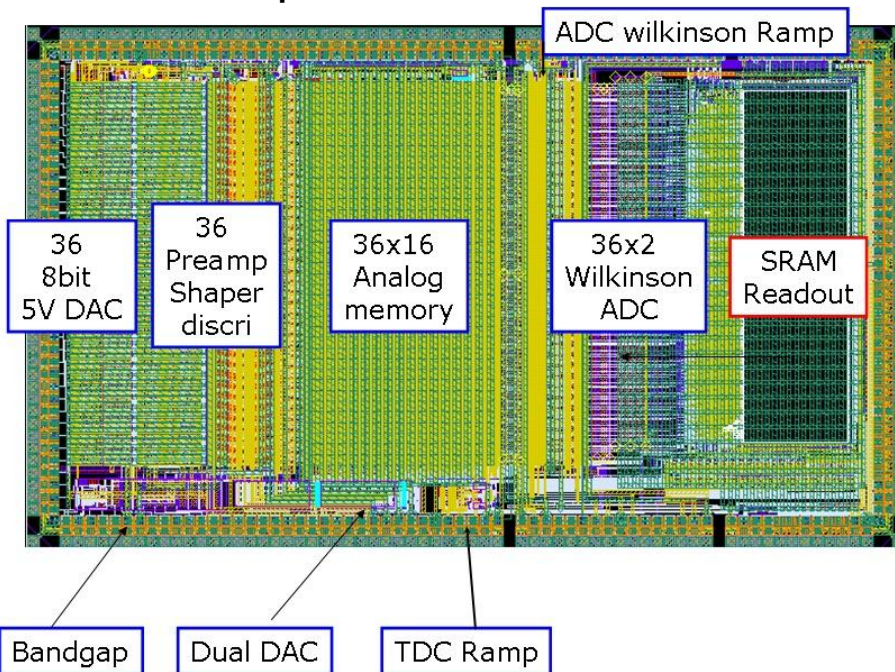
• **SPIROC chip:**
handles signal from 36 SiPM



- SPIROC Status :

- March 2010 dedicated production run: **2 SPIROC prototypes** are submitted:

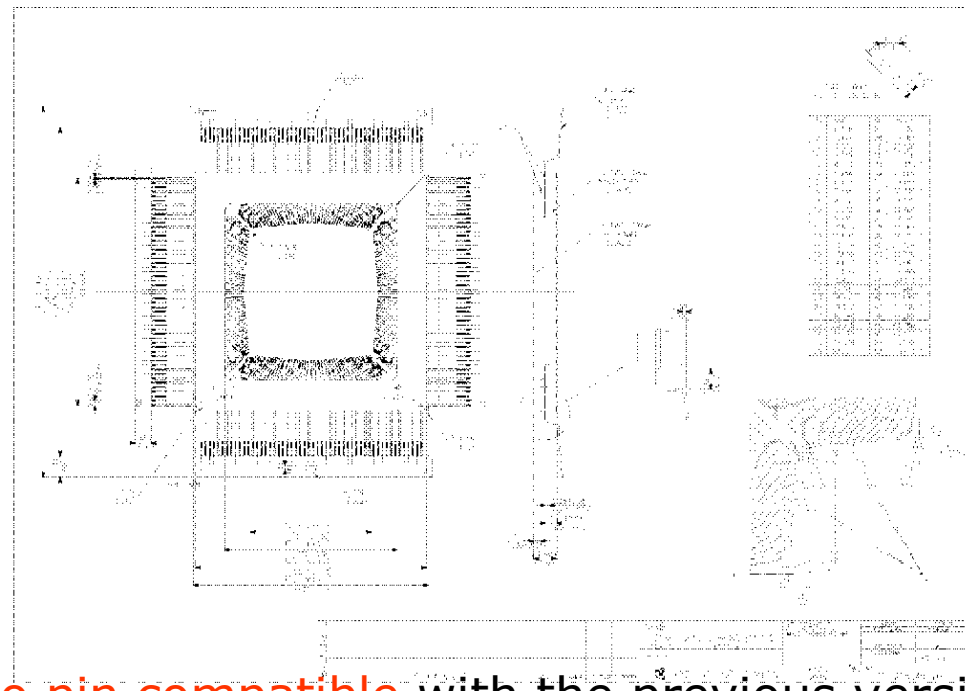
- A **conservative** prototype (SPIROC 2a) in which the major bugs of SPIROC 2 are fixed
- A **more aggressive** prototype (SPIROC 2b) in which the major bugs of SPIROC 2 are also fixed and some interesting improvements are added



Fabricated in SiGe AMS 0.35 μm
Chip area: 30 mm² (4.2mm \times 7.2mm)
Packaging : TQFP 208
36-channel ASIC
Charge measurement
Time measurement
Autotrigger on MIP or spe
Power consumption : 25 μW /channel
(in power pulsing mode)

- Packaging: TQFP 208 (made by US company I2A)

**Dimensions:
28x28x1.4 mm**

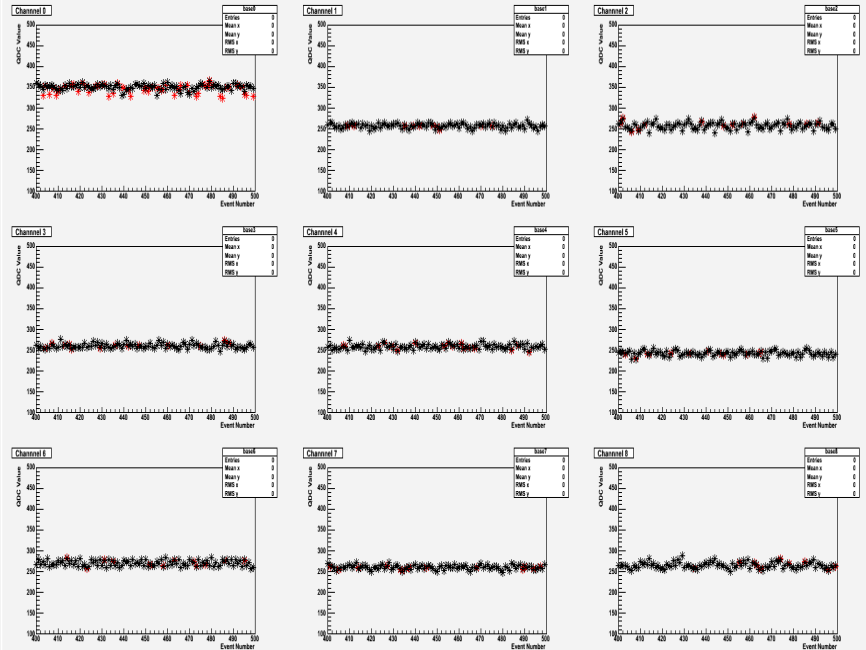
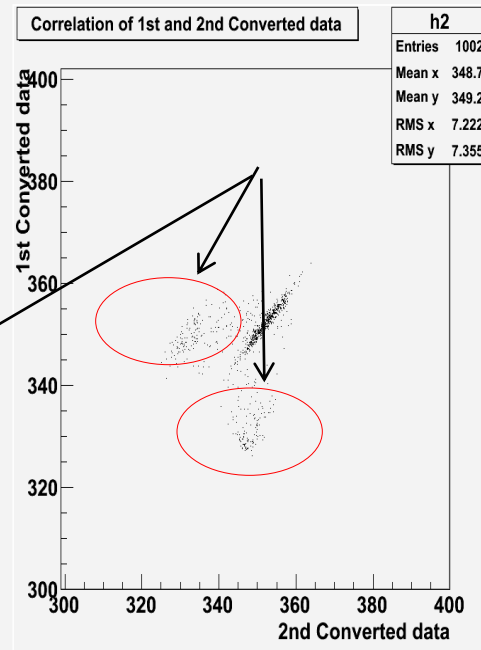
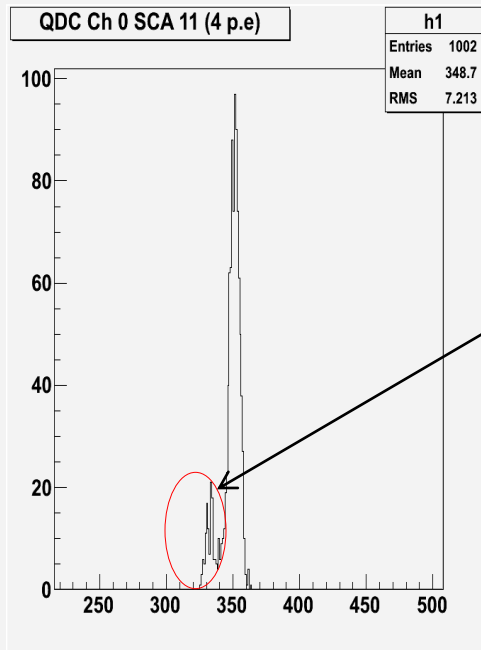
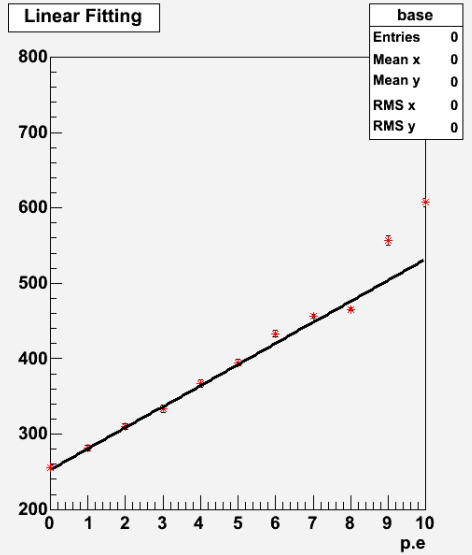
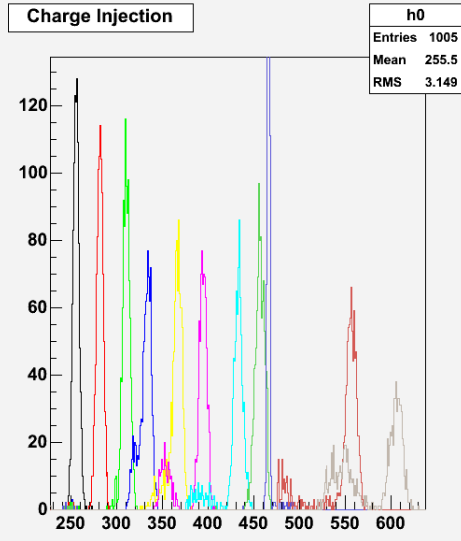


- NB: SPIROC 2a and 2b **pin to pin compatible** with the previous version except for the following pins:
 - A NC pin becomes the OR36 output (SPIROC2a and SPIROC2b)
 - The pin "pw_on_sca" and pin "pw_on_dac" have merged to liberate a pin for LVDS trig_ext signal (SPIROC2b)

Measurement on Spiroc 2



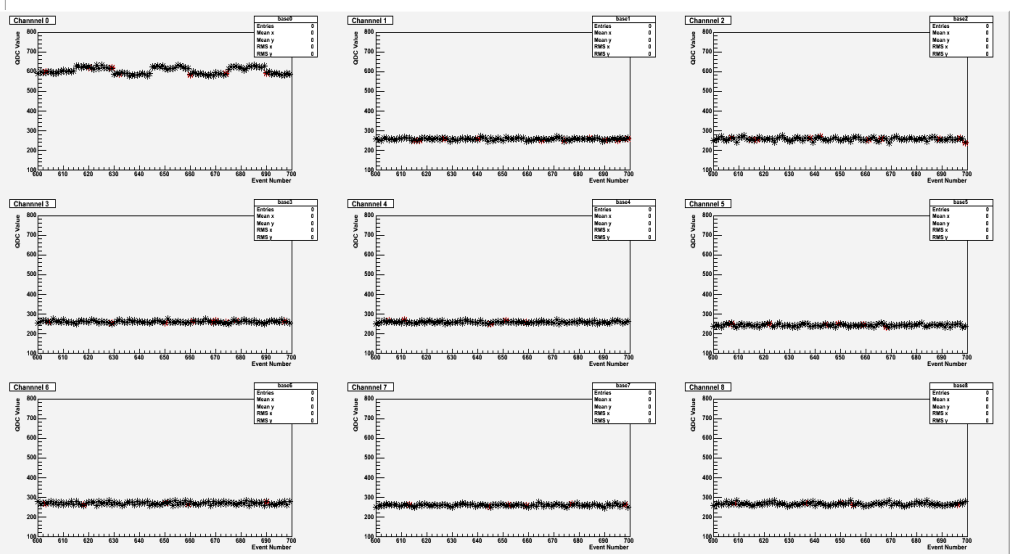
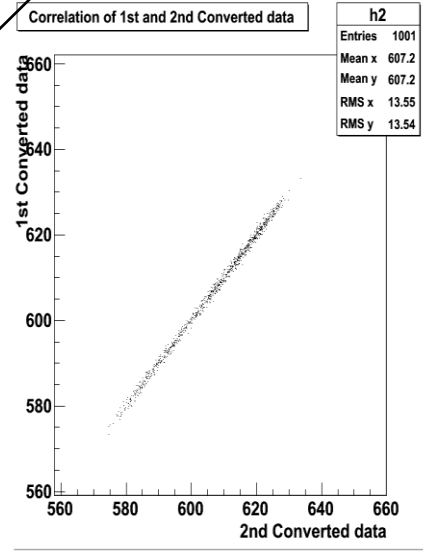
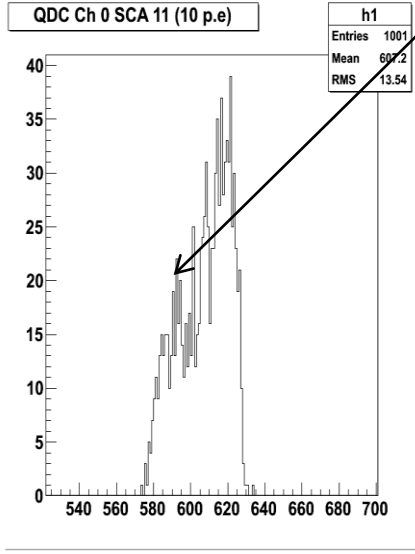
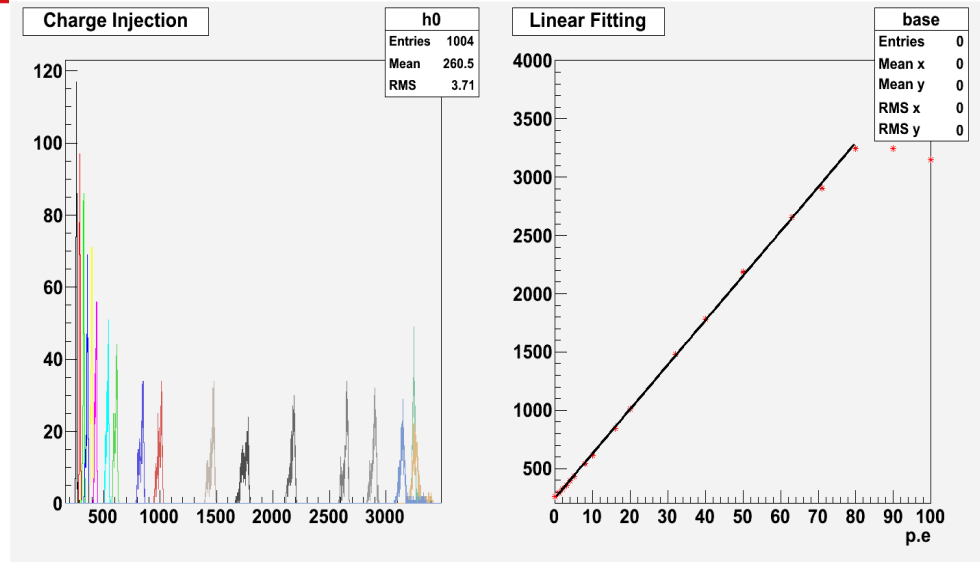
- Setup: Different charges injected in channel 0, full autotrigger mode, plot obtained on column 10 (High gain) Cf=200fF, $\tau=50\text{ns}$
- Analogue memories are converted twice by forcing the « flag_tdc_ext » signal
- Problem during conversion phase



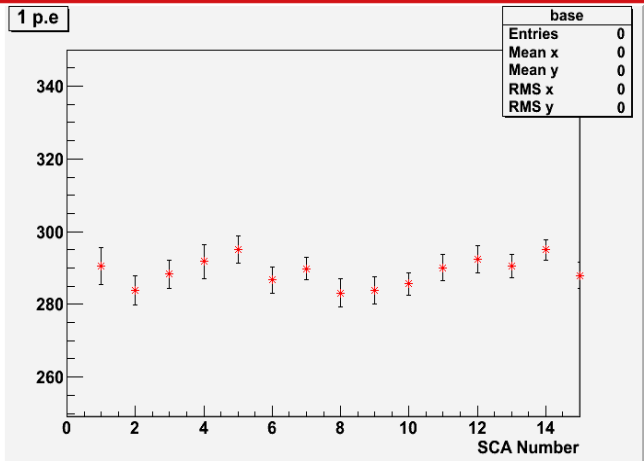
Measurement on Spiroc 2



- Setup: Different charges injected in channel 0, full autotrigger mode, plot obtained on column 10 (High gain) $C_f=200\text{fF}$, $\tau=50\text{ns}$
 - Gate added with « val_evt » signal
- To be investigated

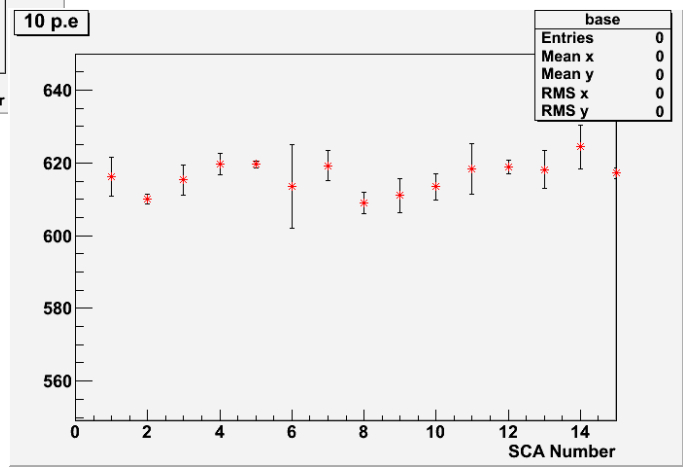
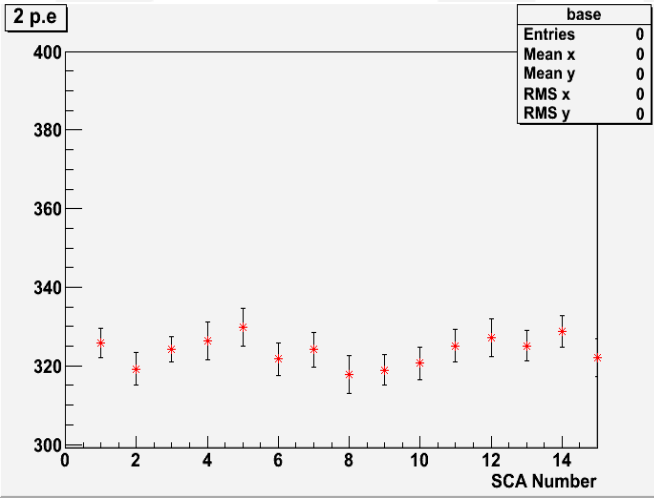
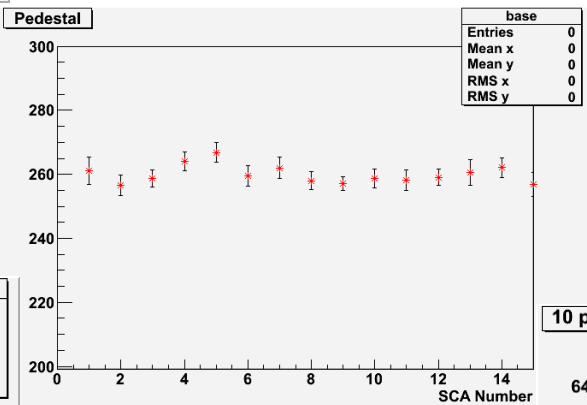
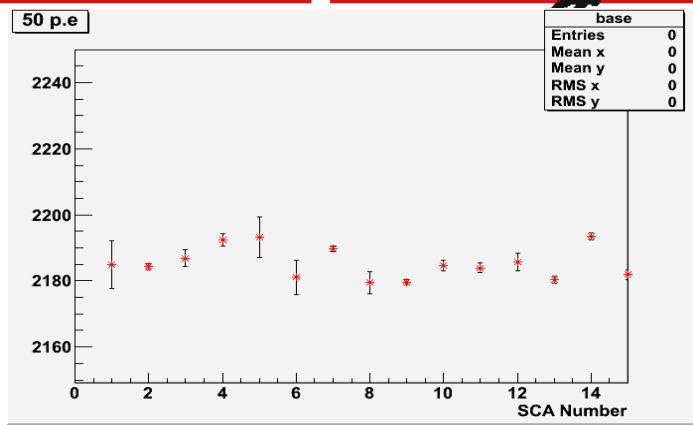


Measurements on Spiroc 2



- Setup : Different charges injected in channel 0, full autotrigger mode, plot obtained on each analogue memory

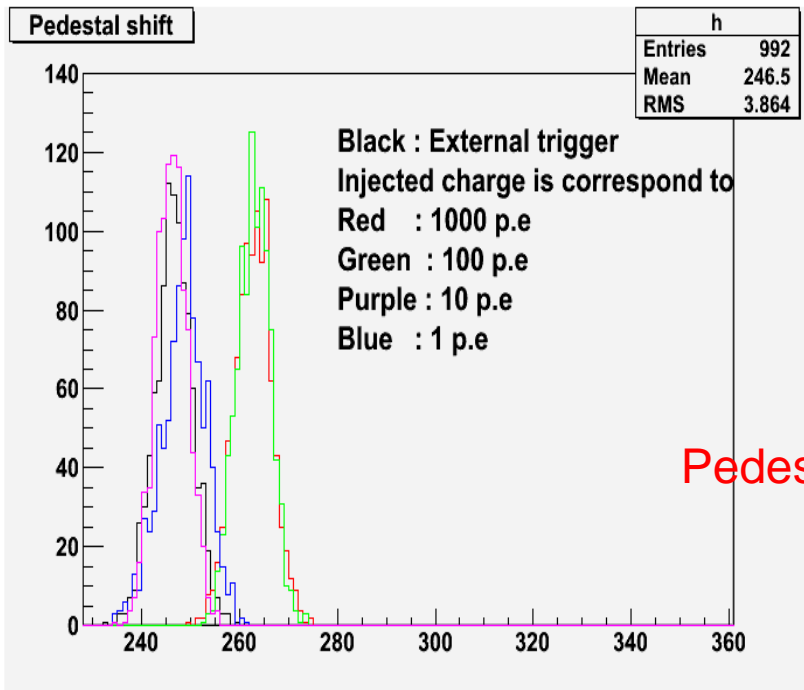
- Gate added with « val_evt » signal during acquisition phase



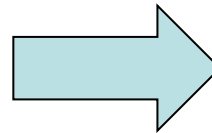
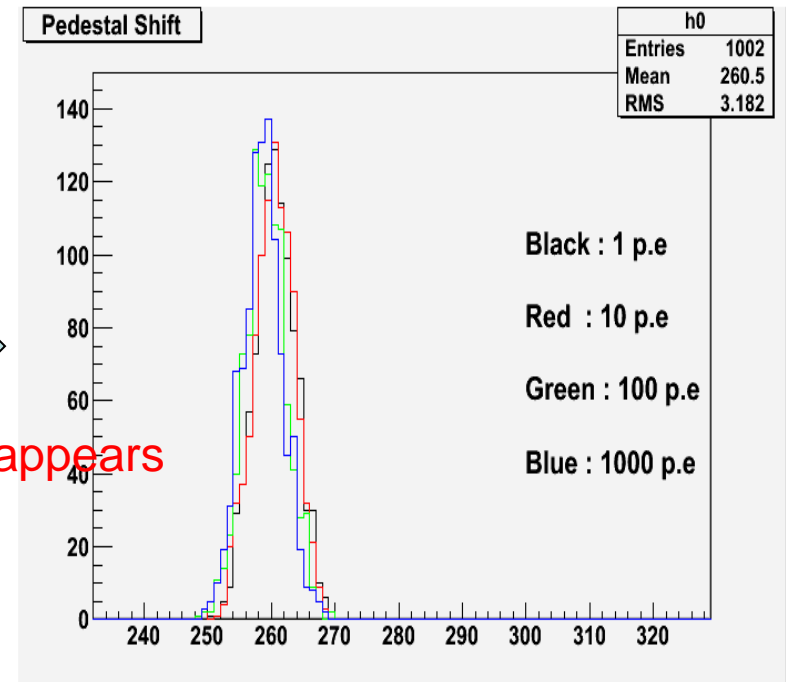
Pedestal stability issue

- Setup: Different charges injected in channel 0, full autotrigger mode, plot obtained on an other channel

Without a « gate » in acquisition phase



With a « gate » in acquisition phase



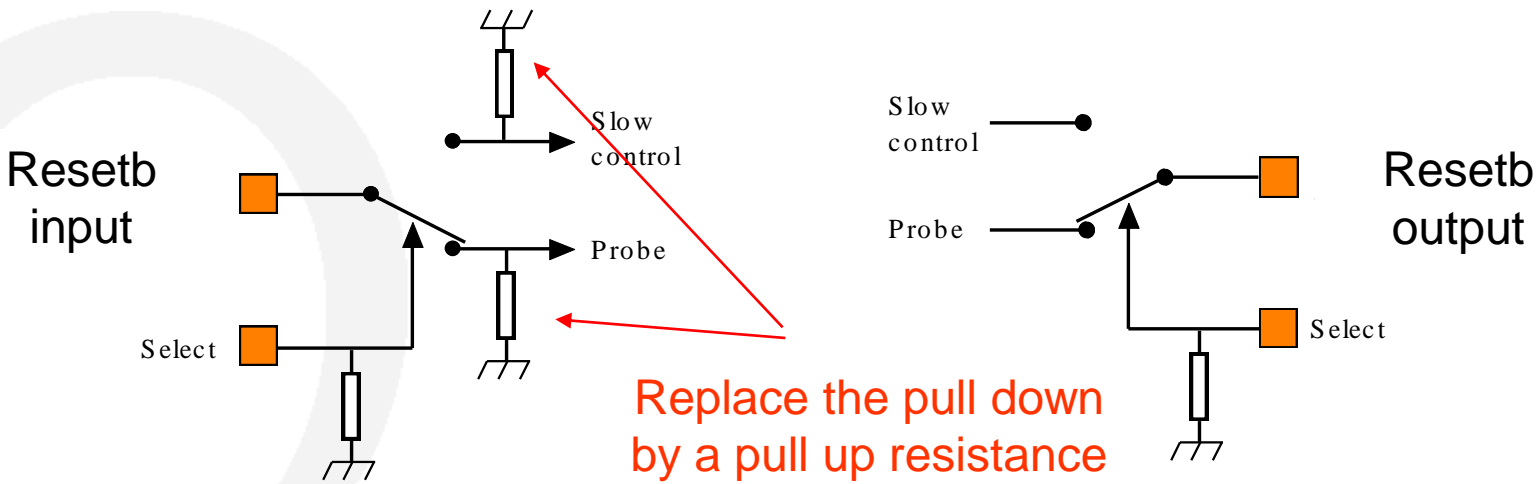
Pedestal shift disappears

- Last March 2010 : **PRODUCTION RUN**
- Schedule: Delivery expected => **next summer**
 - Wafers by end May 2010
 - Chips expected in July 2010
- SPIROC 2a chip :
 - **Conservative prototype** : major bugs fixed
- SPIROC 2b chip :
 - **Innovative prototype** with « controlled » improvements also submitted
- Both chips (almost) **pin to pin compatible with Spiroc 2**
- Measurements in collaboration with DESY group to be continued
- Some problems have to be investigated

Backup slides



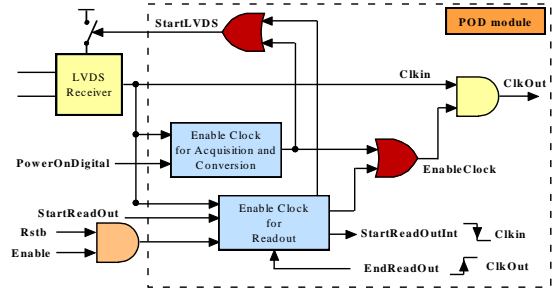
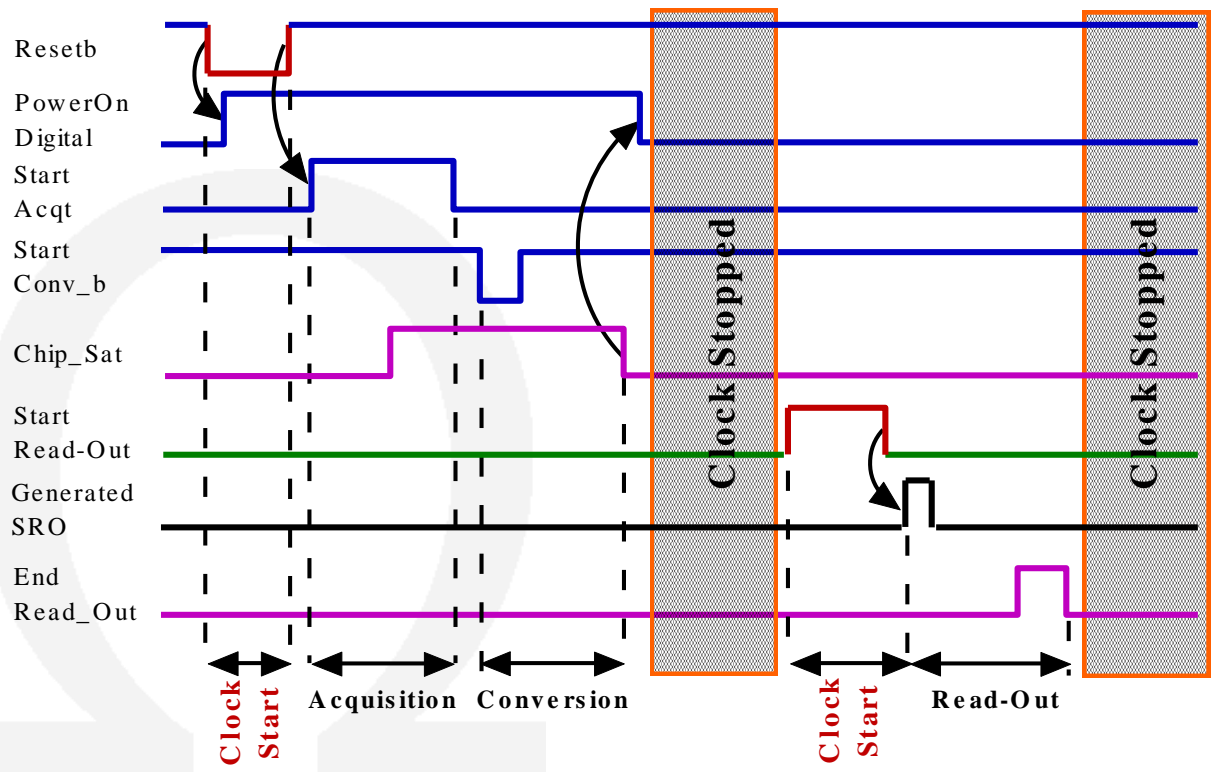
- Conservative version of SPIROC 2:
 - fix the slow control and probe bus :
 - By adding buffers in critical points as done in HARDROC2B
 - By correcting the Bug on the reset signal of the multiplexed probe and slow control register
 - » **Active low reset forced to 0 when not selected**
 - » **Intempestive reset when register is unselected**



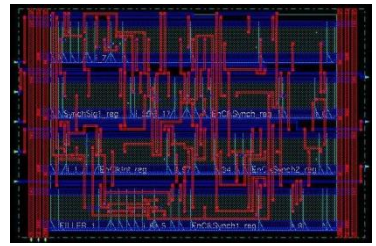
- By putting a default Slow control set-up

- Conservative version of SPIROC 2:

- add the POD module for the 2 clock LVDS receivers to reduce idle power dissipation (already tested on Hardroc2)



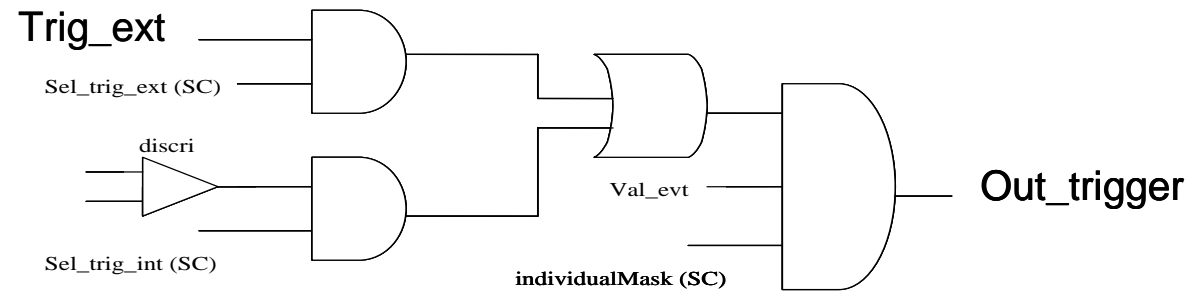
- Calibrated (LVDS start time)
- From DAQ
- From daisy chain
- From ASIC
- From POD



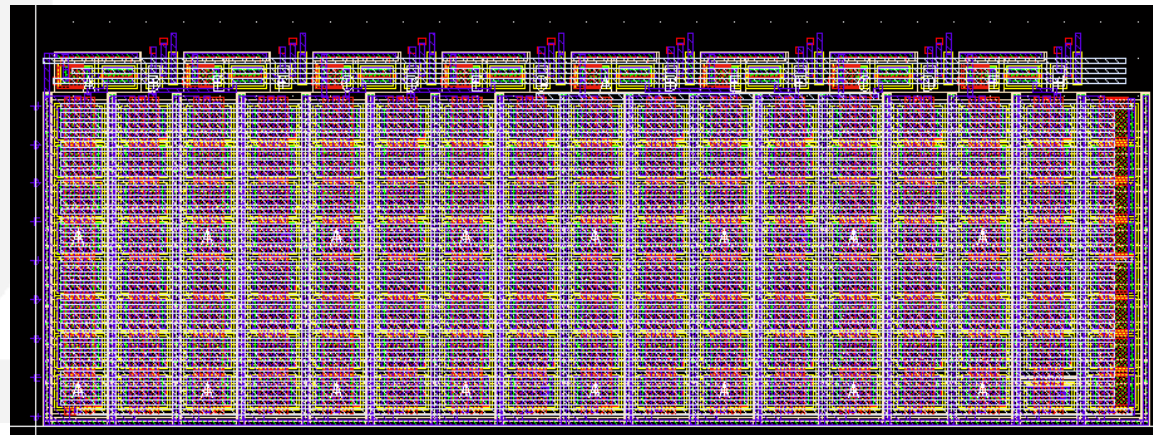
- Conservative version of SPIROC 2:
 - Put a OR36 output on a non selected pin
 - Decrease the consumption of the low gain preamplifier
 - The backup SCA is OFF when unused in order to save power



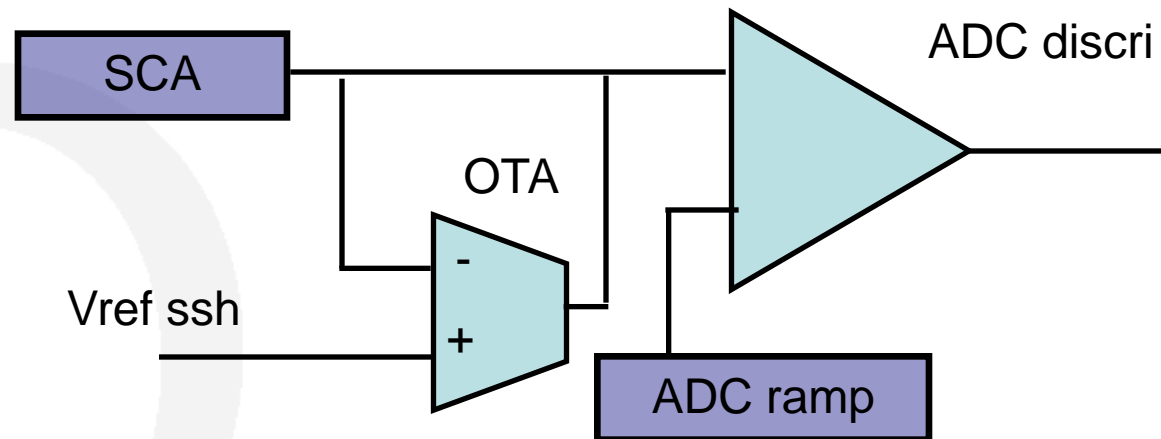
- SPIROC 2a + the following improvements:
 - 6-bit Preamplifier gain adjustment per channel (25fF, 50fF, 100fF, 200fF, 400fF, 800fF) : each preamp gain can vary from 25fF to 1.5pF with a step of 25fF)
 - External trigger input (LVDS)



- put the improved version of 8-bit input DAC with new spatial arrangement for a better matching



- SPIROC 2a + the following improvements:
 - put the improved version of threshold 10-bit DAC
 - fix the first "zero-frame" by adding an **active pull-up** to reference voltage on ADC discri input (Not implemented as expected on SPIROC 2a because the risk would be too high)



- **SPIROC 2a + SPIROC 2b + the following improvements:**
 - **New TDC to have 100 ps accuracy (just submitted last November on PARISROC 2 Chip)**
 - **Replace the ADC ramp by an optimized one**
 - **Replace the ADC discriminators by an improved one (PARISROC)**
 - **8-bit input DAC : auto-regulation with respect to detector temperature**
 - **“Powering-up mode” of SCA columns to save power:**
 - **SCA columns are powered only when they are used**
 - **New improved and optimized digital part**
 - **Possibly Wei's input stage after testing**
 - **Possibly new I2C slow control interface**