# AHCAL Electronics.

## SPIROC2 and HBU measurement results

Mathias Reinecke
CALICE ECAL/AHCAL - EUDET electronics and DAQ - AIDA
DESY, July 5th to 6th, 2010

HELMHOLTZ GEMEINSCHAFT

CALICE Calorimeter for ILC

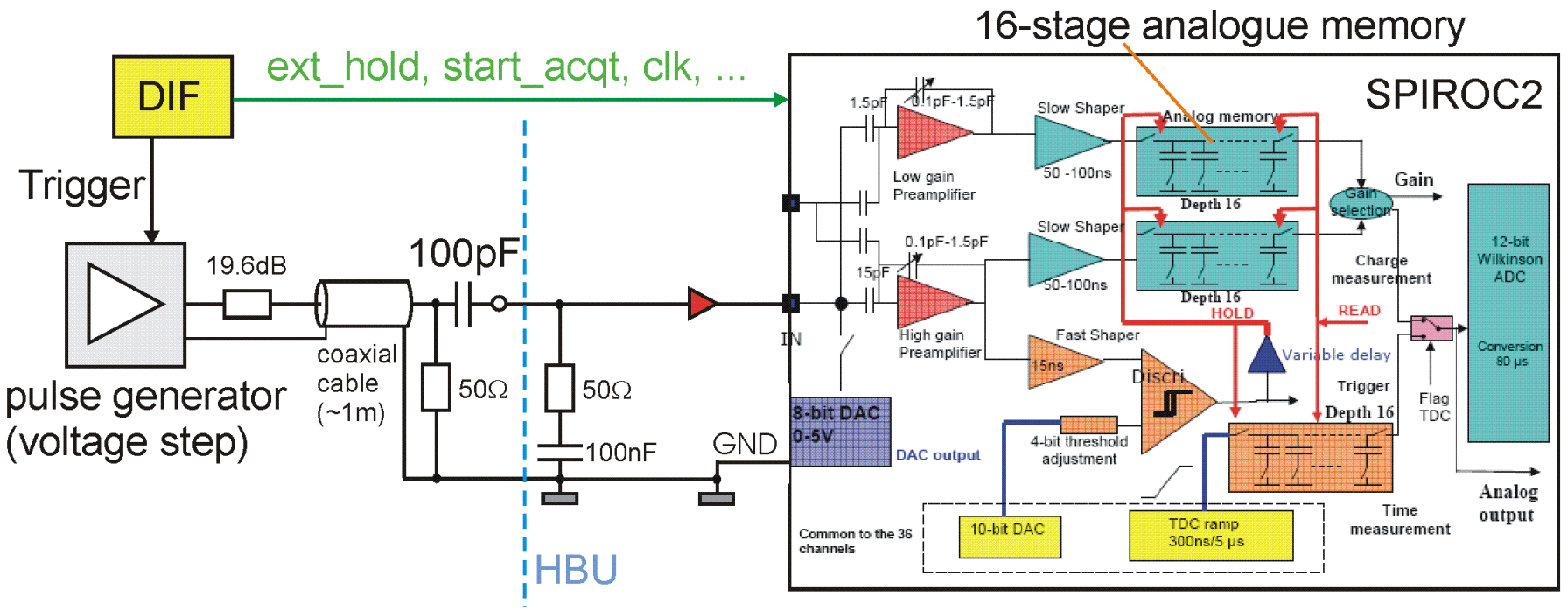
EUDET

DESY

# Outline

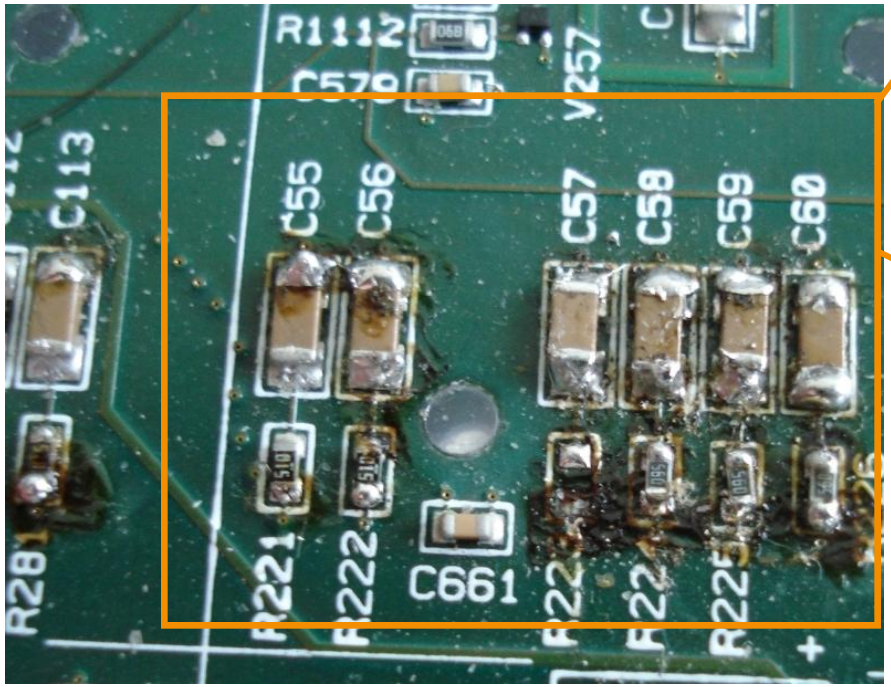
- Setup Electronics for Charge Injection
- SPIROC2 measurement results
  - Shaper Output
  - HOLD Scans
  - Autotrigger
  - Problems with first cells of Analogue Memory
  - Dynamic Range
  - Rate Dependency
- Conclusions

# Charge Injection Setup I – HBU_I in laboratory

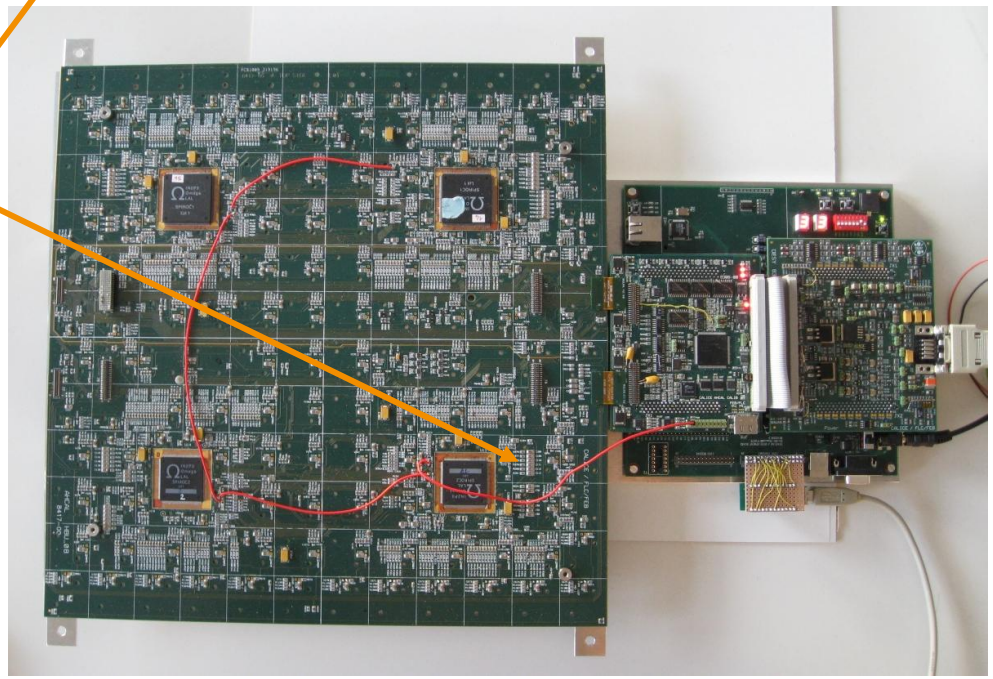



Looks like an easy setup, but ….

# Charge Injection Setup II




SiPM termination @ SPIROC2 input

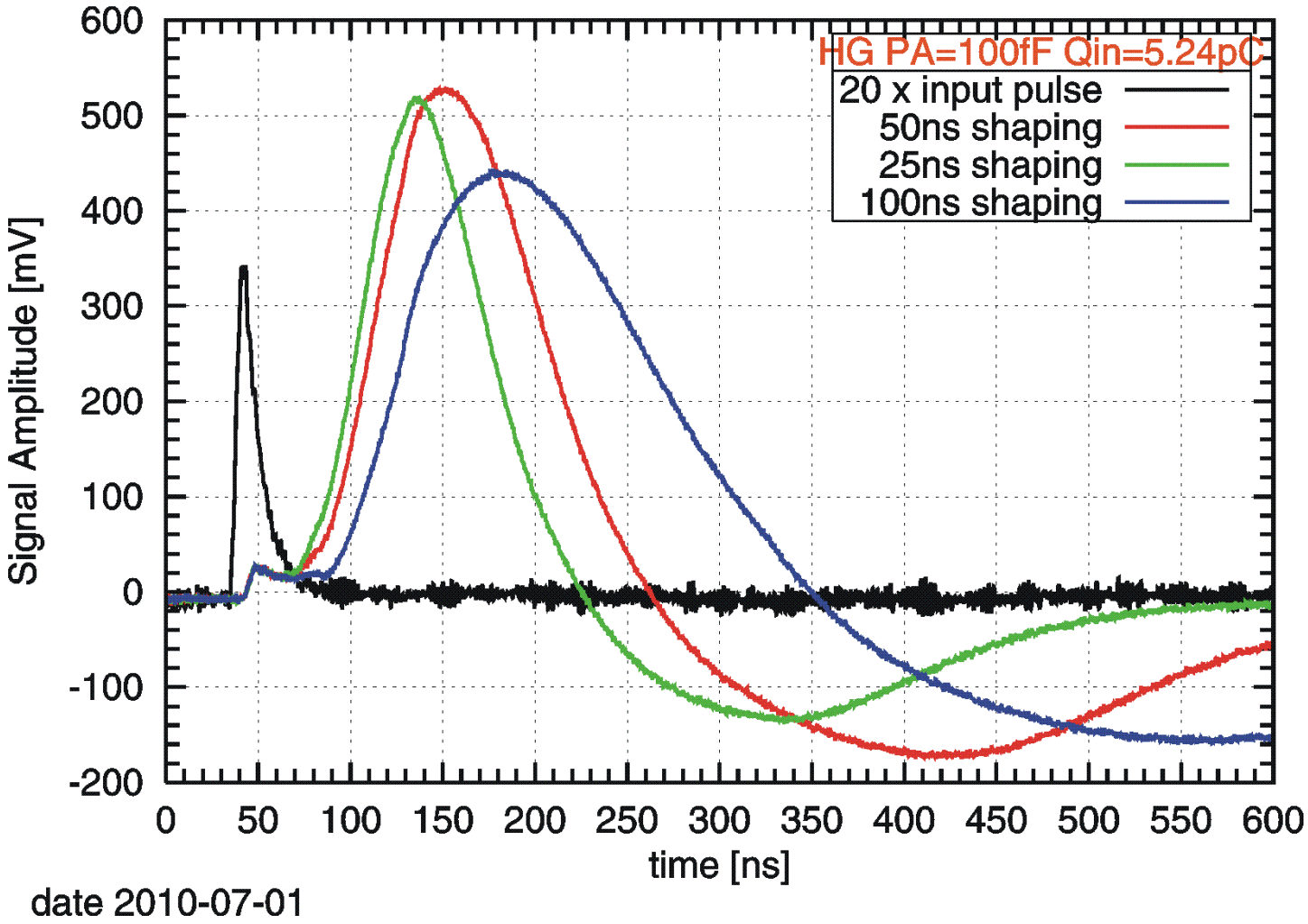


**HBU has not been designed for charge-injection tests!**

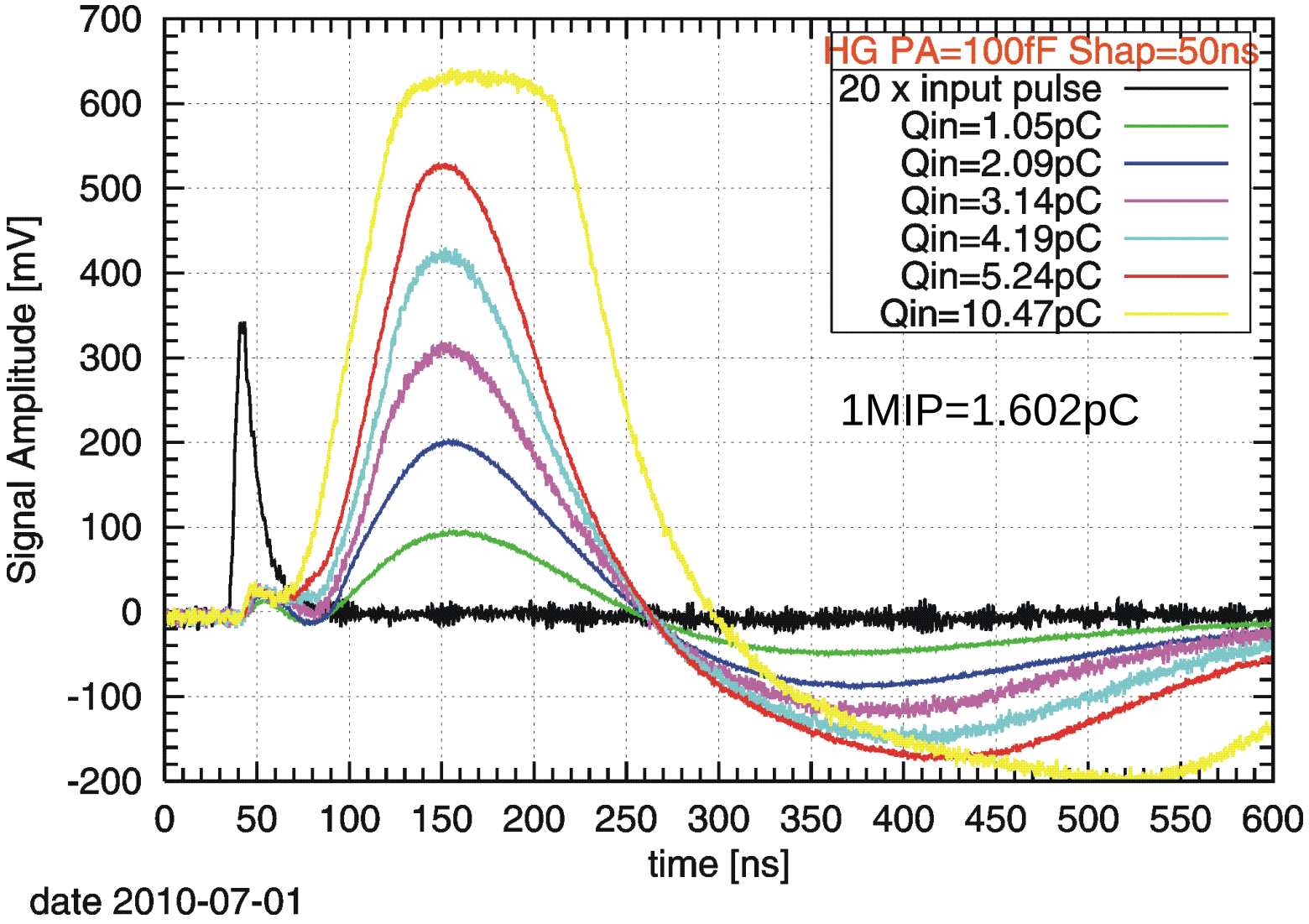
Initial Idea: Analogue SPIROC tests => LAL testboards,
HBU => tests of digital part / readout chain / DAQ / system (SiPMs)

Due to new effects: HBU is used for analogue tests as well…

# SP2 Shaper Output (Analogue test output)

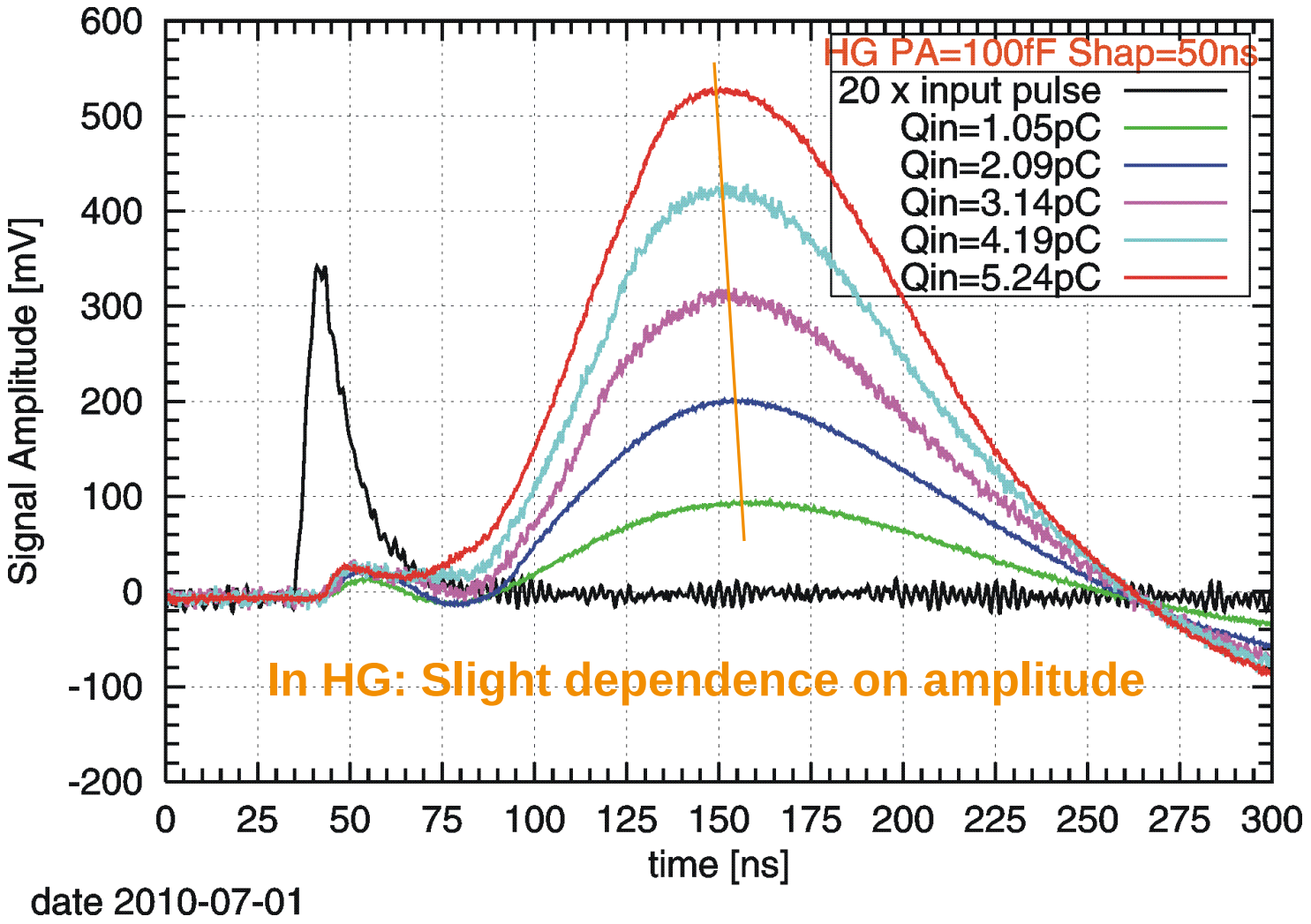


# SP2 Shaper Output (Analogue Testoutput)

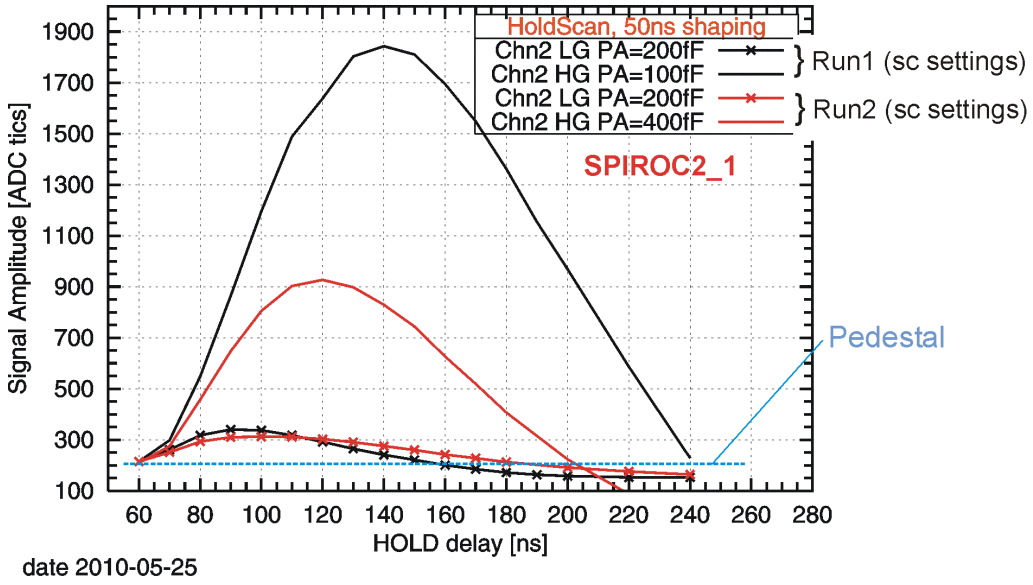


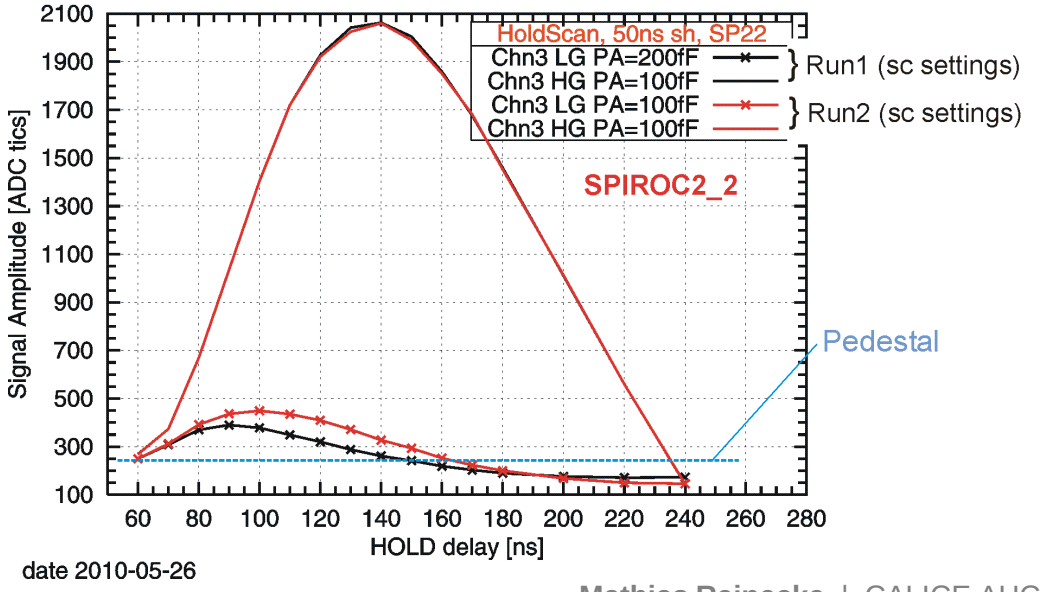
# SP2 Shaper Output (Analogue Testoutput)

*Zoom of last plot*



# SPIROC2 HOLD Scans – External Trigger



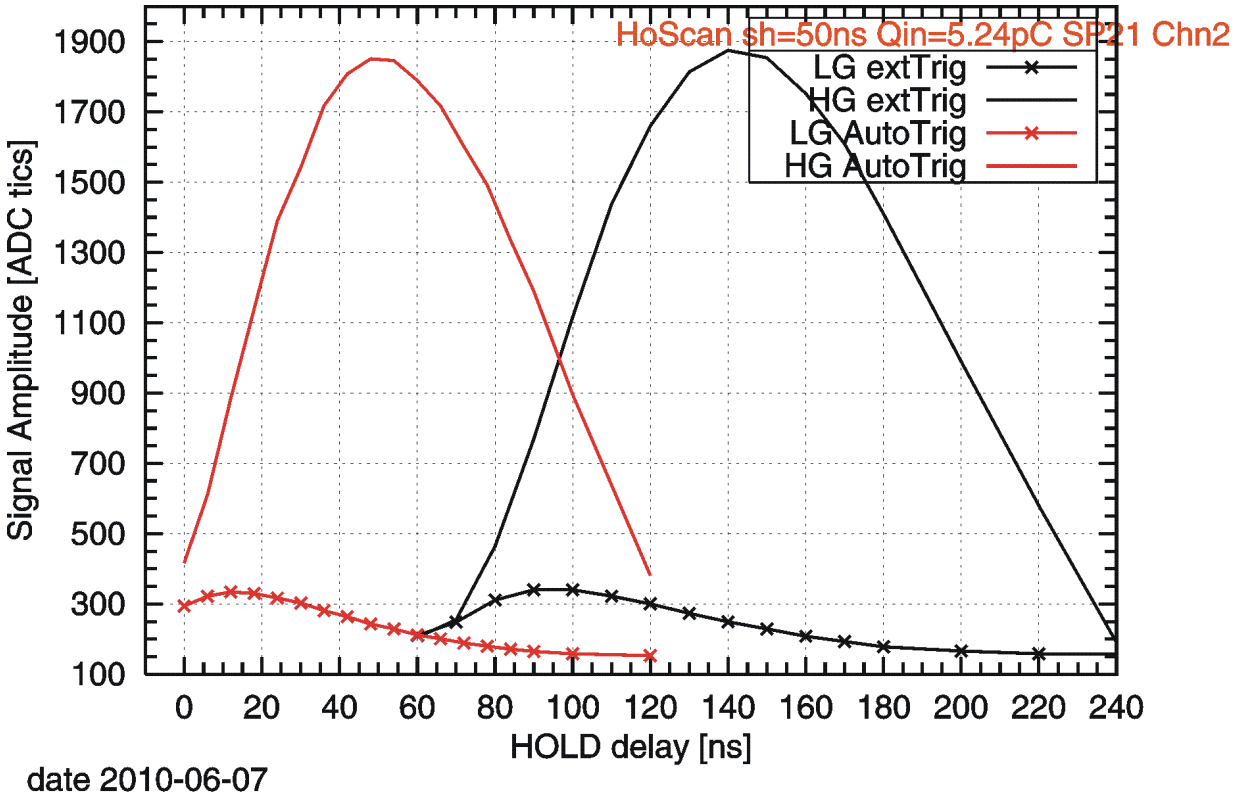

Maximum in HOLD Scans

- is different for HG and LG
- depends on PA feedback cap.
- depends on signal amplitude (not shown here)

*Results are confirmed by LAL, effects can be seen in measurements but not in simulation.*

# SPIROC2 HOLD Scans – Internal Trigger (Autotrigger)

‘Autotrigger’: Most important operation mode for SPIROC2 => ‘ILC mode’



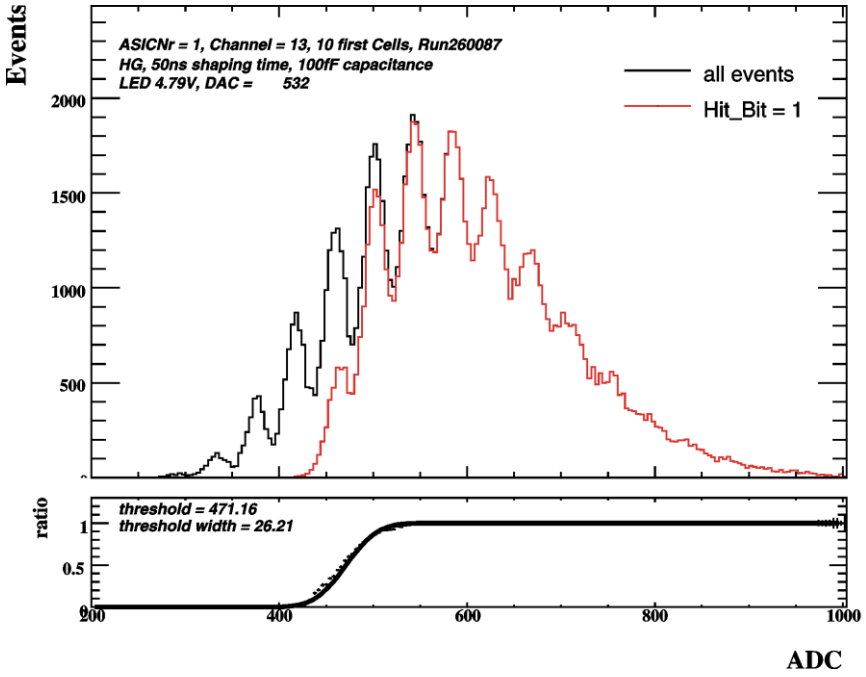

Autotrigger hold delay: 2ns per 6-bit-tic in slow control data.

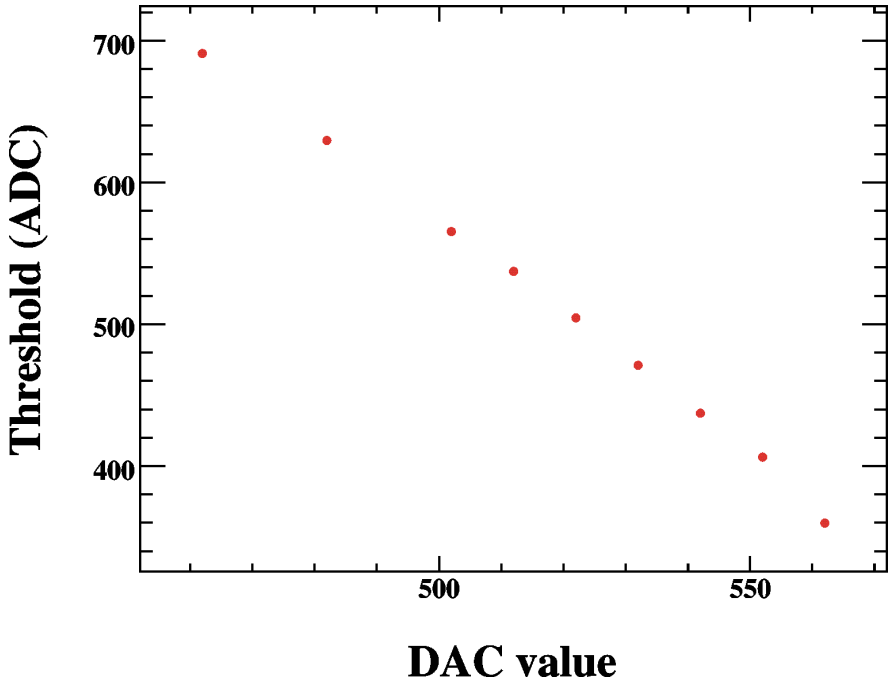
Results for Autotrigger agree with the external trigger results.

# Autotrigger Threshold Adjustment

Aim: Understand how to set the Autotrigger threshold DAC for an input charge, and the autotrigger behaviour

Step 1: Use **external trigger** and analyze the **Hit-Bit**

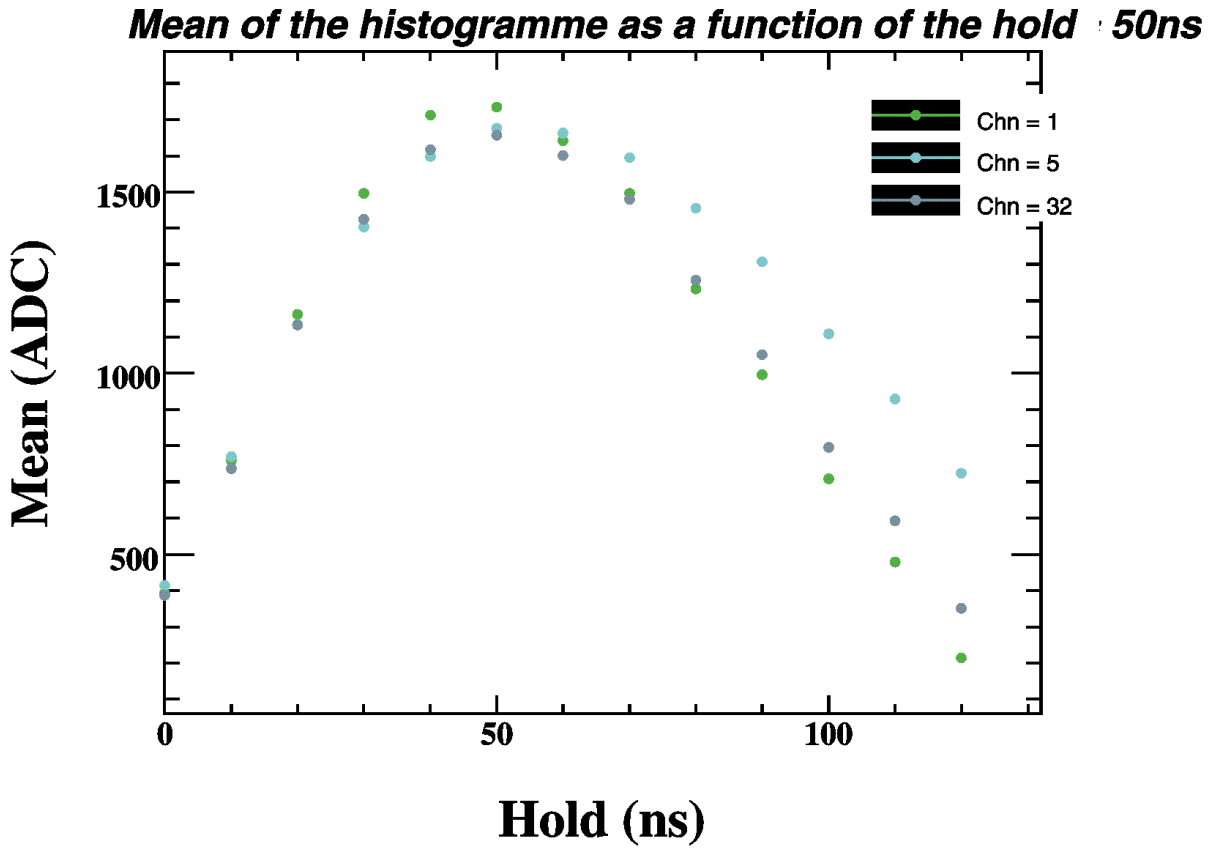



Results by
Jeremy Rouene

# Autotrigger Threshold Adjustment

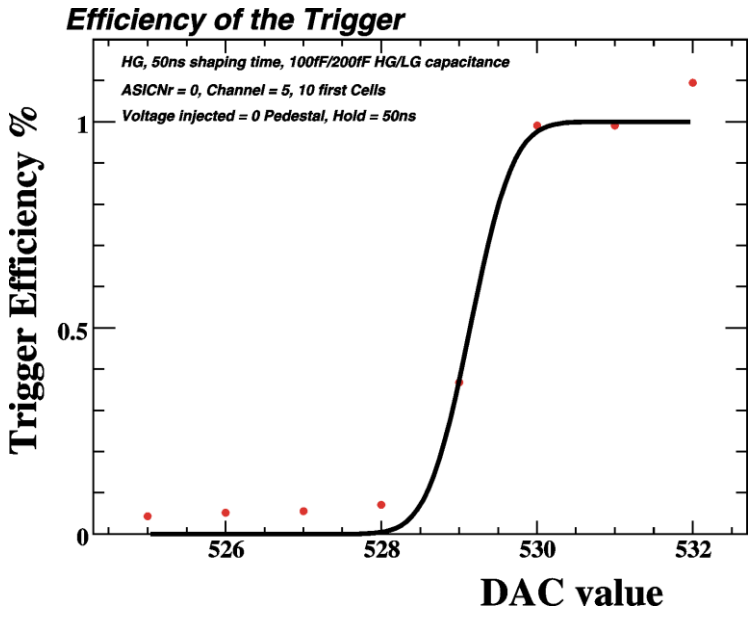
Step 2: Look for the optimum hold-position with autotrigger and check if this is the same for different channels



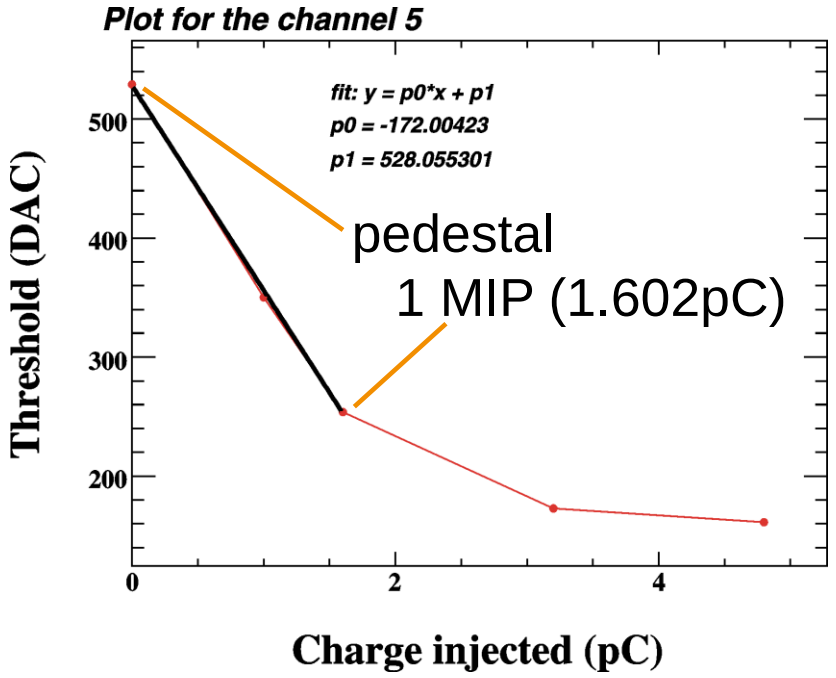

Results by
Jeremy Rouene

# Autotrigger Threshold Adjustment

Step 3: For a fixed input charge, look at which DAC threshold value the SPIROC2 triggers reliably



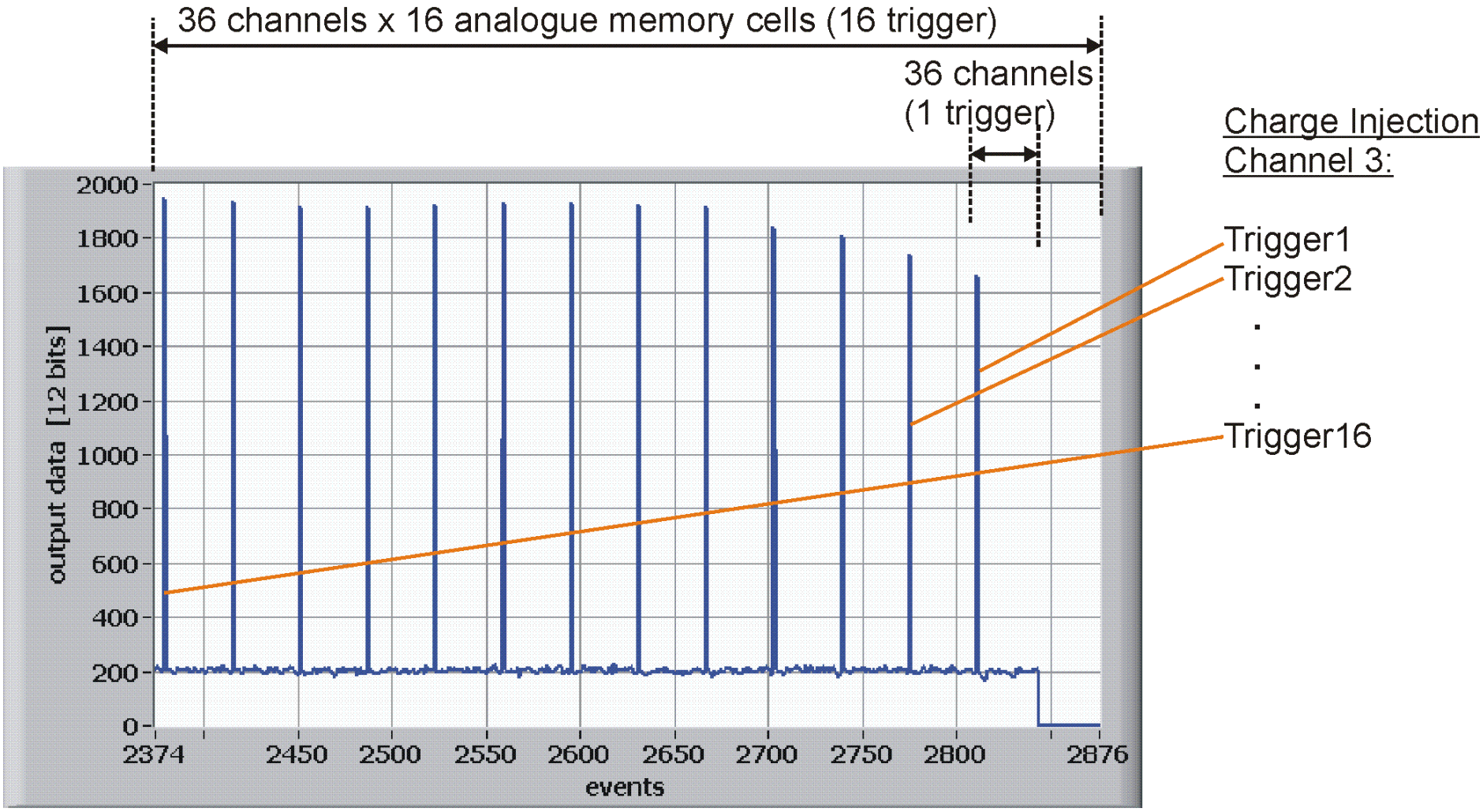

Step 4: Depict the DAC thresholds for different input charges and calculate the slope



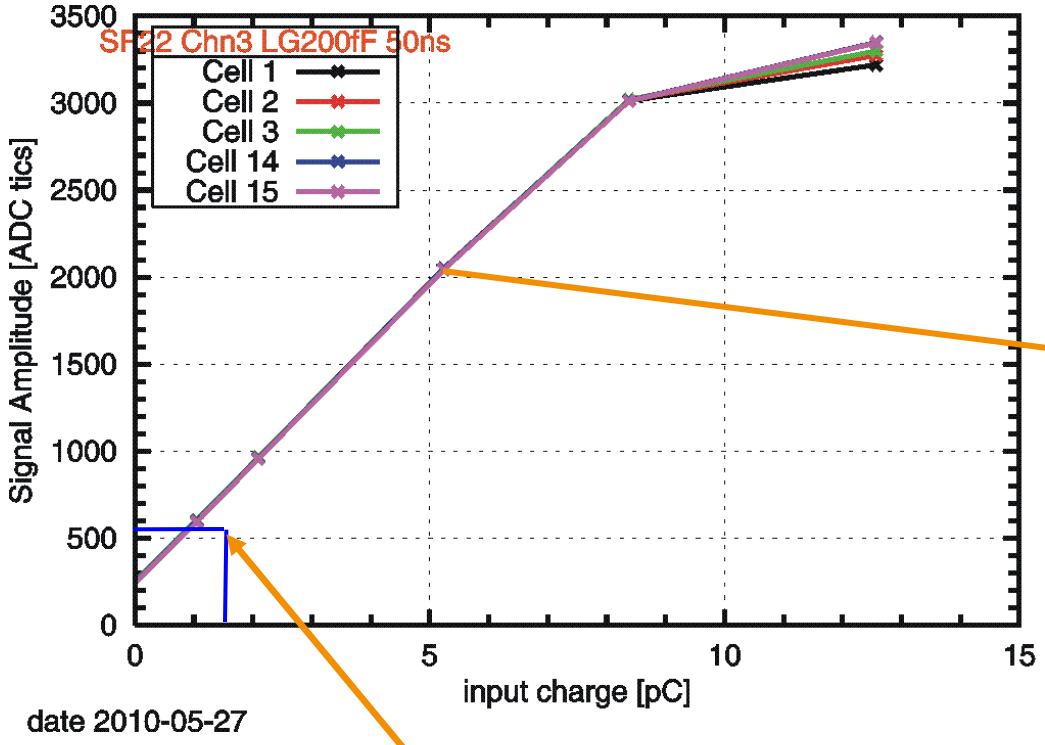

Results by
Jeremy Rouene

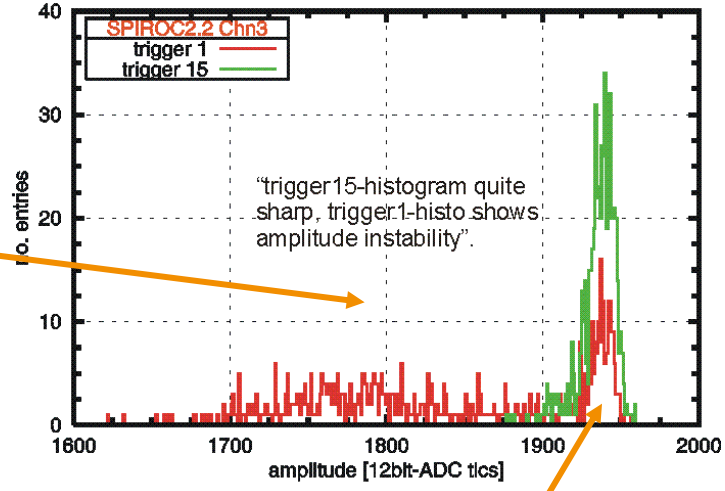
**~172 DACtics / pC**

# Amplitude decreased in first Memory Cells



# SP22 HG dynamic range



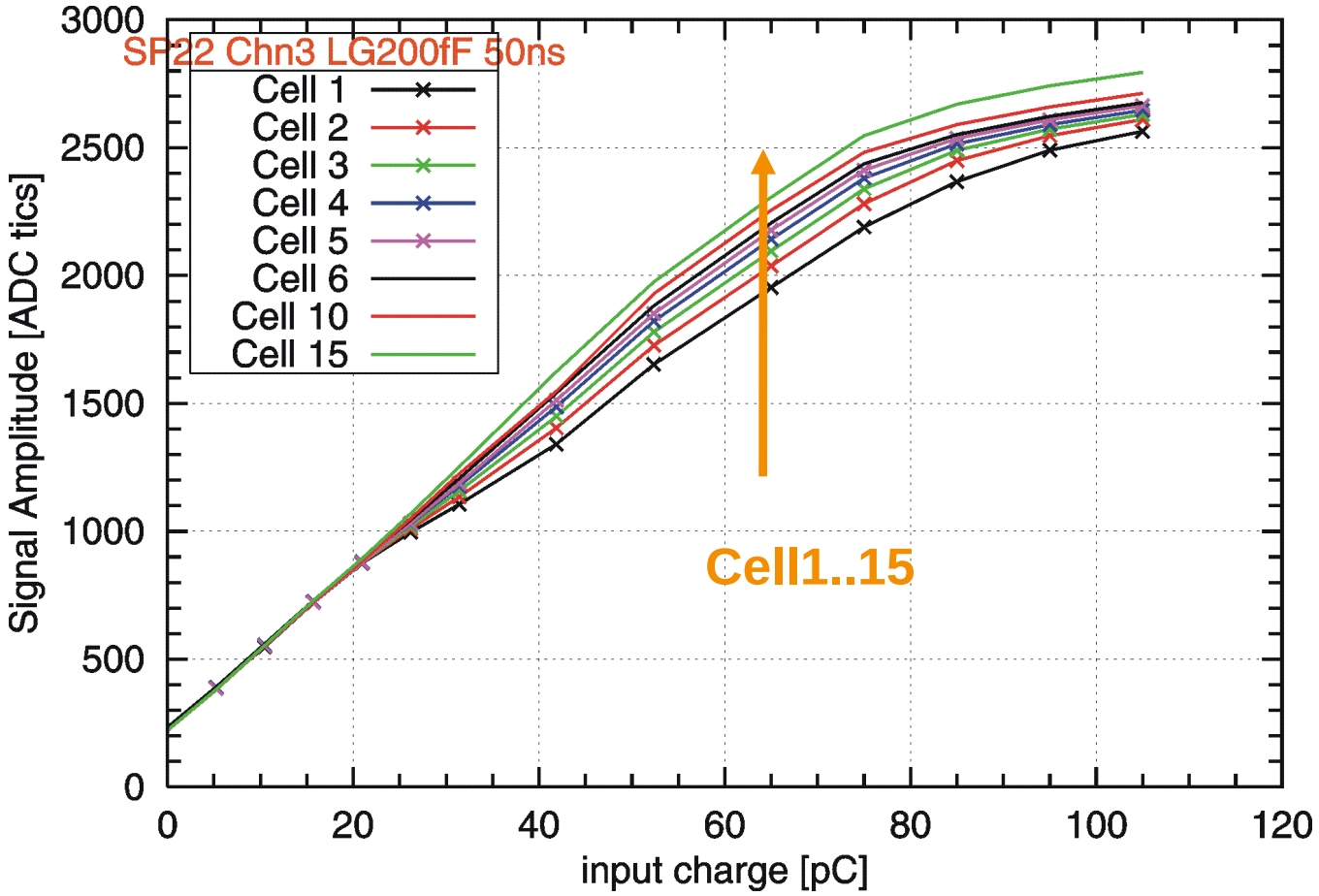




For first triggers: Used right Maximum

MIP should be here!
So a MIP is not 1.6pC (because SiPM gain is not 10^6)

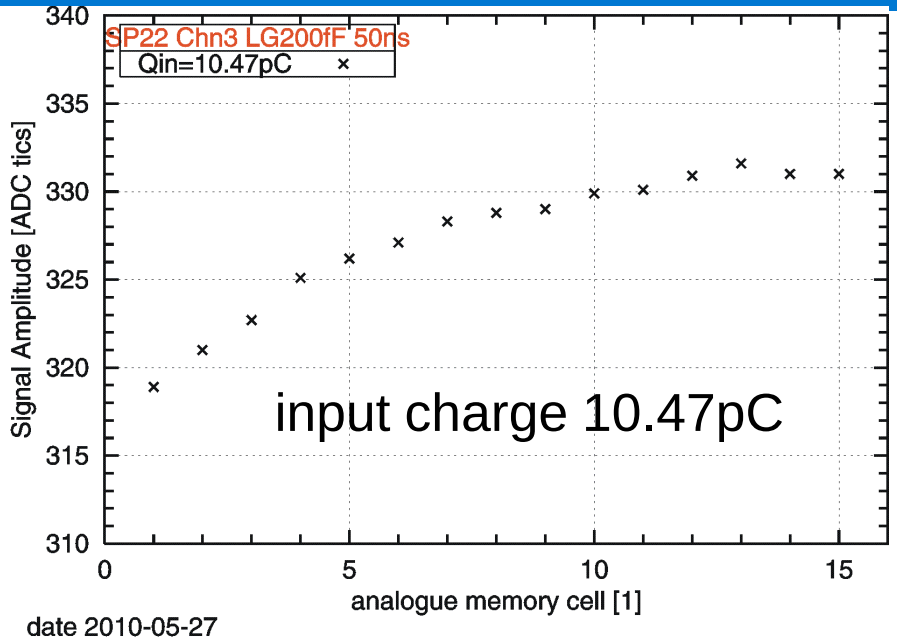
HG PA=100fF
LG PA=200fF
50ns shaping
ext_Hold=140ns

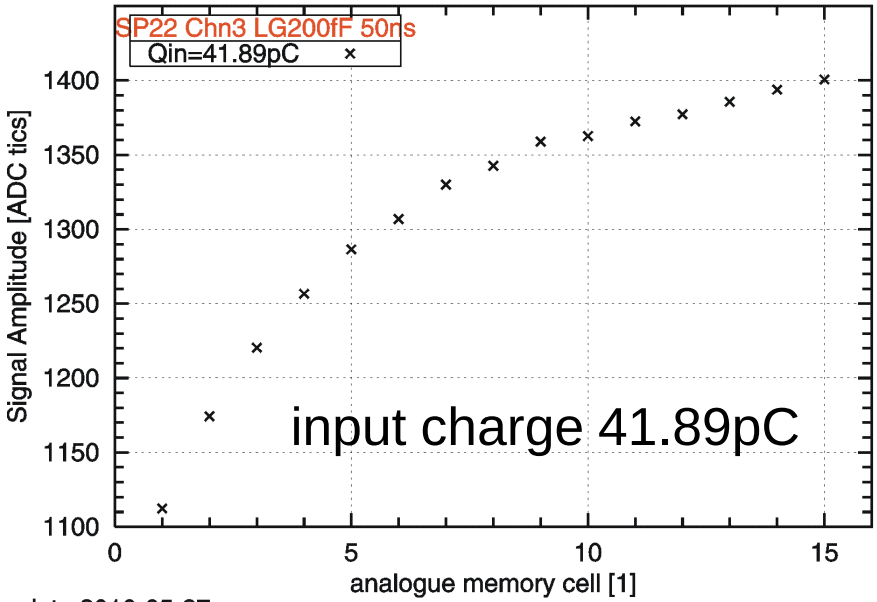
# SP22 LG dynamic range



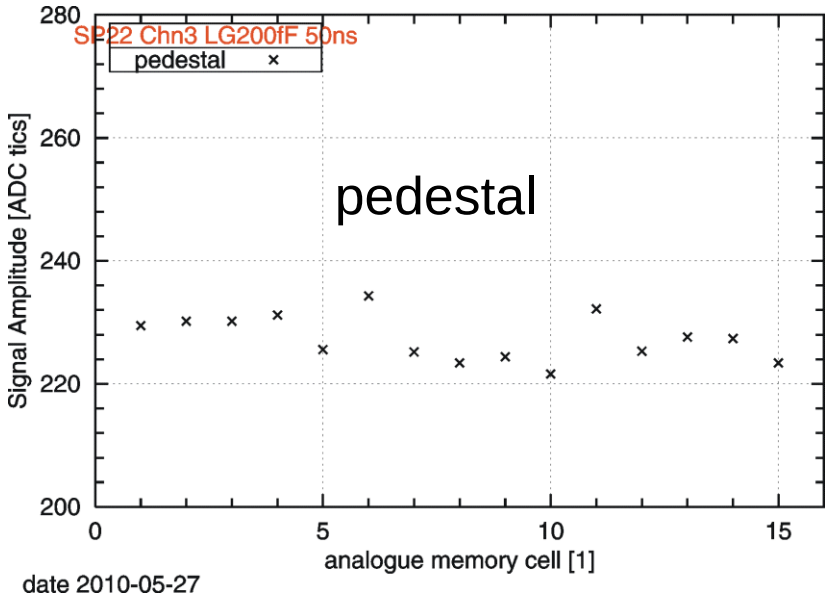

HG PA=100fF
LG PA=200fF
50ns shaping
ext_HOLD=95ns

# Cell Dependence and Stability (SP22, LG)

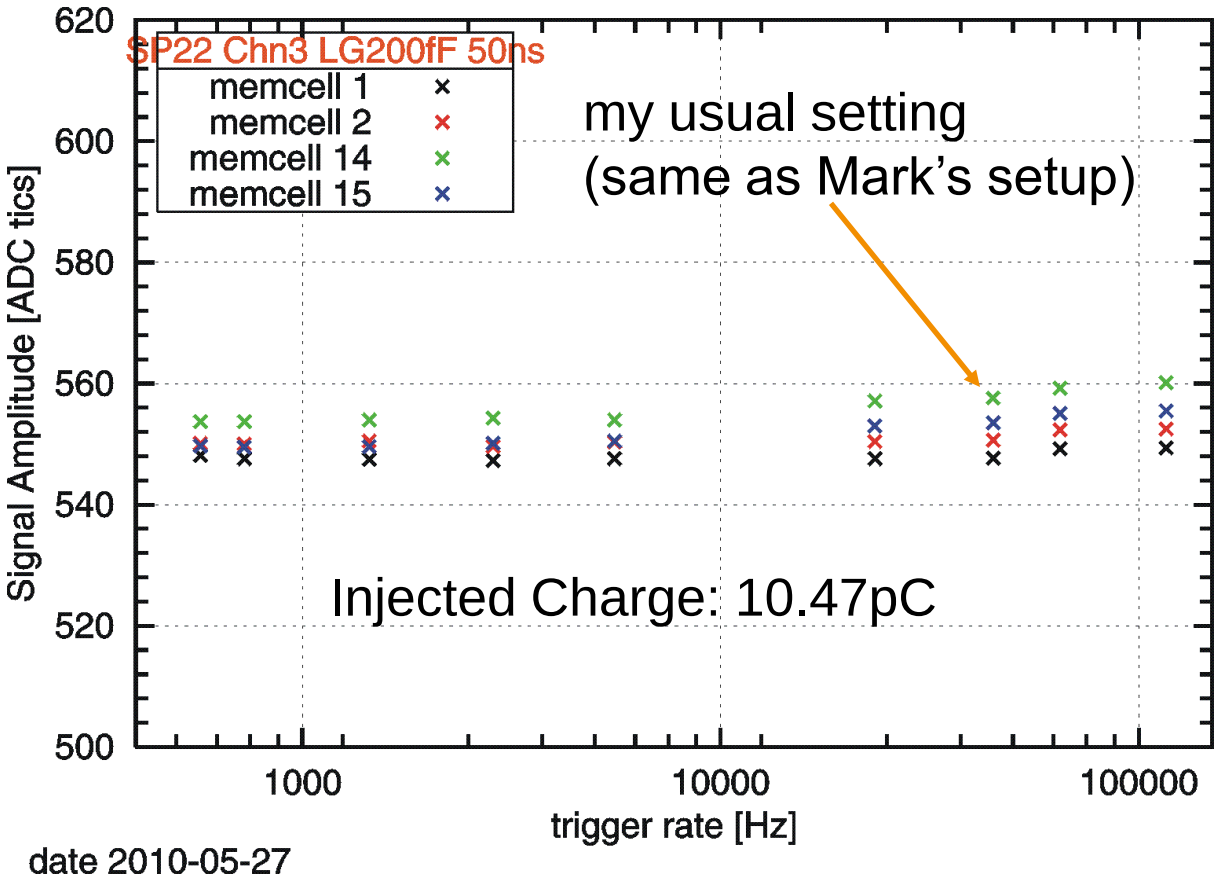



Both plots on left:
**pedestal subtracted**



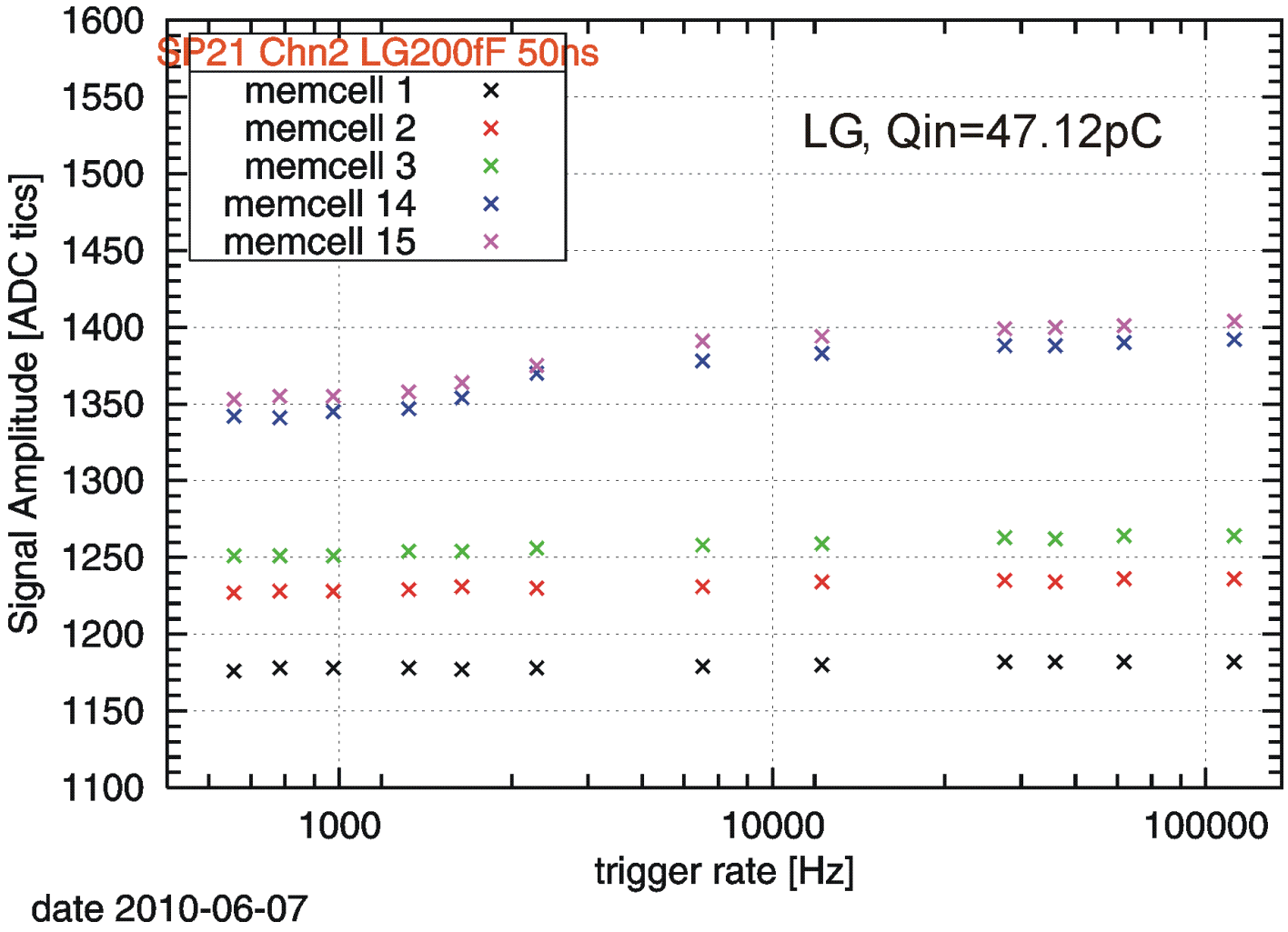
# Rate dependency (SP22, LG, small input charge)




*signal on memcell1 is stored the longest time.*

No signal loss during storage in analogue memory can be observed!

# Rate dependency (SP22, LG, large input charge)



# Conclusions and Outlook

- Effects and their origin need clarification (HBU or SPIROC2 problems).
- Ongoing system tests are important, but delay redesigns as well.
- Consequences of the current effects are not clear until the reasons are not understood.

# Backup Slides

# SPIROC2 HOLD Scans – amplitude dependency