Update on KLauS SiPM readout chip in Heidelberg

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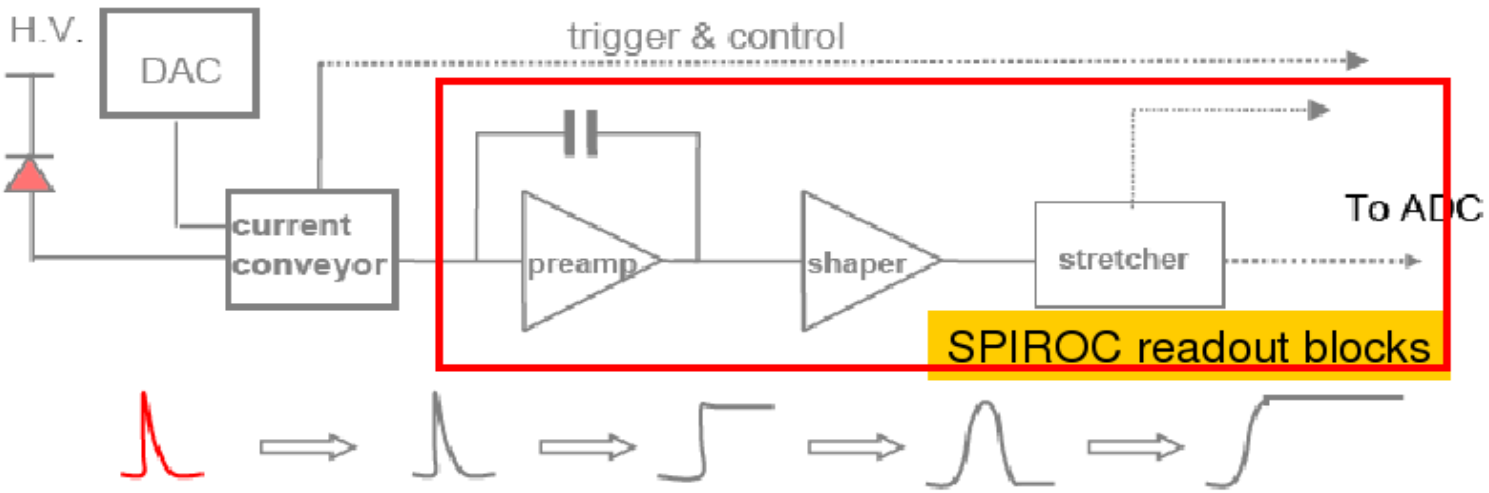
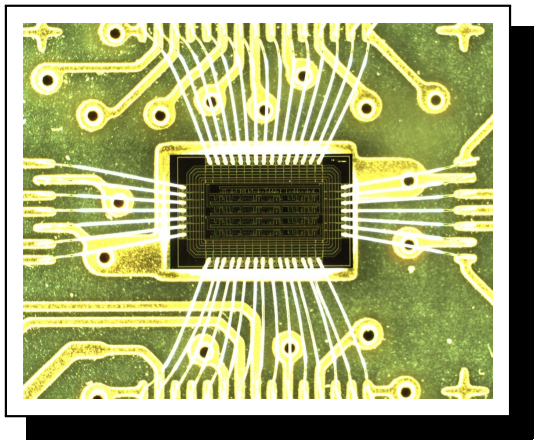
Outline

KLauS in AMS 0.35um CMOS





- submitted in Nov. 09
- designed in AMS 0.35um CMOS
- 4 channels
- analog processing of SiPM signal

S/N and Sgl. Pxl. Spectrum

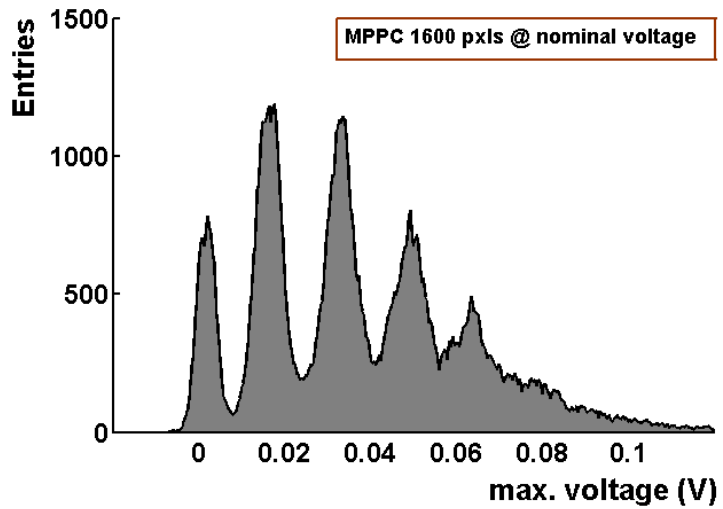
Noise Measurement

- S/N > 10
  2.5×10^5 gain SiPM
  (40fC)

Details:

- low freq. noise observered
- noise increase with larger shaping time
- main noise source from conveyor

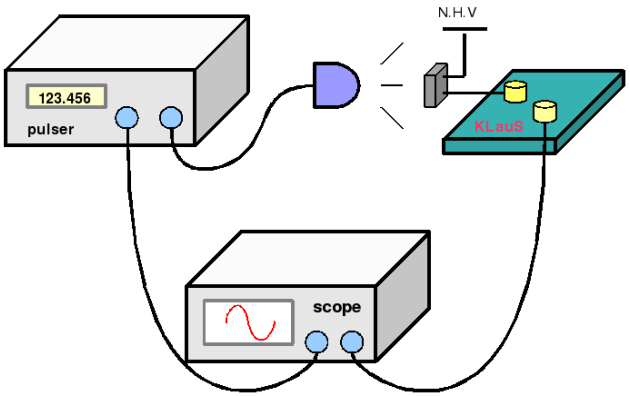
MPPC 1600pxls sgl. pxl. spec.



nominal voltage, gain 2.5×10^5

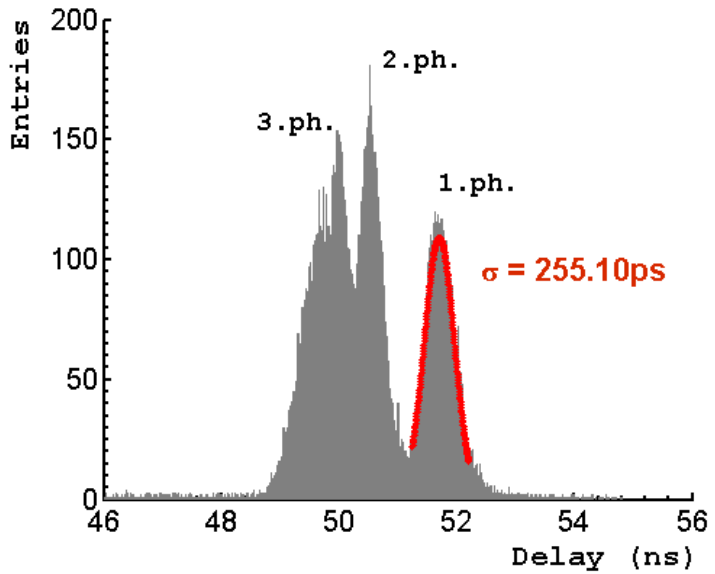
Sgl. Pxl. Timing

LED timing measurement



- KLauS trigger Delay to Pulser Trig.
- Thrd. @ 0.5 pixel
- To cfm. walk and jitter msmt.

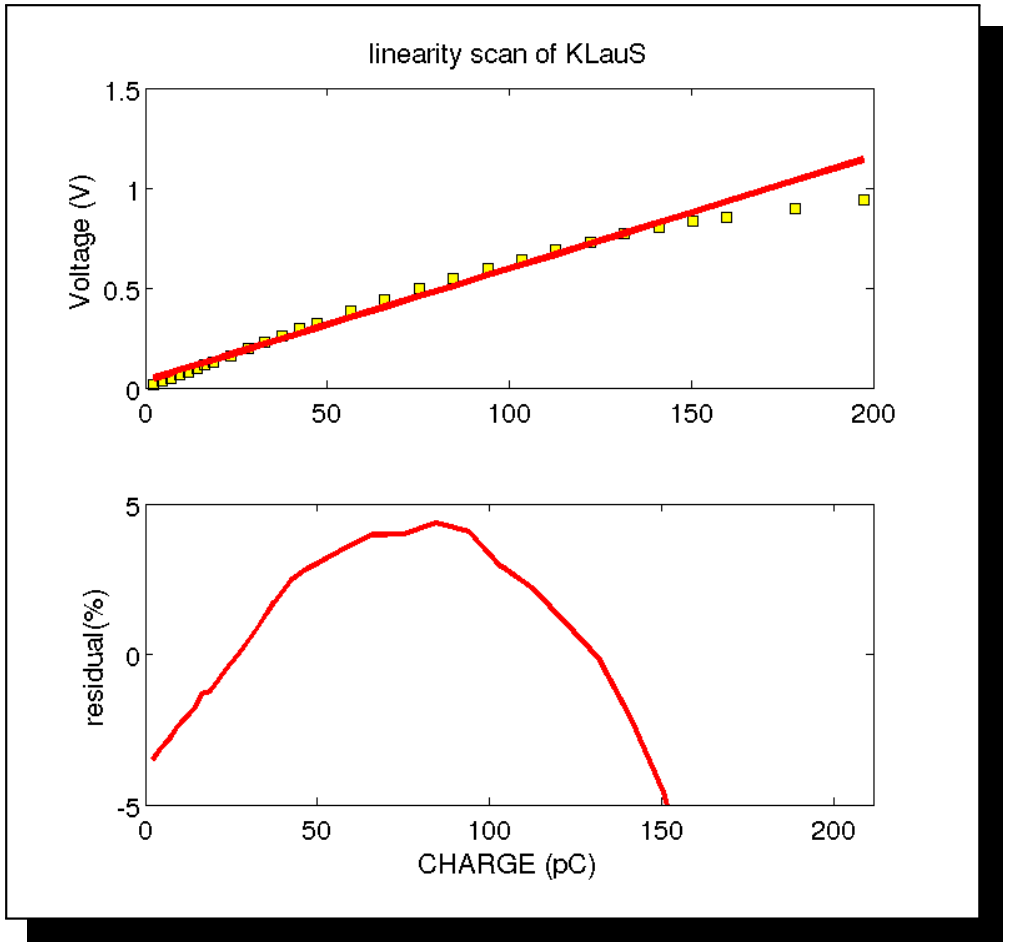
- sgl. pxl. jitter $\sim 260\ ps$
- total walk $\sim 3\ ns$
- $\sqrt{(t_w)^2/6 + \sigma^2}$
- M.I.P $< 200ps$



Words on dynamic range

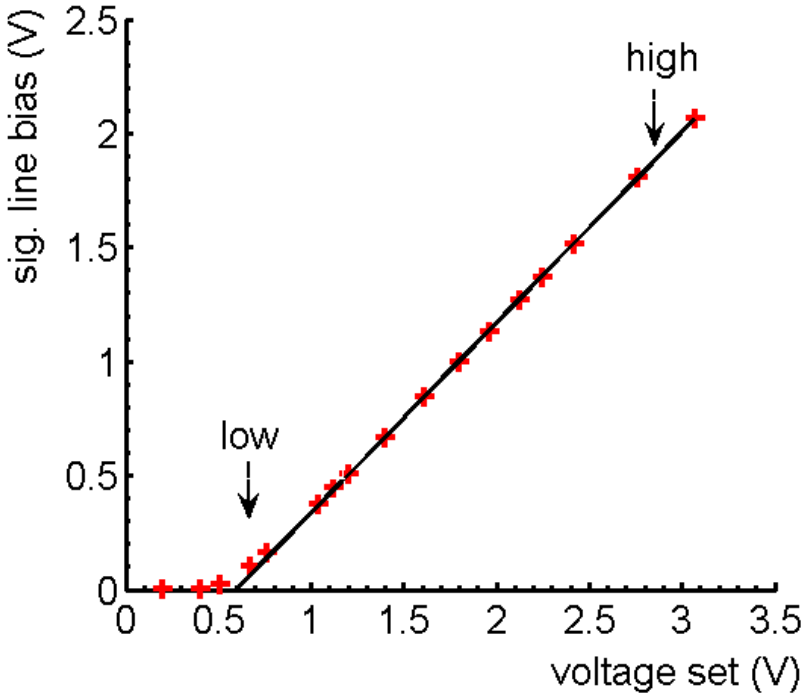
- measure up to 150 pC
- non-linearity $\pm 5\%$

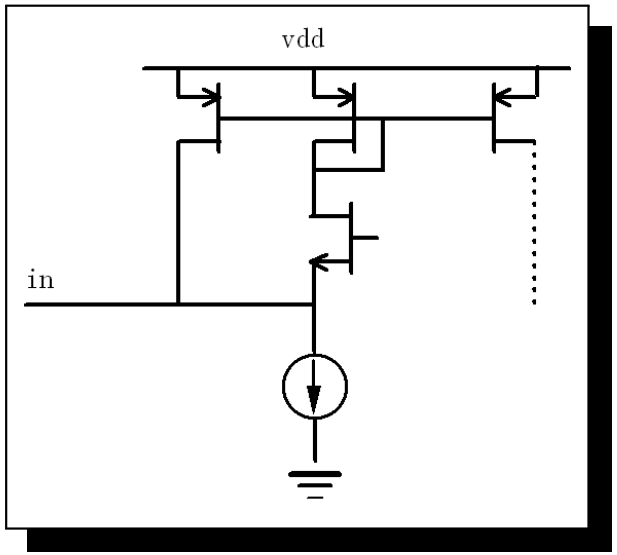
- pulser with 50Ω output impd.
- real $V_{out} = 2\times$ noml. voltage
- chip input $>$ 50Ω in L.F.
- real range $>$ measured noml value



sig. line bias tune

MPPC bias tune voltage.

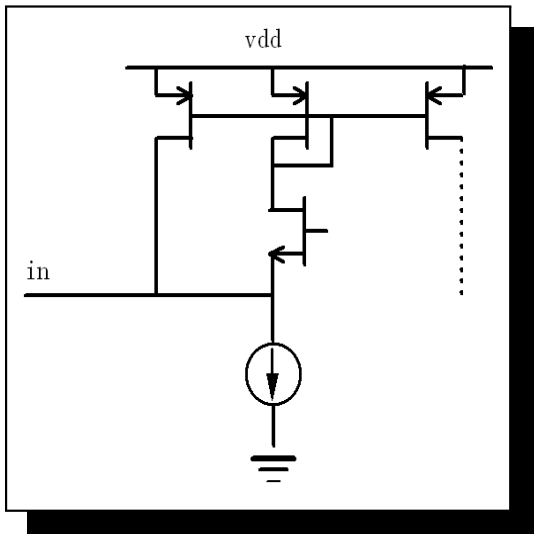


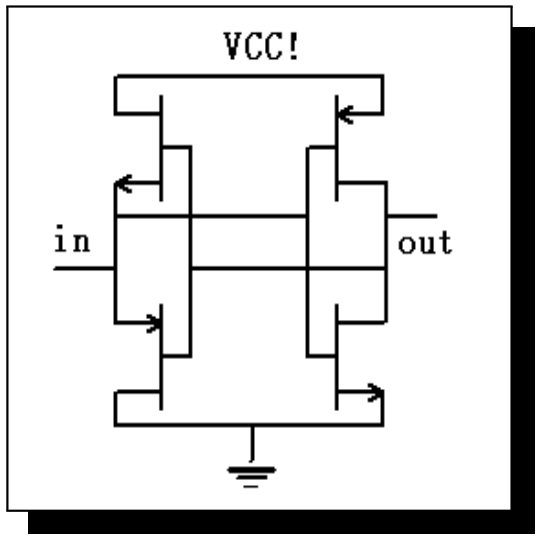


- residual $\leq \pm 1\%$ @ [0.7V 3V]
- $V_{tune} \sim V_{set} - V_{th}$
- output tune range [0.3V 1.9V] > 1.5V

Power and other open issues.

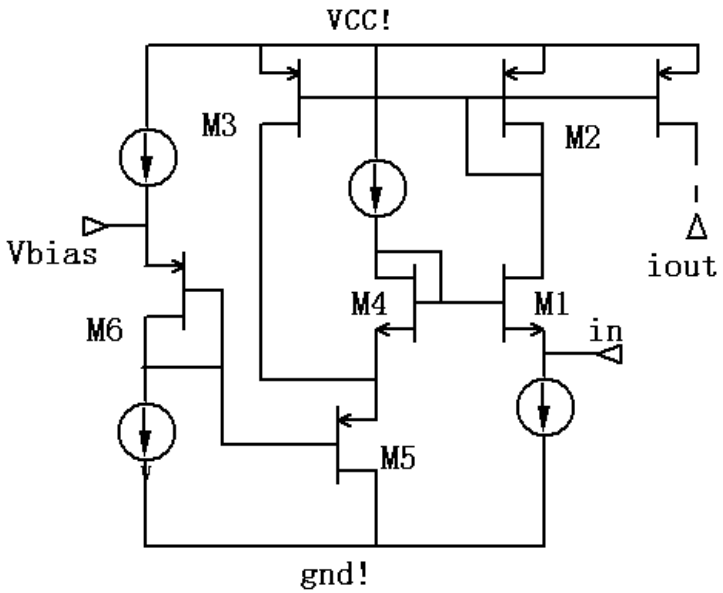
- bias current 500μA , can be reduced
  does not affect dynamic range
- power saved, no preamp (capa. only)
  + powerfree discrimination (current cmp.)
- bias cannot be held, when off
  can be accomplished with translinear loop
  (see new design)





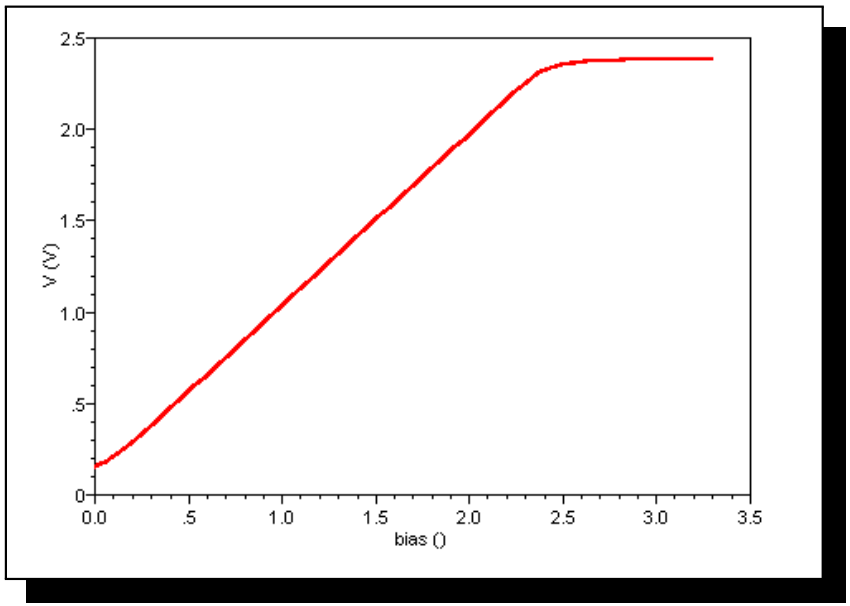
Conveyor with translinear loop

- input impd. $r_x \approx \frac{1}{gm_1} - \frac{gm_3}{gm_2 \times gm_5}$
- current transfer BW doninated by input impd. and mirror pole
- voltage followed by two translinear loops, $M_1 M_4$ and $M_5 M_6$
- bipolar input stage is under investigation
- power pulsing possible , input current scale down to sub-micro Ampre



Power Pulsing with new Conveyor Unit

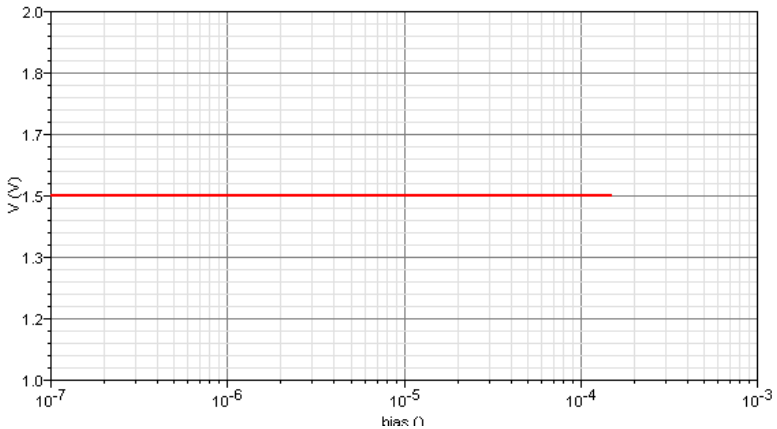
voltage transfer curve



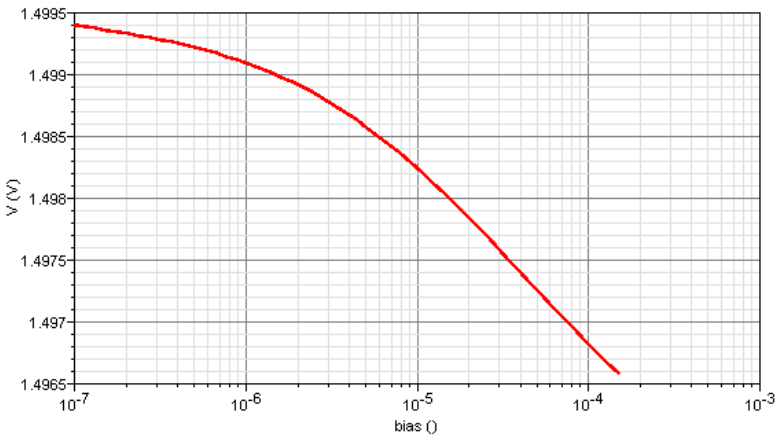
x - voltage set

y - sig. line bias

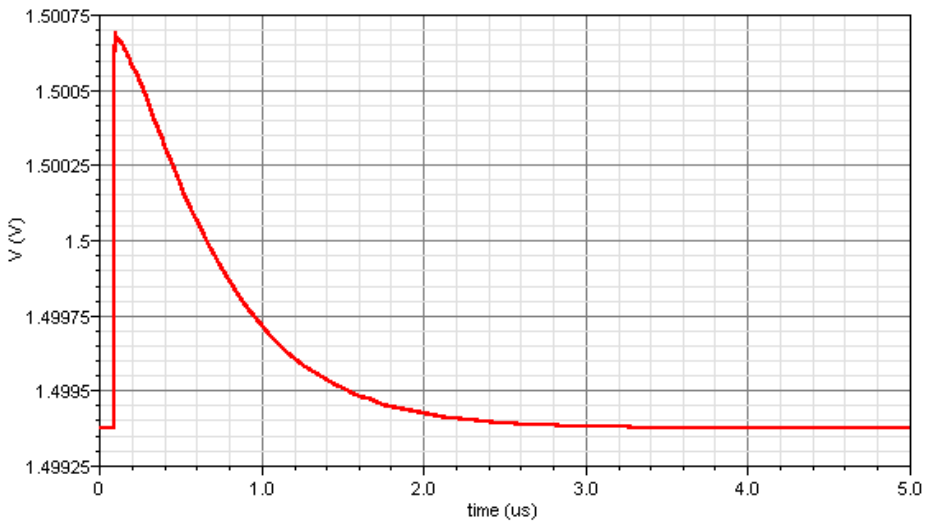
bias current scan



enlarged, 3mV offset

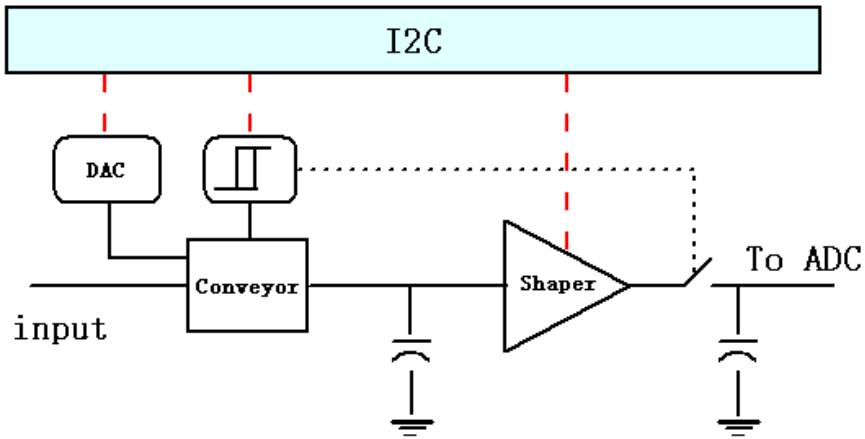


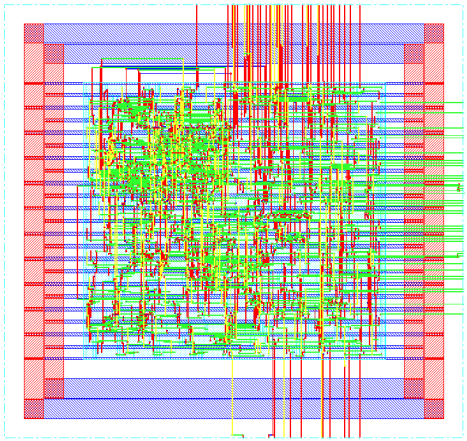
power-off response



- single pixel response , peak vol. 1.3mV, $2\mu s$ width
- pile up pedestal change of 1mV

KLauS 2.0 analog channel upgrade





- new analog part planned this year with more channels
- with I2C inferface
- AMS 0.35um SiGe , benefit from bipolar
- submission in Nov. 02

Summary

KLauS measurements

- KLauS input stage functional
- S/N $>$ 10, Pixel Timing 260ps
- 150 pC range, bias tune $>$ 1.5 V

new submission of KLauS 2.0

- KLauS 2.0 in AMS 0.35μm SiGe , more channels planed
- new full analog processing chain, with less units, low power
- submission in Nov. 02