R&D activity @ LPC Clermont-Fd dedicated to the VFE of the Si-W Ecal

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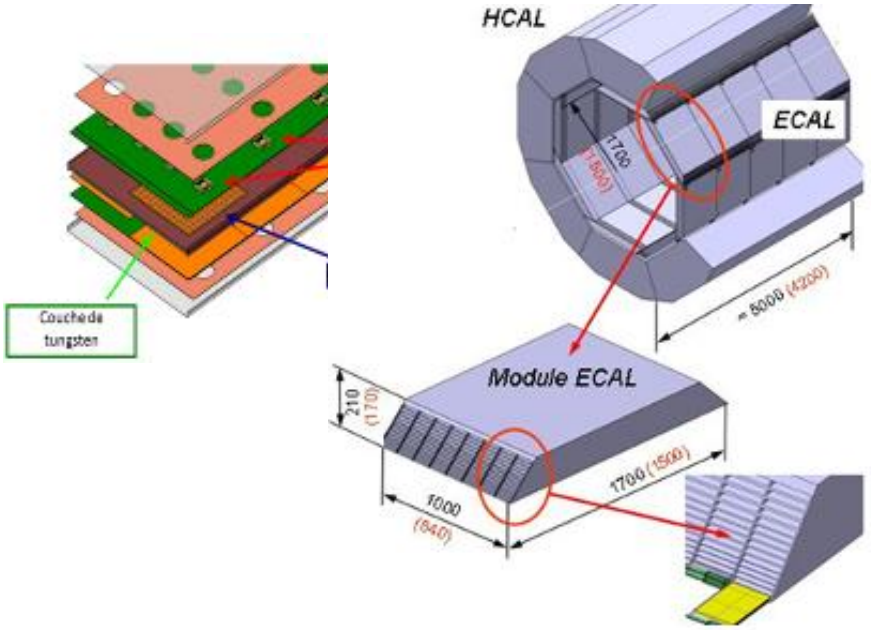
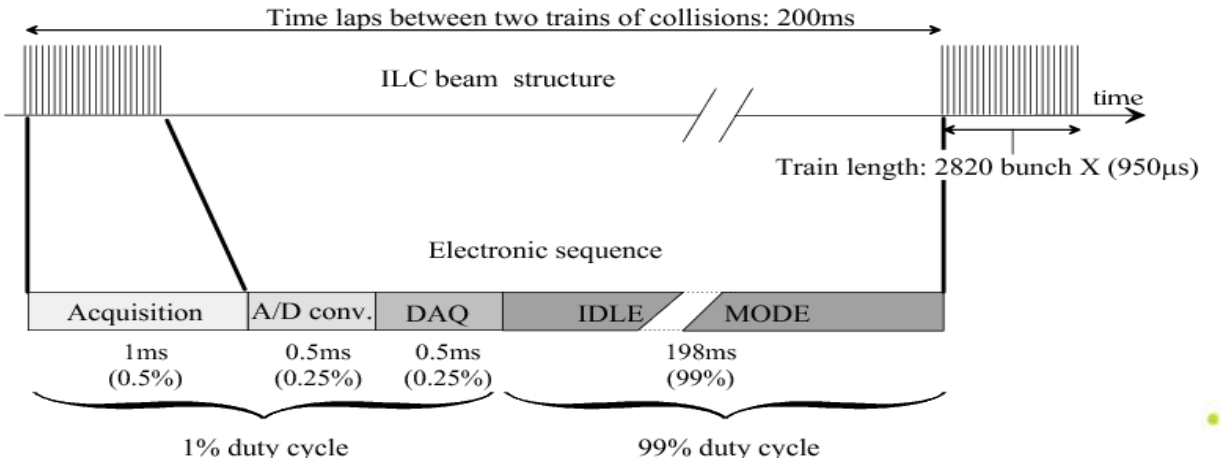
Challenges for next generation of Ecal

- ✓ Sandwich structure of: thin wafers of silicon diodes & tungsten layers
  - ➢ Embedded Very Front End (VFE) electronics
    - ➢ Deeply integrated electronics
- ✓ Large dynamic range of the input signal (15 bits)
  - ✓ **0.1 MIP -> ~3 000 MIPs**
- ✓ Minimal cooling available
  - ➢ Ultra-low power : 25 µW per VFE channel

⇒ power pulsing required

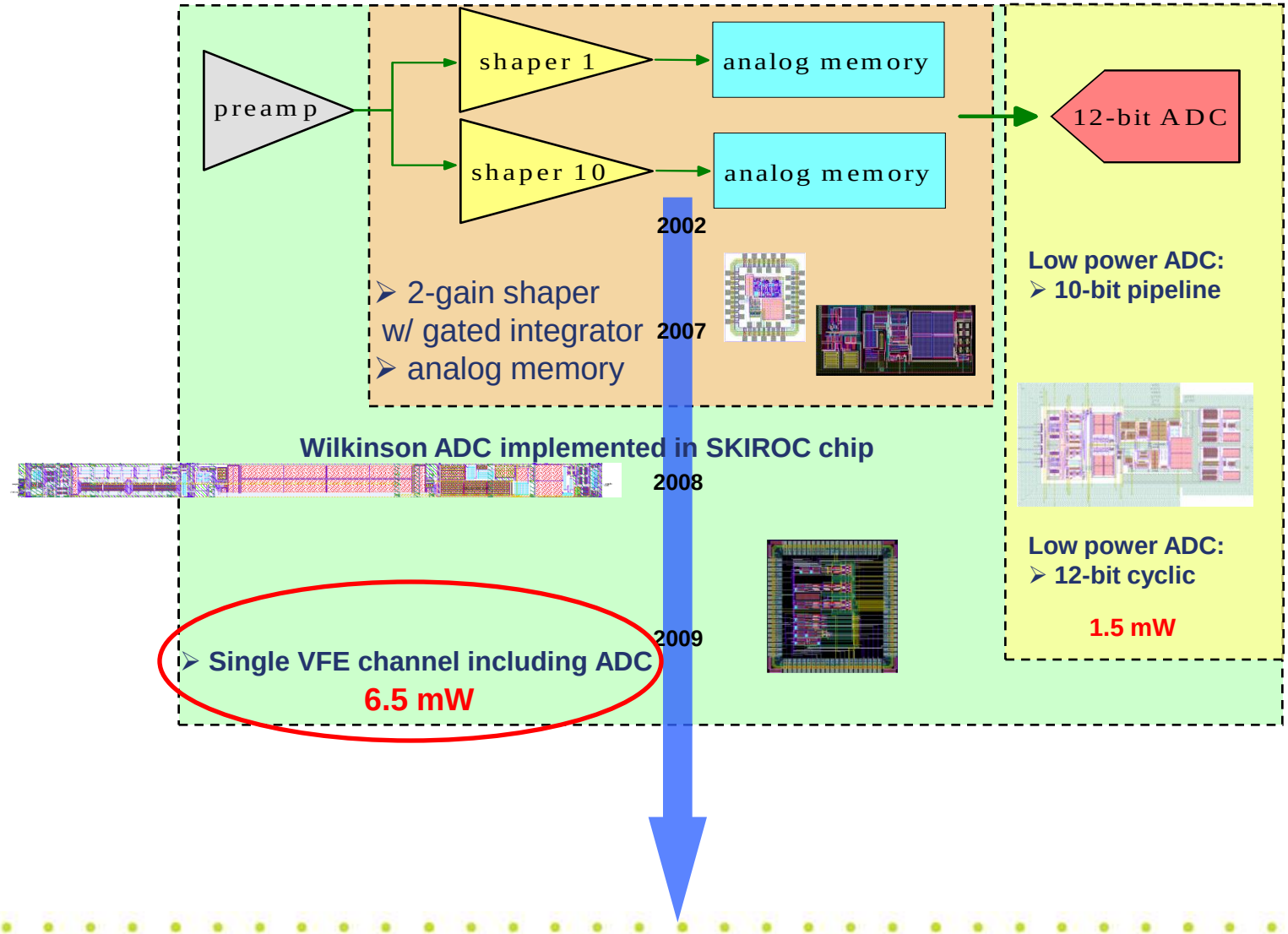


« Tracker electronics with calorimetric performance »

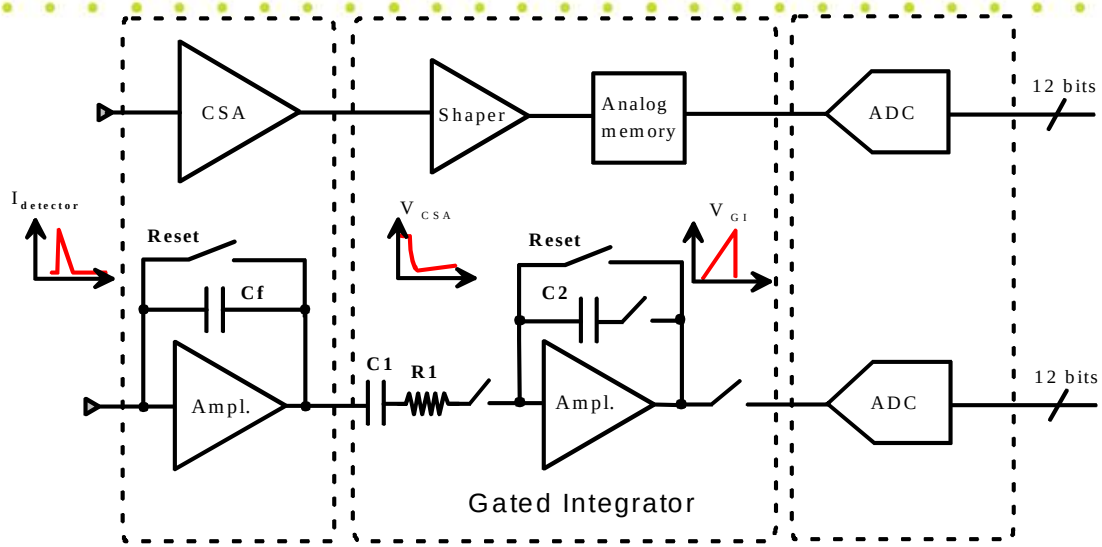


Road map of the R&D activity @ LPC Clt-Fd

"Long is the road …"



Architecture of the VFE designed



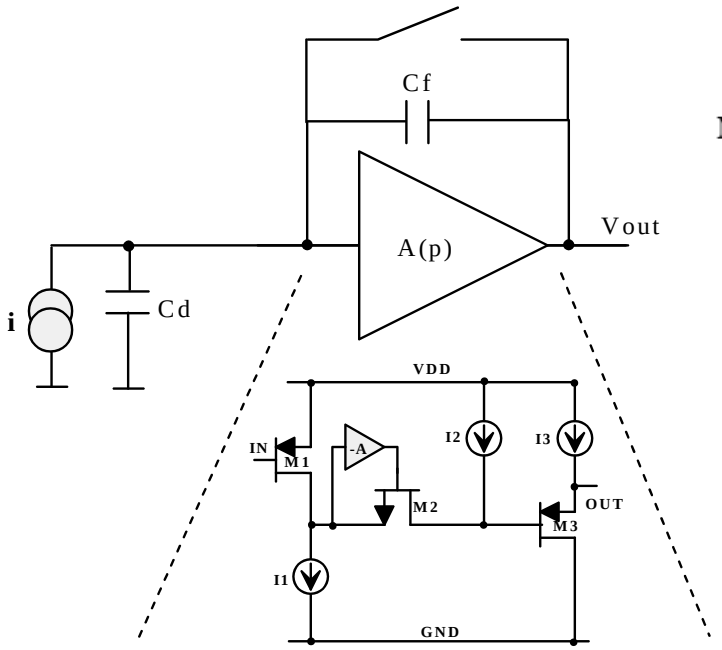
- ✓ **Charge Preamplifier**
  - The amplification of the charge delivered by the detector is performed with a low-noise Charge Sensitive Amplifier (CSA)
- ✓ **Shaper and Analog Memory**
  - The bandpass filter is based on a gated integrator which includes an intrinsic analog memory thanks to the integration capacitor
- ✓ **Analog to Digital Converter**
  - The converter is a customized low power 12-bit cyclic ADC
- ✓ **External digital block (in a FPGA)**

The charge preamplifier

- The amplifier is based on a boosted folded cascode, followed by a source follower
  - **Boosted Cascode : High gain performance**
  - **Source follower : Low output impedance**

$$V_{out} \approx -Q/C_f$$

Q, the charge delivered by the detector.
***Cf,* the feedback capacitor.**

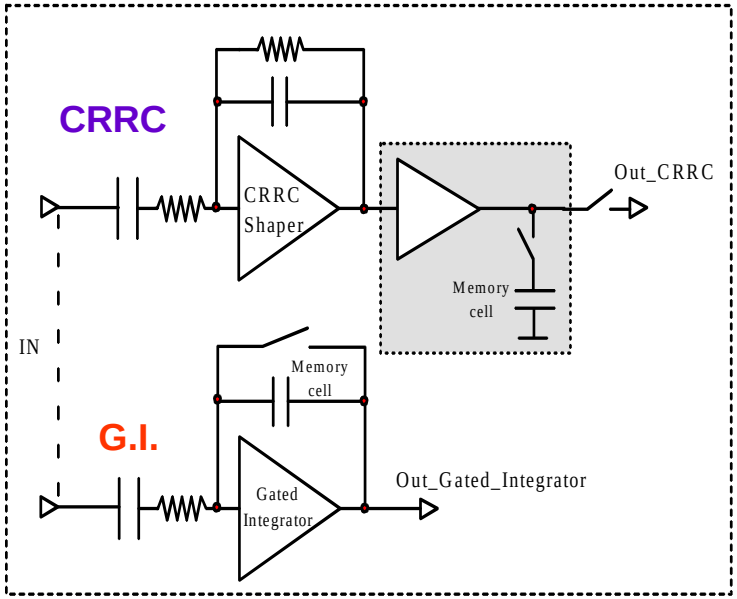


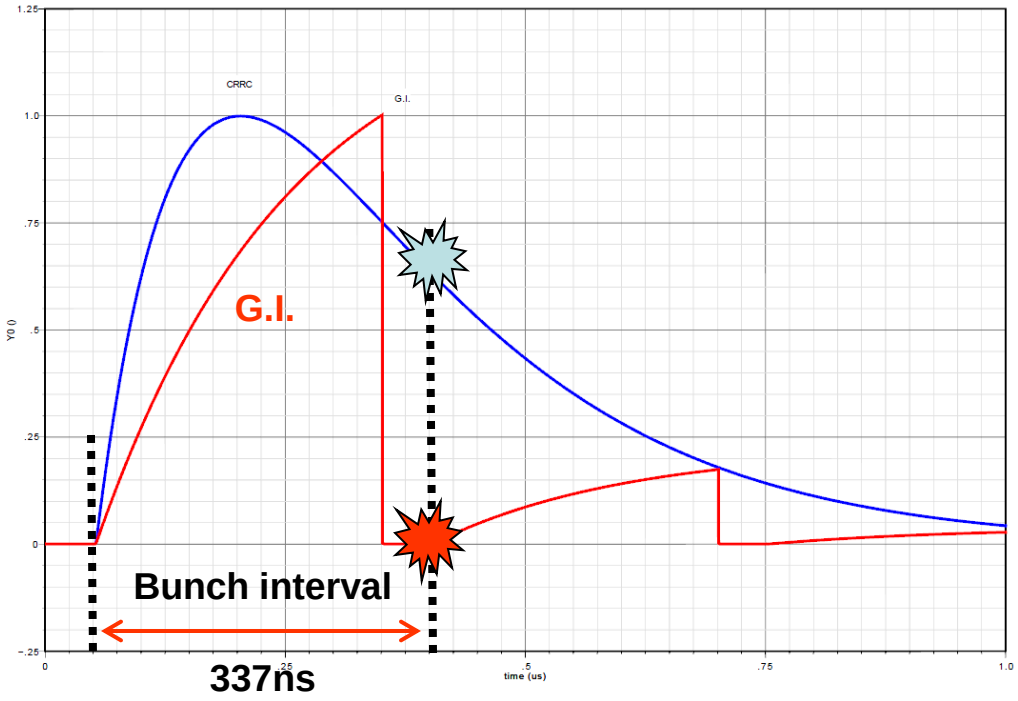
MAIN CHARACTERISTICS OF THE CSA (SIMULATED RESULTS).

Power supply	3.3 V
Consumption	3.54 mW
$C_{Detector}$	30 pF
$C_{Feedback}$	
Transconducta	
Open Loop Gain G_{OL}	83 dB
Gain-Band Width	105 MHz
Output swing	1.0 V
ENC (with a 200 ns CCRC shaper)	0.5 fC
Dynamic range	80 dB

50% for masters of the current sources
→ can be shared by several channels

CRRC Shaper vs Gated Integrator (GI)





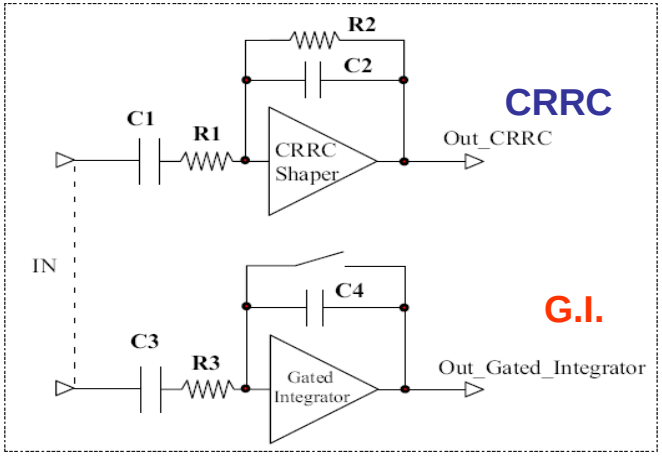
- **The integration capacitor of the G.I. can be used as an analog memory cell (switch opened at the end of the integration)**
  - no extra analog-memory stage required
- **The fast switched reset of the capacitor of the G.I. allows a time of integration near to the bunch interval**
  - no pile up
  - improved noise filtering (see next slides)

Comparative noise filtering performances of Gated Integrator and CRRC filtering

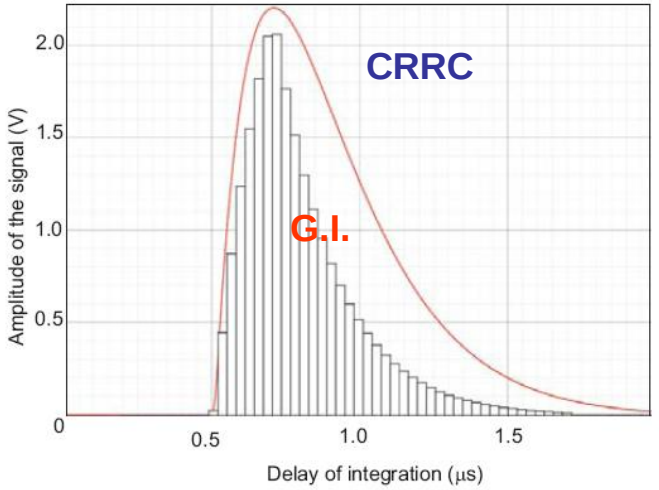
- CRRC shaper is time invariant filter
- Gated integrator is time variant filter

  - **To compare performances, weighting functions R(t) in time domain MUST BE USED**

- *The weighting function is the measurement of influence of a noise step generated before the measuring time on the amplitude at the measuring time*

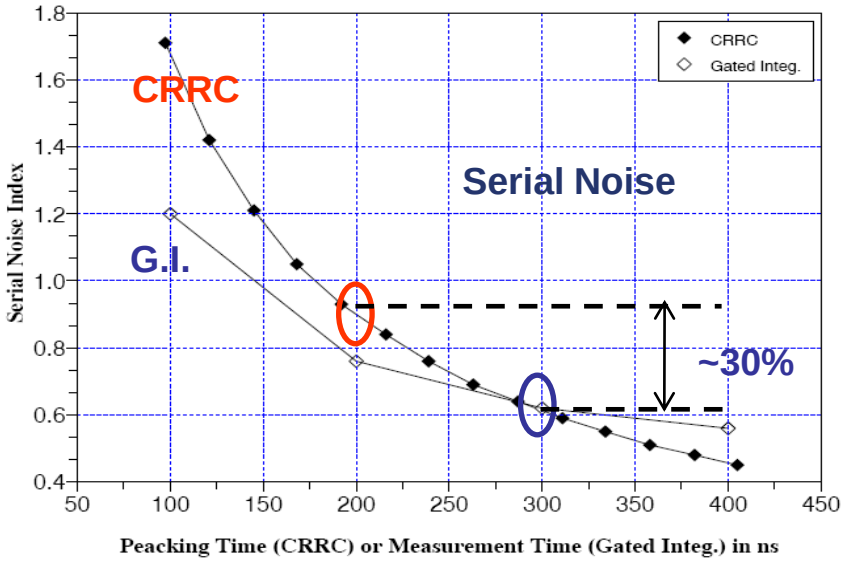


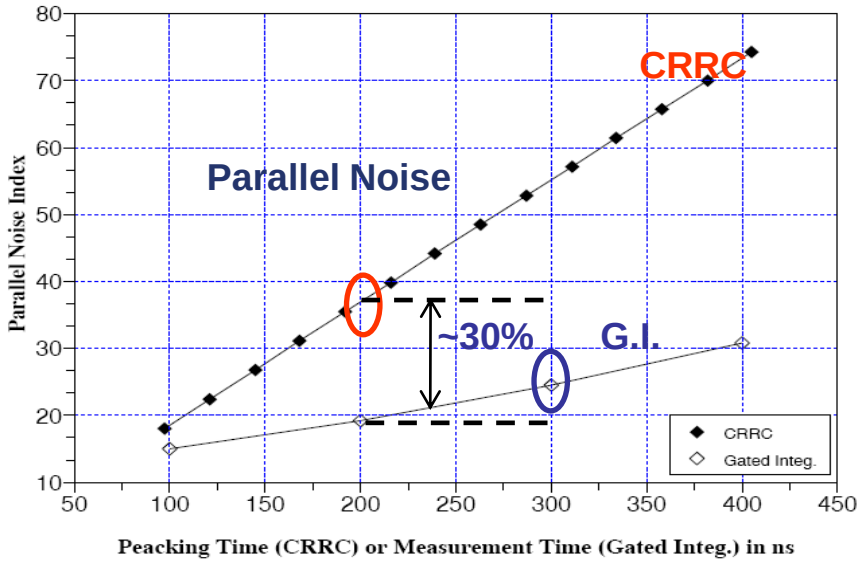
Obtained with simulation software



Comparative performances of Gated Integrator and CRRC filtering

- **Noise indices have been simulated with Analog Artist (Cadence) Software for several peaking times (CRRC) and durations of integration (G.I.)**



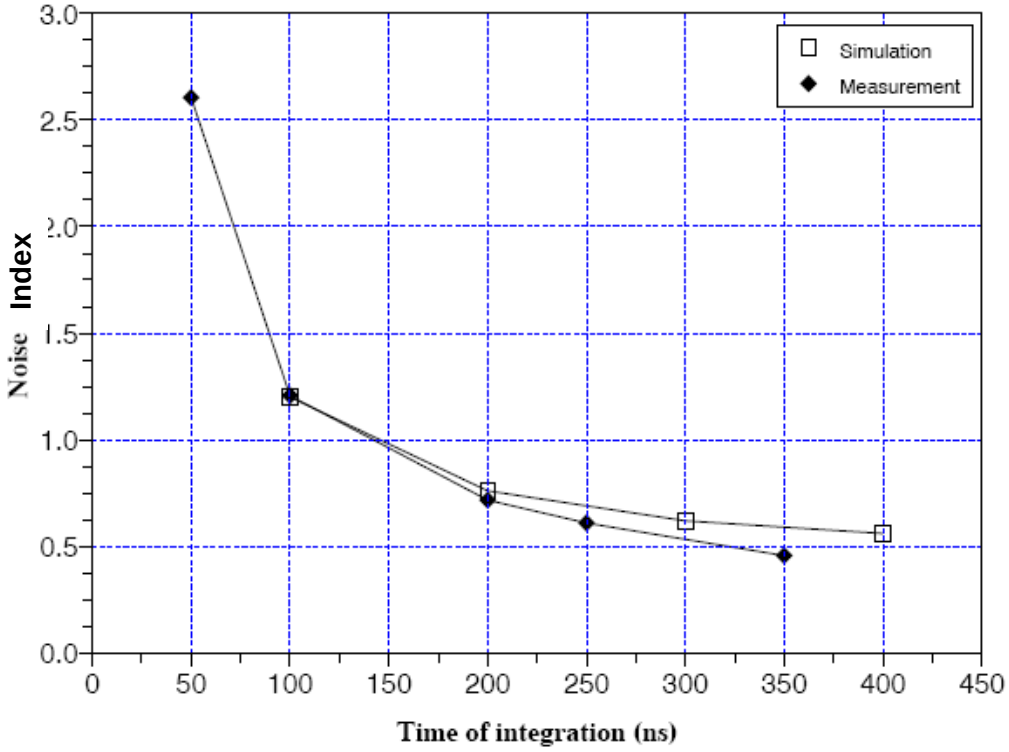


- **The peaking time of the CRRC shaper is limited due to pile-up consideration**
  - → 200ns with a bunch crossing of 337ns (ILC).
- **For the Gated Integrator, fast reset of integration capacitor allows duration of integration near to the bunch crossing interval**
  - → 300ns with bunch crossing of 337ns

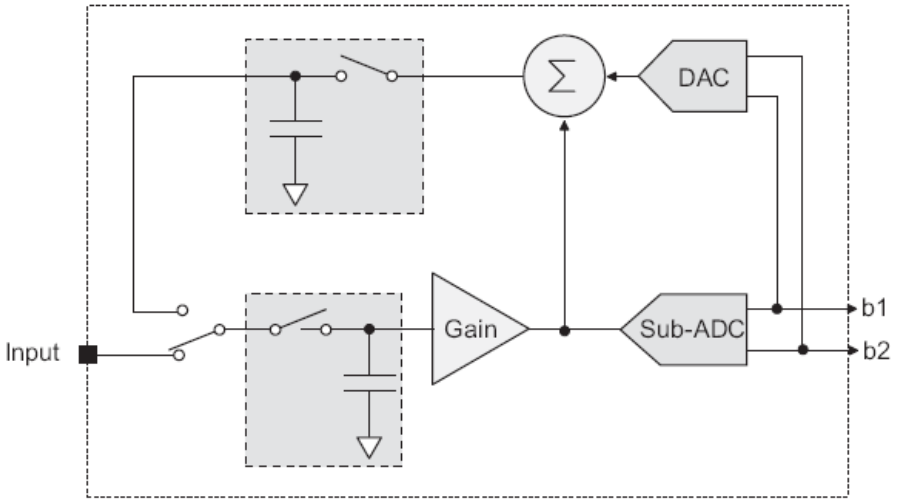
→ both serial and parallel noise indexes can be reduced by about 30% with the G.I. filtering.

Variation of the noise Simulation/ Measurements

- Variation of the noise versus the time of integration of the G.I. obtained by simulation (serial index) and by measurement
  - **Dominated by serial noise.**



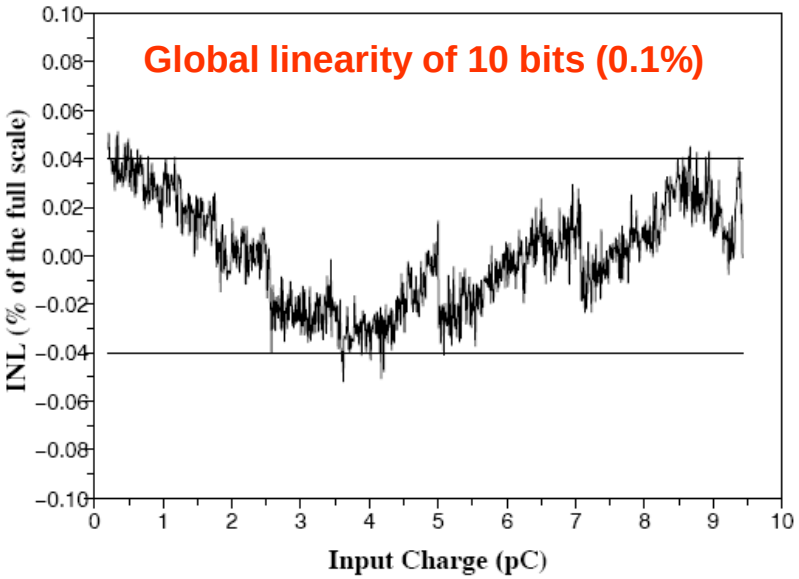
Architecture of the 12 bits cyclic ADC

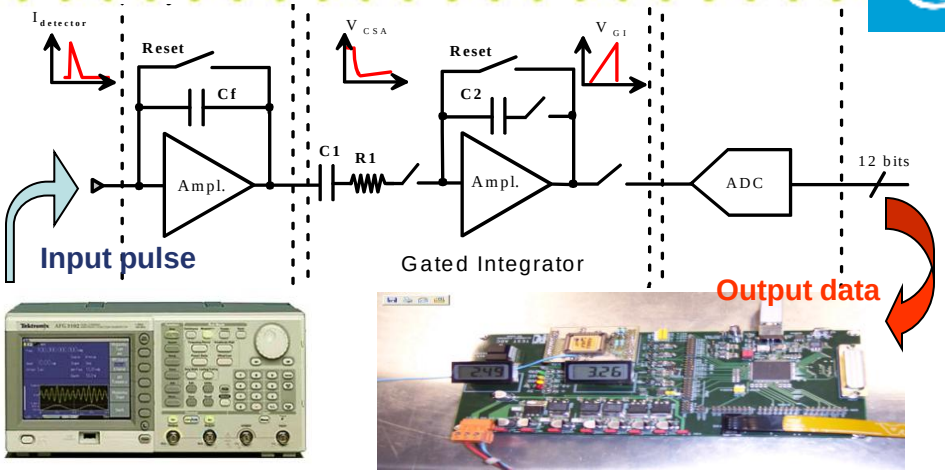


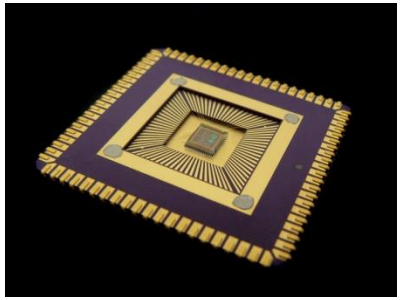
Architecture	1.5-bit/stage
Area	0.12 mm^2
Supply Voltage	3.0 V
Resolution	12 bits
Dynamique range	2.0 V differential
Time of conversion	6.8 μs
Consumption	1.5 mW
INL	3 LSB
RMS Noise	0.3 LSB

- The cyclic architecture is well adapted to **compact-low-power** converter.
  - 1.5 bit per stage architecture
  - Clock frequency: 1MHz
- Presented IEEE NSS 2008 Dresden
  - "A custom 12-bit cyclic ADC for the electromagnetic calorimeter of the International Linear Collider"

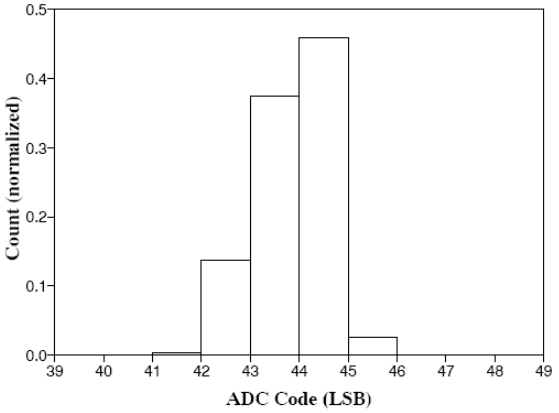
Results of measurements of the VFE (1)







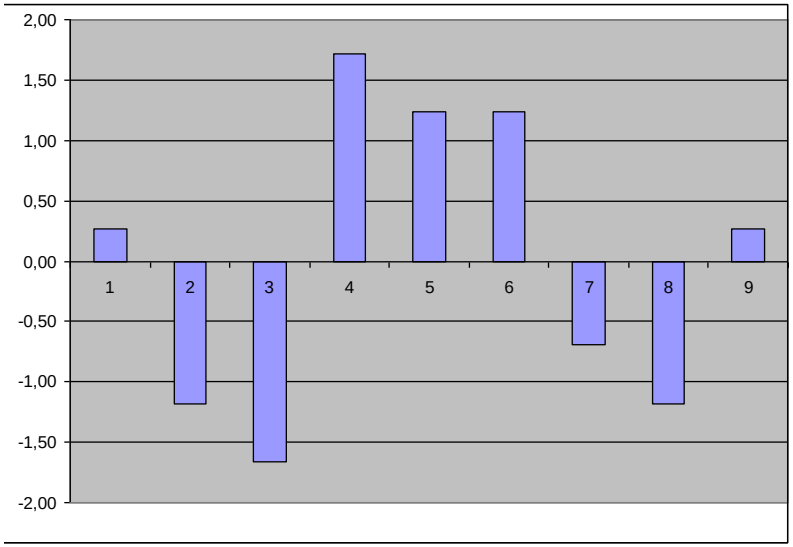
The standard deviation of the noise at the output of the channel is **0.76 LSB (370 µV rms).**
The Equivalent Noise Charge **(ENC) at the input of the channel is then lower to 2 fC.**

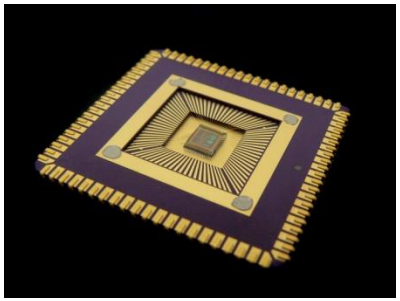


The power consumption of the channel is 6.5mW, estimated to 25µW with duty cycle of each block.

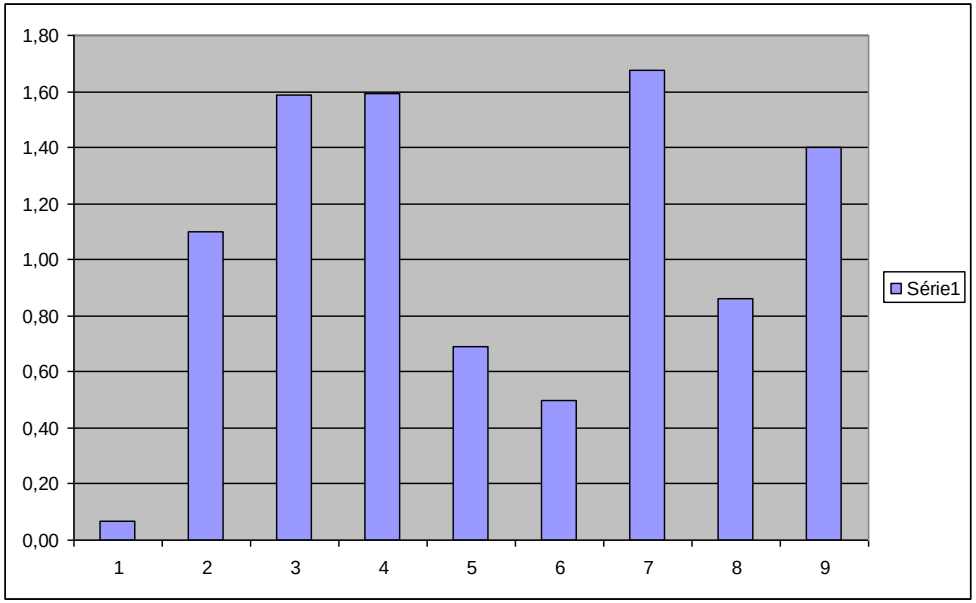
Results of measurements of the VFE (2)

Dispersion of the gain of the 9 chips (in %)



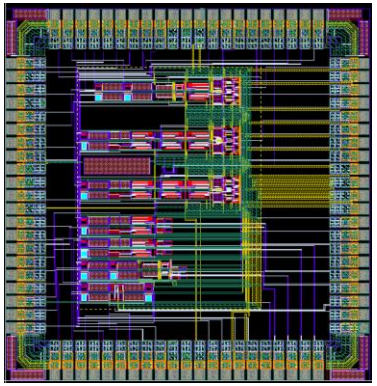


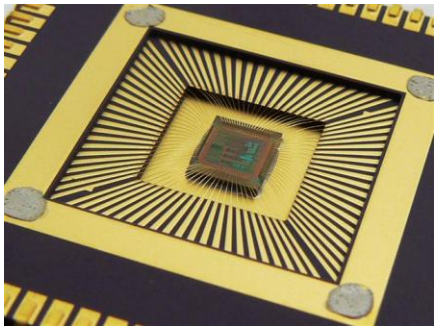
Dispersion of the offset of the 9 chips (in mV)



Summary

- A VFE channel performing the amplification, the filtering, the memorization and the digitalization of the charge from Si detector has been designed and tested.
  - **Global Linearity better than 0.1 % (10 bits) up to 9.5 pC (2375 MIP).**
  - **ENC = 1.8 fC (0.5 MIP)** with a single gain stage
  - **Power consumption with power pulsing estimated to 25µW (no digital part).**



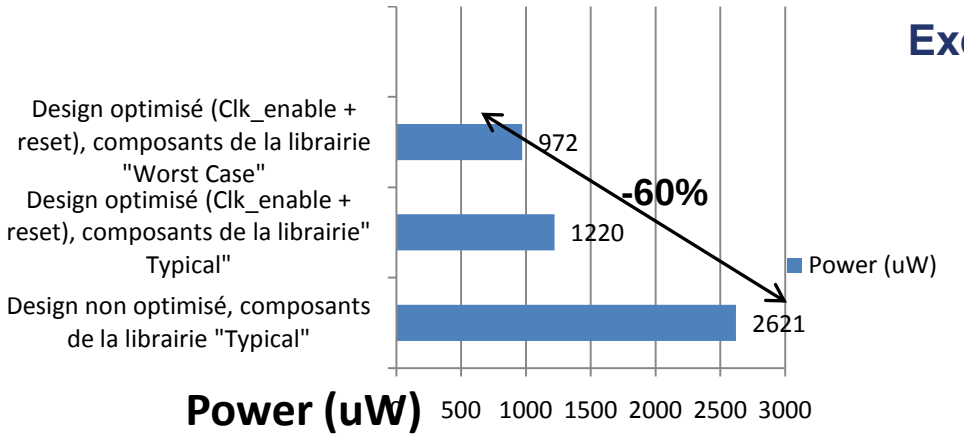


Perspectives

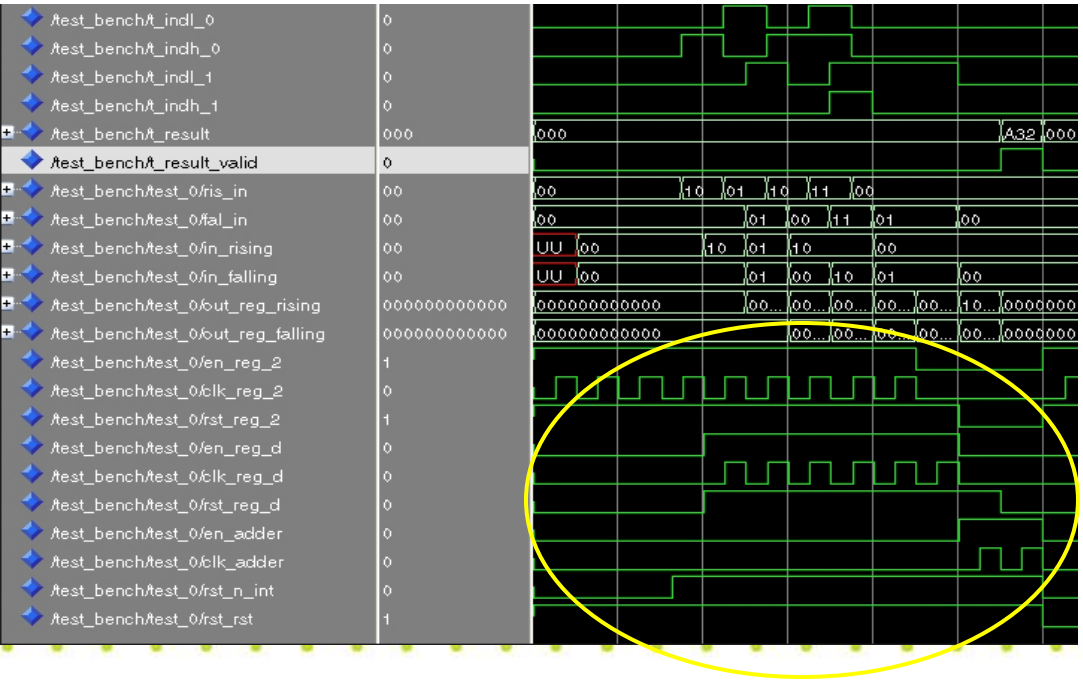
- **Next steps**
  - **Improvement of the dynamic range up to 15 bits**
    - **Reduction of the output noise of the amplifier of the Gated Integrator**
    - **Integration of a multi-gain system on the CSA**
    - **Use of a multi gain shaping**
  - **Integration of the digital block, of the bandgap (ADC references), of the power pulsing, …**
  - **Test-bench for the VFE channel**
    - **realistic environment : wafer/ASU + VFE + (DIF)/DAQ**
    - **versatile and upgradable**
    - **connected to wafer test-bench already in LPC-Clfd**
    - **have to be discussed with LPC-Clfd management for Manpower resource**
    - **Synergy with the Collaboration has to be defined**

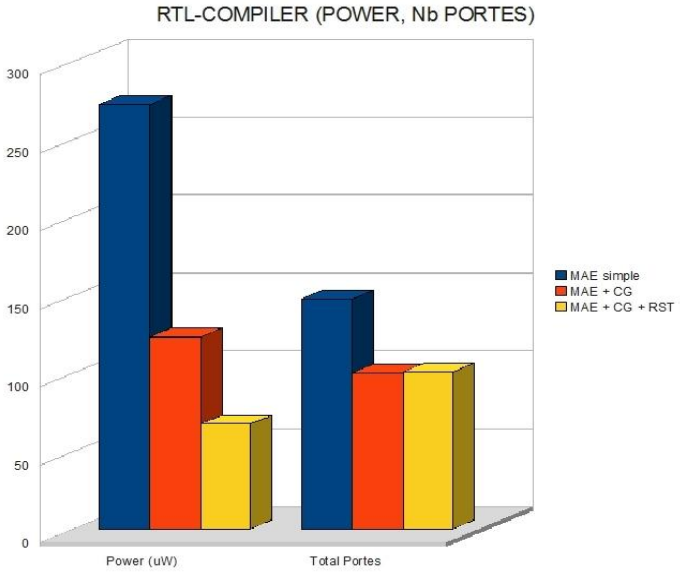
spare

Exemple avec une IP



Exemple avec l'IP qui traite les Bits sortant de l'ADC (une seule conversion): Design optimisés Vs Design simple





CLOCK = 10MHz
P Worst DESIGN = 265uW
P Better DESIGN = 68 uW

Calice in Desy March 09: our slide of Conclusion

Our 12-bit ADC: a VFE Building Block available for the Calice collaboration