Remarks of DAQ2 integration

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CALICE eDAQ
DESY
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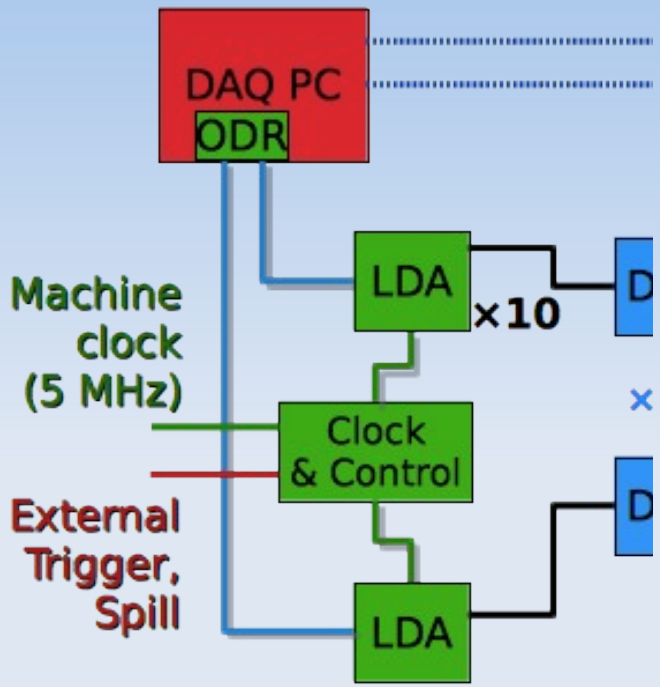
Overview

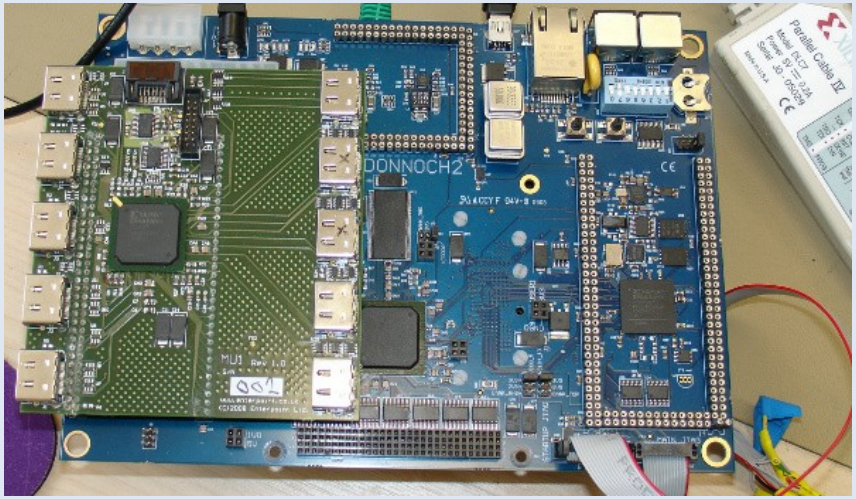
- HW and FW: Not much to say wrt talks
  - *M.Wing: LDA, CCC progress*
  - *Rémi: DIF & DCC + Stability tests*
  - *Matthias : AHCAL specificities*
  - **DHCAL DIF, CCC for small TB**
- SW: XDAQ improving for test beam (last in Mai using USB)
  - Now on SVN
  - SLCIO format for RAW data implemented
  - Integration of drivers for DAQ-II being prepared
  - **Integration of CondDB soon needed (1m² DHCAL = 144 ASICs)**
    - **Integration with previous SW mandatory**
- Next TB
- New HW (lower priority): BIF card

CCC adaptation for direct DIF Sync

- Goal:
  - replace DIF – DIF synchronisation by ring (used in DHCAL prototypes)
  - Central Clk and trigger distribution and Busy handling
- Reprogrammation of CCC CPLD
  Done by **J. Prast & G. Vouters** (LAPP)
  - Sending of fast commands (8b/10b directly to DIF) by RS232
    - Sync;
    - StartAcq
    - StopAcq
    - Reset
    - StartReadout
    - .....
- Used for
  - RPC DHCAL Cosmic
  - µMegas TB with Gassiplex
- Check Guillaume's talk tomorrow morning for more information.

HW and FW status: LDA





- LDA critical points
  - Small mezzanine CCC
    - Absolutely needed for TB
      - Broadcast of Clk, Trigger signals to DIF's
      - Merging of Busy signals (RAMfull treatᵗ or ReadOut)
    - HW (25 Cards) ready
    - FW needs to be updated
  - DIF mezzanine
    - HDMI Z adaptation
      - Dynamic adaptation (in FPGA) dropped (consumption)
      - To be implemented by 100Ω external resistors (was foreseen)
  - FW being debugged in UCL & LLR
    - Multi-Channel readout (MUX) to be fully tested this week (Matt Warren....)
    - FastCommand – Block transfert collisions on Ethernet (image next slide si pas montré par Rémi??)

HW & FW status: DIFs

- **DHCAL DIF prod launched (LAPP)**
  - Pre-serie re-launched for immediate use (n × 1 m² RPC, µMegas)
  - → to be ready (⊃ tests) in September
- **FW: Check Rémi's talk**
  - Integration of **most** DAQ2 components ✔
    (Handcheck, FastCommand & Block transfert decoding, Data Sending
    (intermediate flow ✔, high flow ~, flow control ?)
  - Integration of detector blocks
    - Modular Code of DHCAL of Guillaume Vouters (LAPP) soon to be adapted

      Can be used for all type of detectors

Data Flow for TB

- Maximum rates:
  - 3.26 kHz & 2 MB/s Single TB events for DHCAL
- Estimation (to be updated) for
  - ECAL: 1.2 kHz & 115 MB/s
  - ECAL: 5.0 kHz & 340 MB/s
- Check: https://twiki.cern.ch/twiki/bin/view/CALICE/DaqPerfs

N DIF/LDA	N DIF/DCC	LDA-DIF Dclk [MHz]	LDA-DIF FLUX [MB/s]	LDA Dclk [MHz]	LDA FLUX [MB/s]	ODR FLUX [MB/s]	Disk Flux [MB/s]
10	9	50	6.25	1000	125	1000	170

Detector	DHCAL	Evt Size	Mem Size	ASIC Dclk [MHz]	ASIC FLUX [MB/s]
		20 B	128	2.5	0.31

from LC-DET-2004-029

Mode	Calib/Noise Single	Calib/noise Burst	TB Single	TB Burst	Demo
N ASIC/DIF	48	48	4.8	4.8	4.8
σ (NASIC)	0	0	2.6	2.6	2.6
Touched DIF/pla	3	3	1	1	1
ASIC	20 B	2 560 B	20 B	2 560 B	2 560 B
R/O time 1	*64 µ s*	*8 192 µ s*	*64 µ s*	*8 192 µ s*	*8 192 µ s*
R/O time ALL	***3 072 µ s***	***393 216 µ s***	***307 µ s***	***39 322 µ s***	***39 322 µ s***
DIF	960 B	122 880 B	96 B	12 288 B	12 288 B
R/O time	*154 µ s*	*19 661 µ s*	*15 µ s*	*1 966 µ s*	*1 966 µ s*
LDA w/o DCC	9 600 B	1228 800 B	320 B	40 960 B	40 960 B
R/O time	*77 µ s*	*9,830 µ s*	*3 µ s*	*328 µ s*	*328 µ s*
DCC	8,640 B	1,105,920 B	288 B	36,864 B	36,864 B
R/O time	*1 382 µ s*	*176 947 µ s*	*46 µ s*	*5 898 µ s*	*5 898 µ s*
LDA w/ DCC	86,400 B	11,059,200 B	2,880 B	368,640 B	368,640 B
R/O time	*691 µ s*	*88 474 µ s*	*23 µ s*	*2 949 µ s*	*2 949 µ s*
ODR	17,280 B	2,211,840 B	576 B	73,728 B	73,728 B
1000MB/s	*17 µ s*	*2 212 µ s*	*1 µ s*	*74 µ s*	*74 µ s*
Disk	17,280 B	2,211,840 B	576 B	73,728 B	73,728 B
170MB/s	*102 µ s*	*13 011 µ s*	*3 µ s*	*434 µ s*	*434 µ s*
Max R/O time	***3 072 µ s***	***393 216 µ s***	***307 µ s***	***39 322 µ s***	***39 322 µ s***
Min Freq	0.33 kHz	0.00 kHz	3.26 kHz	0.03 kHz	0.03 kHz
Min. evts Freq		0.33 kHz		3.26 kHz	3.26 kHz
			2MB/s		

Occupancy for 100 GeV π in TB evts	
Mean	4.8
sigma	2.6
+3σ /√MemSize	5.49

Parameters codes
Hardware (~fixed)
DAQ (achievable)
Physics (occupancies)

EUDET memo from F. Dulucq on ASIC's interface (check on https://twiki.cern.ch/twiki/bin/view/CALICE/ASICS)

Near Future

- Need an integration meeting soon (basically FR ←→ UK)
  - Update of FW's, mounting of set-up ⊃ CCC ←→ LDA
  - Review of critical points / responsabilities
- Next Uses
  - AHCAL
    - Now (LabView + USB)
    - TB end of 2010 / 2011
      - **DAQ-II needed when ?**
  - SDHCAL
    - TB 3×m² Fall 2010 :
      - **USB + CCC (+ DCC) → DAQ-II ??**
      - *If effort put on DAQ FW*
    - Cosmics tests : Fall check of 40 planes
      - probably on USB (rates ~ 100 Hz)
    - M3 → Spring 2011
  - ECAL
    - Cosmic in Fall
      - FEV COB ; 1 chip; 1 Wafer
      - Lecture DIF USB then USB+DCC+DIF
    - Some short Slabs in Spring 2011
    - Full set-up end 2011 ?
  - W-HCAL
    - Integration of DAQ-I & II needed ?

Longer term: new HW for TB: a BIF card, integrated tests

- ILC-like TB
  - Triggerless ; start DAQ on SpillStart; recording on SpillStop | RamFull
  - ⇒ Recording of beam conditions needed with timestamp
    - Scintillator & Cherenkov bits
    - Wire or Fibre hodoscope → Timing needed ?
- BIF = Beam InterFace card
  - Pure digital information → HaRDROC (SPIROC if timing ?) or FPGA (time precision ?)
    - Readout compatible with DIF's
  - Alternative : TLU2 (developed for EUDAQ / EUDET telescope in AIDA)
- Dev^{t} integrated in AIDA
  - > feb. 2011