DAQ system hardware status

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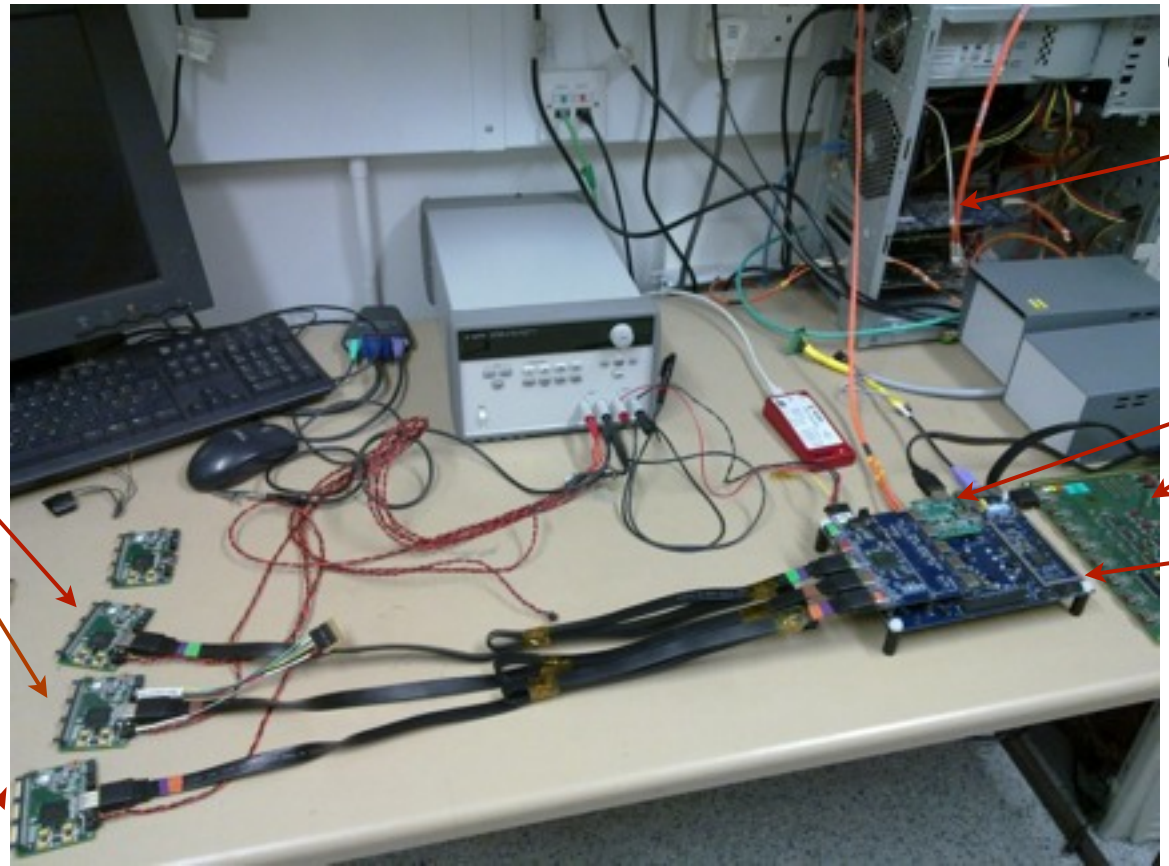
Outline

- System overview and recent progress
- Individual (hardware) component status
- System tests
- Numbers of each component and availability
- Documentation, code repository
- Summary and to dos

DAQ system overview

(**Detector Unit** : ASICs)
DIF : Detector InterFace connects generic DAQ and services
LDA : Link/Data Aggregator fans out/in DIFs and drives links to ODR

ODR : Off-Detector Receiver is PC interface
CCC : Clock and Control Card fans out to ODRs (or LDAs)



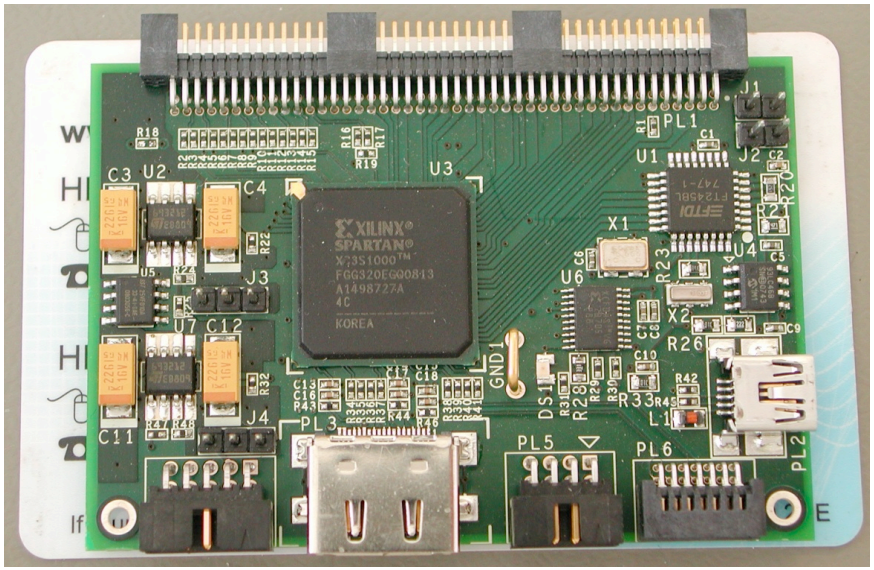
Overall status—recent progress

Have been concentrating on :

- firmware improvements and finalisation for all components;
- hardware orders to have enough systems available for lab and beam tests;
- system tests to get data passed along whole DAQ chain;
- LDA add-on board for for CCC.

ECAL DIF

- The ECAL DIF has been developed by the Cambridge group; HCAL DIFs developed by other groups, but all within the DIF task force.
- To produce a full batch of 40.
- 10 new DIFs have been produced and being used in system tests at UCL and also at LLR.
- Working well at UCL and feedback from LLR good.
- Producing 10 more at Remi's request.



- All PCBs and components in-house so can produce all 40 when needed.

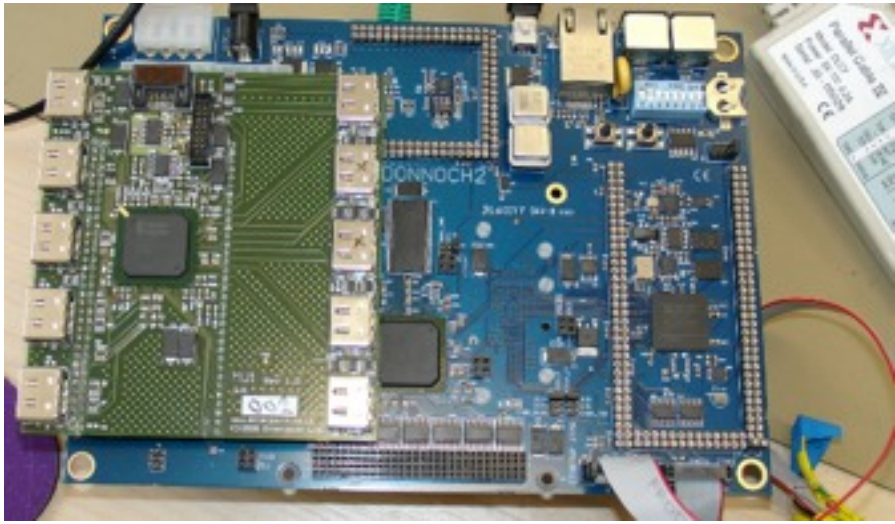
CCC

- Overall status unchanged for a while.
- Full complement of 10 boards with power supplies tested.
- One in LLR and two in LAPP.

- CCC link to LDA has been done :
  - Board designed at UCL and built at Cambridge;
  - Produced 25 boards (one for each LDA);
  - Have been using CCC to LDA as clock source in system tests;
  - Will post 3 to LLR this week.

LDA

- The LDA (from Enterpoint) consists of :
  - Mulldonoch2 baseboard;
  - add-on HDMI board to connect to 10 DIFs;
  - an add-on ethernet board to connect to an ODR;
  - a CCC add-on board.
- Firmware development :
  - still ongoing as part of system tests;
  - more later.



- Hardware status—recall all three (Enterpoint) boards had problems and needed re-design :
  - another came along with the production run; some HDMI connectors broke or broke the cable. Care needed on (un-)plugging; ease is cable dependent;
  - SAMTEC admitted fault in their connectors; 8 boards with manufacturer for repair;
  - decided to get a few more spares ...
  - should have ~25 complete LDAs by end of summer.

ODR and DAQ PC

- System has generally been stable for a while.
- Have 8 ODRs in-house along with 6 DAQ PCs :
  - one in LLR;
  - three are ready to be shipped to users;
  - decided to include a network card so do not have to use fibre which may be easier initially for some.

System tests

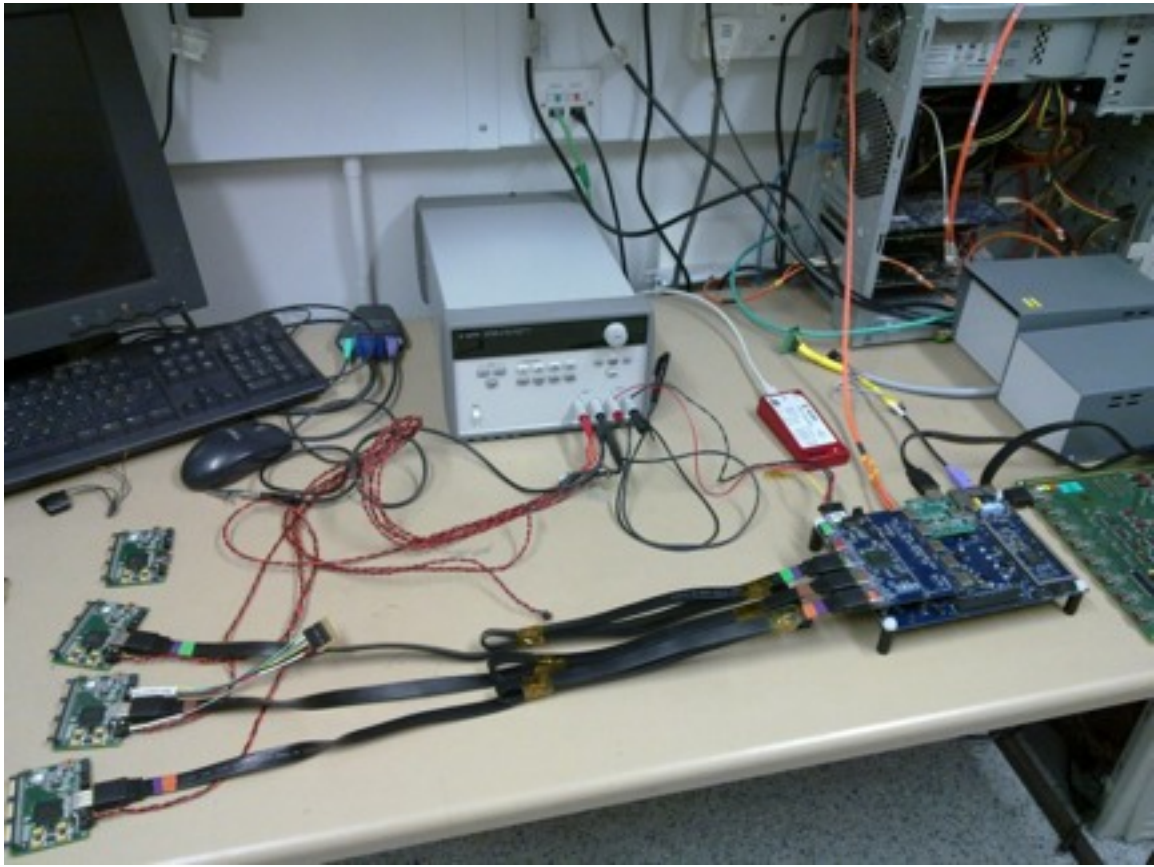
Have a system set-up in UCL :

- DAQ PC with ODR <=> LDA <=> DIF and CCC source;
- using wireshark and `scope to check data flow;
- have successfully sent fast commands all the way up to the DIF and received data packets back on the PC—full chain established;
- have successfully used CCC via LDA add-on as clock source;
- have had more than one DIF working and more than one HDMI port;

To do :

- multiple DIFs; “just” some firmware modifications.
- multiple LDAs.
- various improvements, “feature” corrections in discussion with LLR.

Ongoing ...



Hardware numbers needed

Detectors' requirements :

- ECAL : 30 layers ⇒ 30 DIFs, 3 LDAs, 1 ODR and DAQ PC, 1 CCC
- AHCAL : 48 layers ⇒ (48 DIFs), 5 LDAs, 2 ODRs and 1 DAQ PC, 1 CCC
- DHCAL : 40 layers ⇒ (120 DIFs, 14 DCCs), 2 LDAs, 1 ODR and DAQ PC, 1 CCC

DAQ groups have to provide :

- 30 ECAL DIFs, 10 LDAs, 4 ODRs, 3 DAQ PCs, 3 CCCs;
- sufficient spares for test-beam running;
- additional systems for tests in labs.

Summary of status :

- 40 ECAL DIFs (have built 10, building another 10, components for rest)
- 25 LDAs (putting together, iterating with Enterpoint)
- 8 ODRs and 6 DAQ PCs (ready)
- 10 CCCs (ready) + 25 LDA add-ons (ready)

Documentation / repository

- All components *should* have extensive documentation on twiki : it is being updated and as components are basically done, can soon be finalised.
- Twiki main :

  https://twiki.cern.ch/twiki/bin/view/CALICE/CALICEDAQ
- Also list of hardware availability /status started.

  https://twiki.cern.ch/twiki/bin/view/CALICE/HardwareList
- Code being put in CERN svn :

  https://svn.cern.ch/reps/calicedaq/

Summary

- Progress (firmware, purchasing, developing) for all components and overall system.
- We have built up a stock of components which should be sufficient for lab and beam tests. Almost complete.
- System tests are coming along with feedback from LLR.
- Stock of hardware to be delivered to detector groups. Who wants what ?

To dos

- Build all DIFs (not critical).
- Complete LDA batch; check with company and build all at UCL.
- System tests : multiple DIFs; multiple LDAs
- Ensure all work is thoroughly documented on the CALICE wiki and code stored in svn.