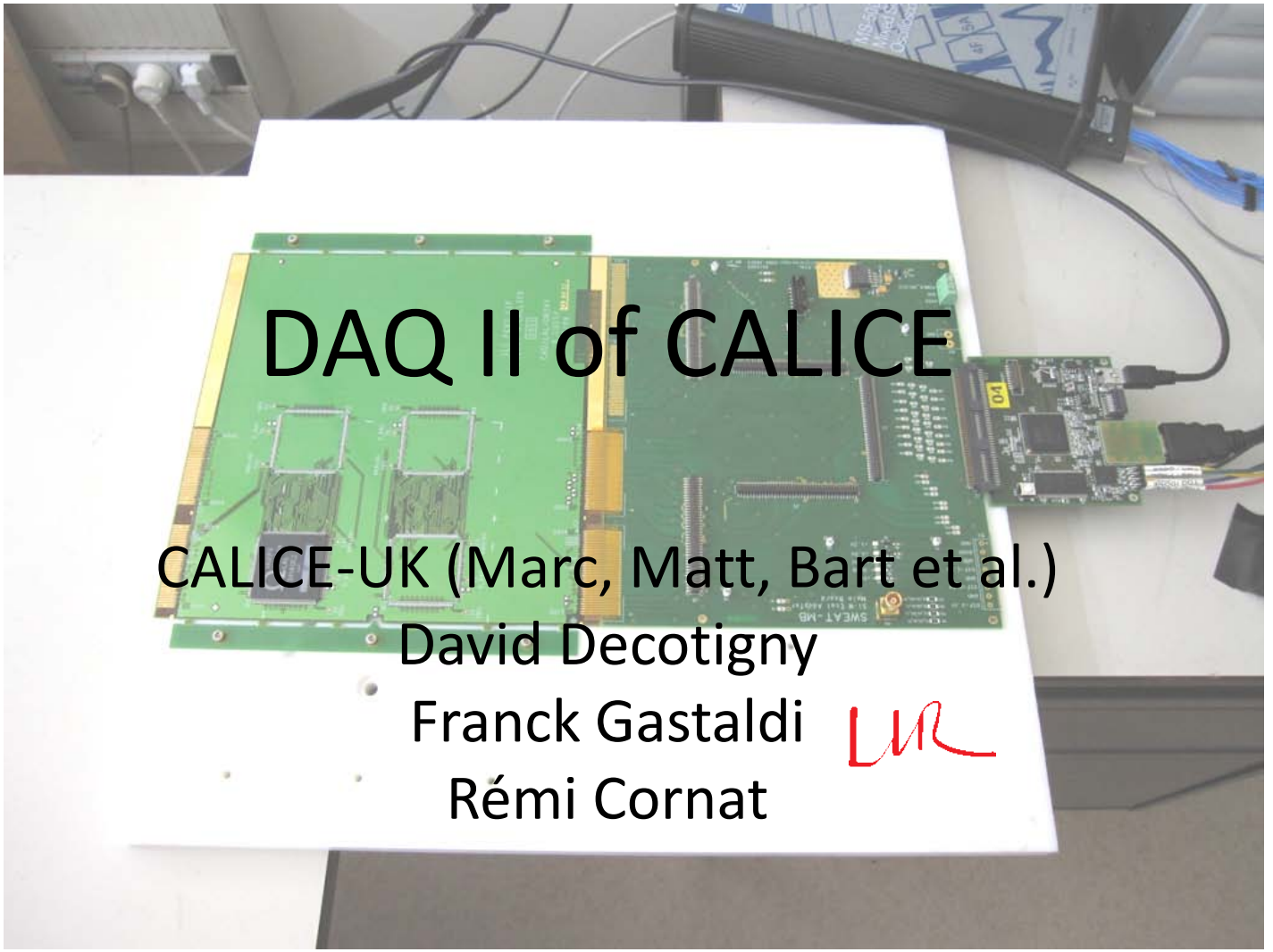
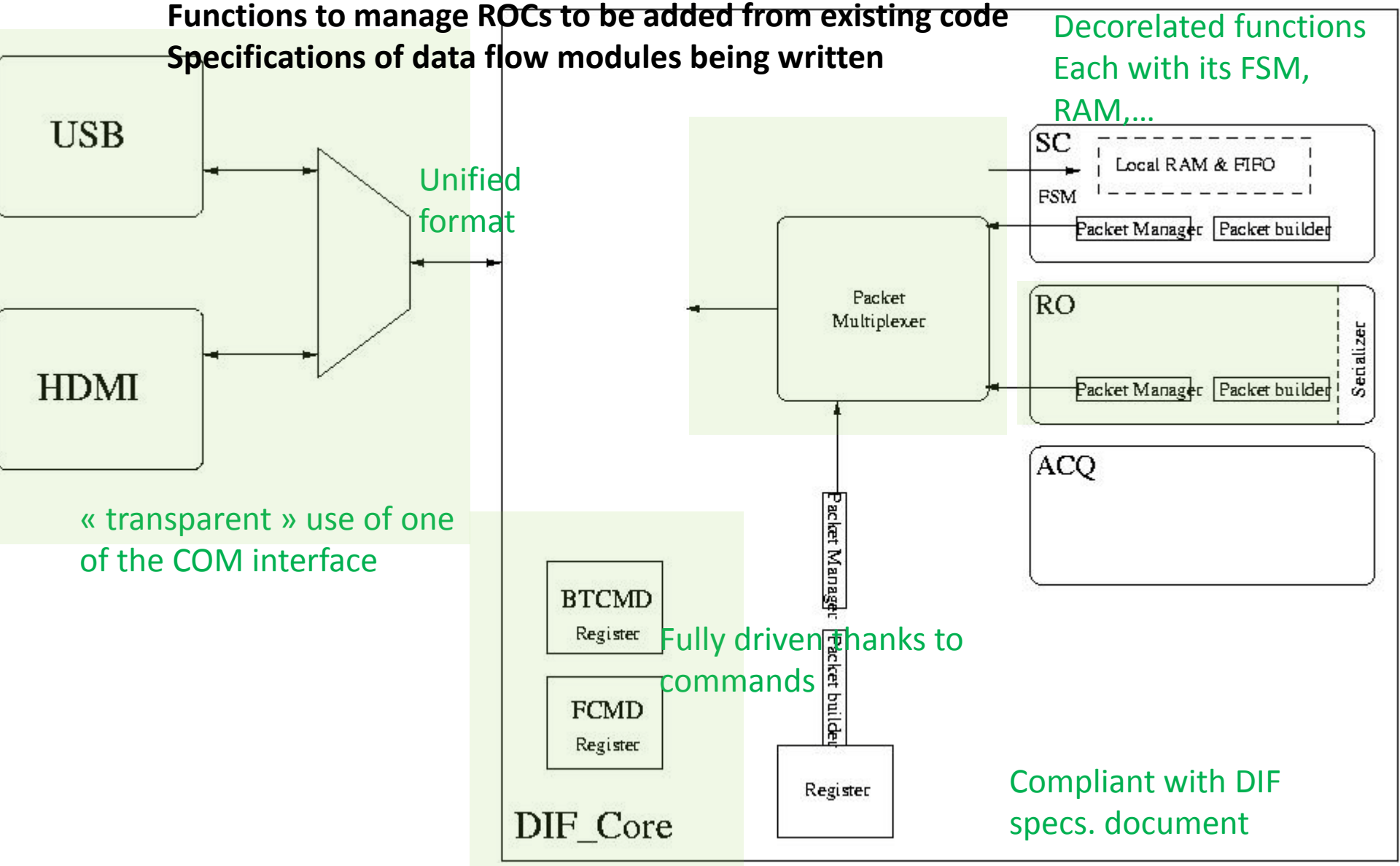


DAQ II of CALICE

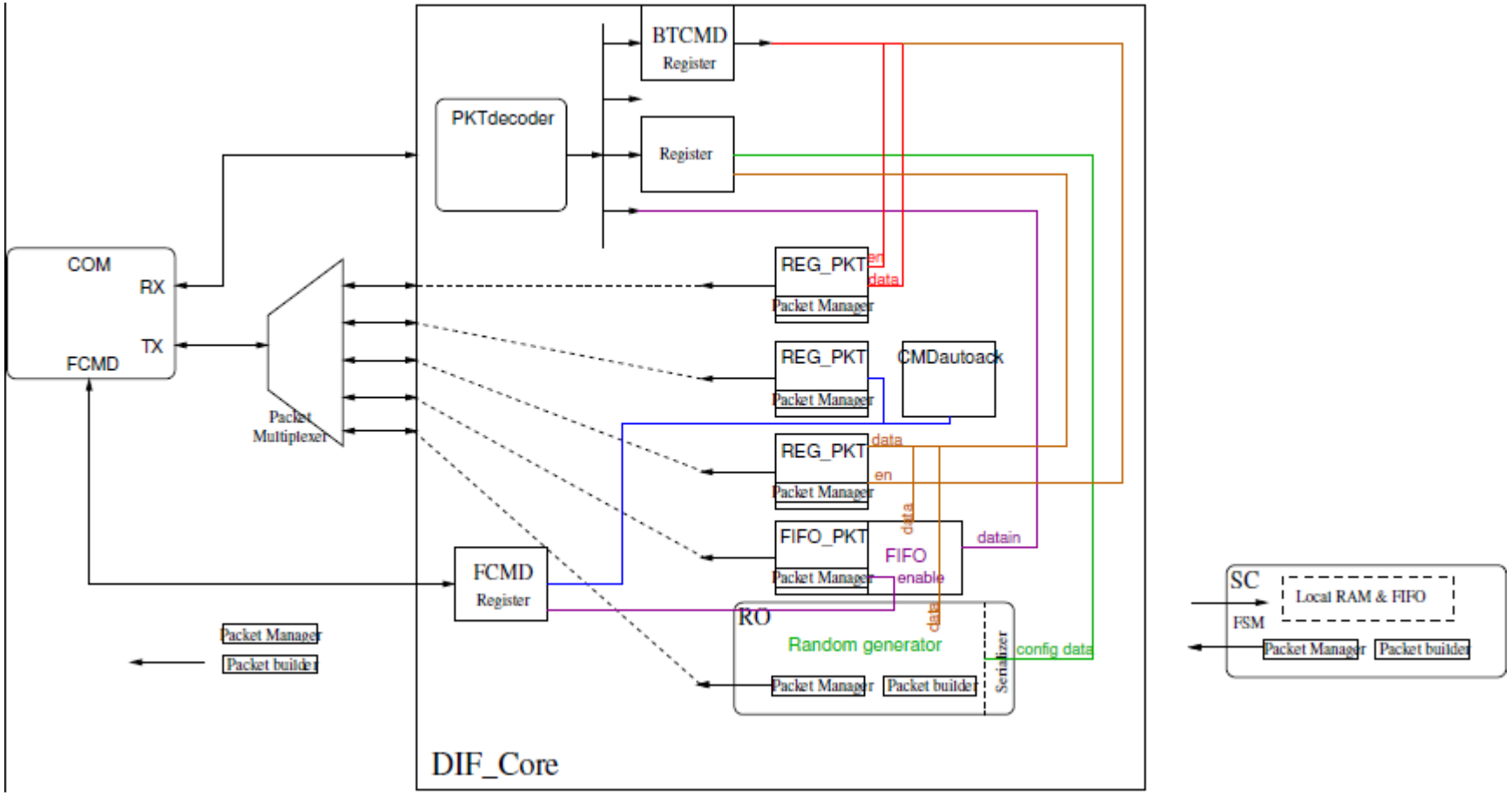
CALICE-UK (Marc, Matt, Bart et al.)
David Decotigny
Franck Gastaldi
Rémi Cornat

DIF : basic version

Functions to manage ROCs to be added from existing code
Specifications of data flow modules being written



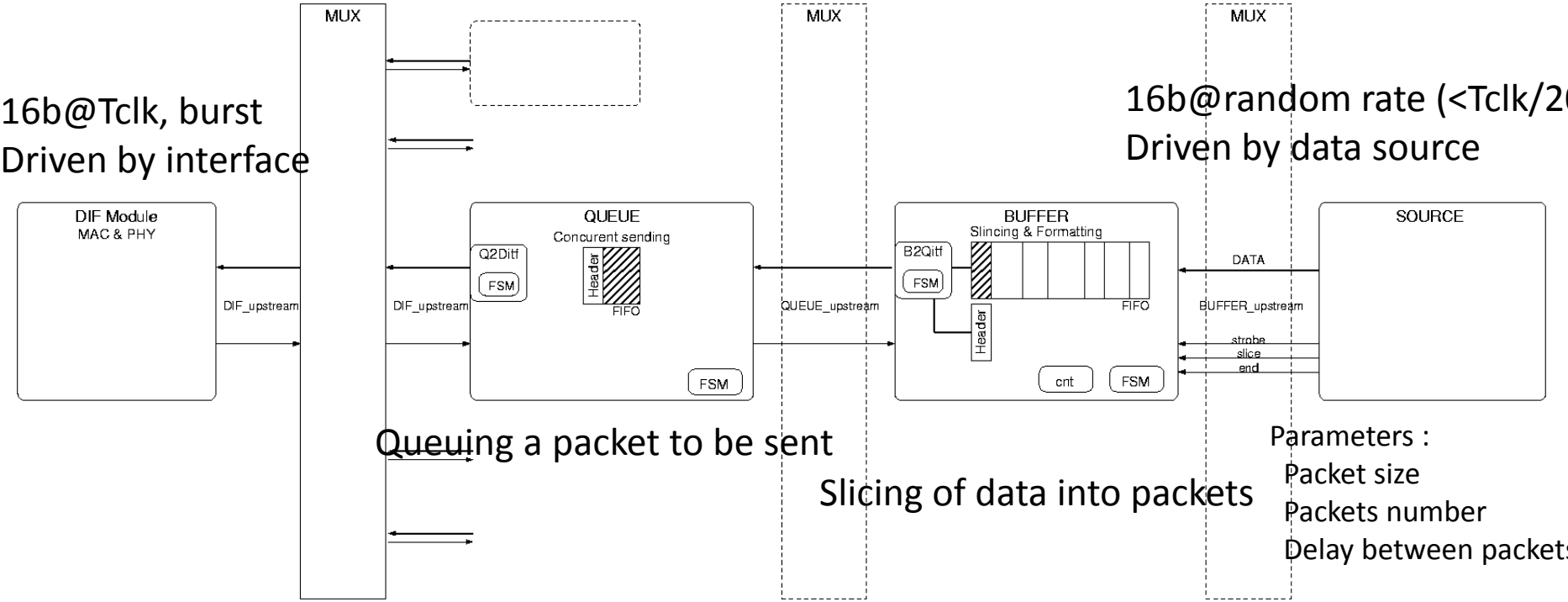
DIF firmware for testing DAQ



TX buffers

16b@Tclk, burst
Driven by interface

16b@random rate (<Tclk/20)
Driven by data source



Queuing a packet to be sent

Slicing of data into packets

Parameters :
- Packet size
- Packets number
- Delay between packets

Two levels of buffers
Modular design with similar interfaces
Handshake protocols, optional MUXs
Random data source to perform system tests

Template code will exist by the end of July on our SVN repository

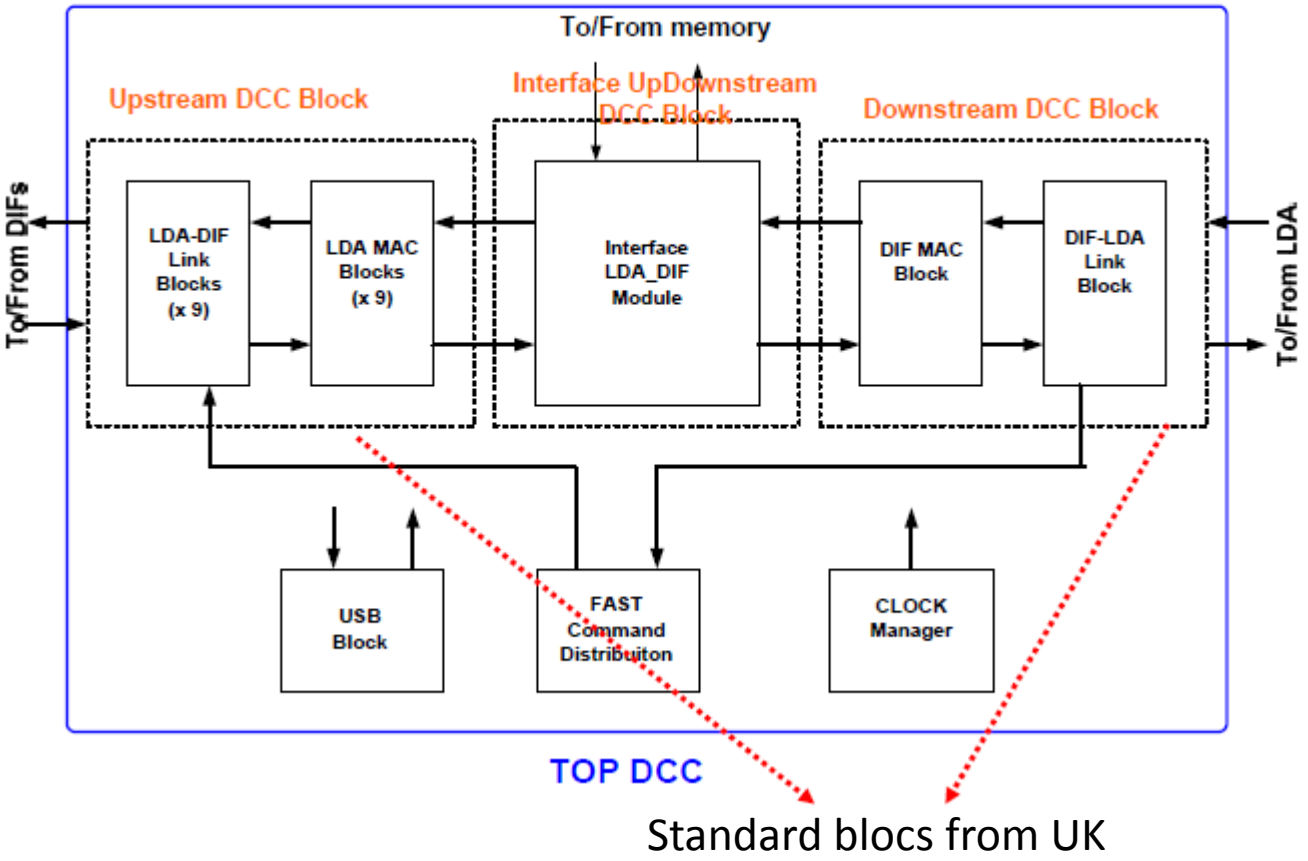
Status of DIF tests

- March'10 : DIF working with a DCC board (Done)
  - Serial link tested and validated
  - Part of specifications of the hdmi side implemented
  - USB I/O of the DCC
- June'10 : DIF working with a DCC + LDA (Almost done)
  - (almost) full specifications implemented (Done)
  - Including ROC chips functions (from Guillaume/Mathias) (In progress)
  - Ethernet I/O of the LDA (Done)
  - SW for debug & Test
- September'10 : more than 1 DIF working with a DCC + LDA (Partially done)
  - Synchronization with "final" DAQ SW (In progress)
  - Full use of CCC (In progress)
- Later on : to be discussed

DCC Firmware

- Firmware is under debug to manage 9 DIFs
- 2 kinds of access on DCC :
  - USB : DCC is like a LDA
    - DCC sends BTCMD or FCMD
    - DCC read-out DATA from DIFs
  - HDMI : True DAQ link
    - LDA sends BTCMD or FCMD to the DIFs via the DCC
      - Currently, only broadcasts are realized (no ID for the DIFs)
    - LDA read-out the DATA from DIFs (one packet after the others)

DCC firmware



The DCC is 99% transparent

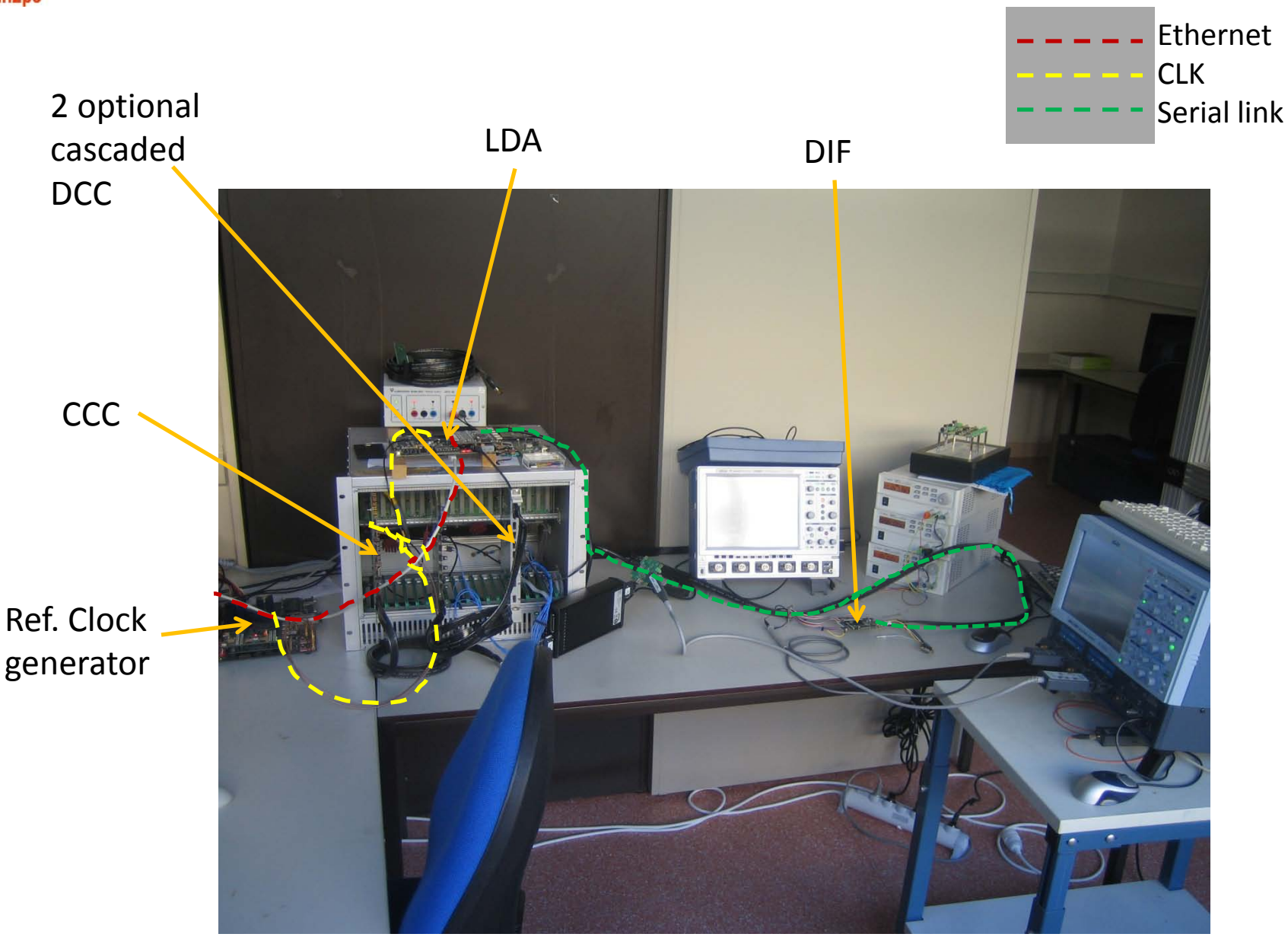
DCC Schedule

- Until August
  - DCC (prototypes) tests on DAQ chain
- DCC Firmware:
  - Everything works correctly
  - Improvements (if necessary) will be always possible for the firmware on DCC production.
- Since two weeks :
  - DCC boards in production
  - 2 boards will be (in theory) received by the end of July before a “green light” for the launch of all the production
  - We expected all boards at mid-October (it depends on the schedule of the company)
- By the end of the year : Boards should be ready for a test beam

Tests with LDA/DCC/DIF (aka. “DAQ 2”) at LLR

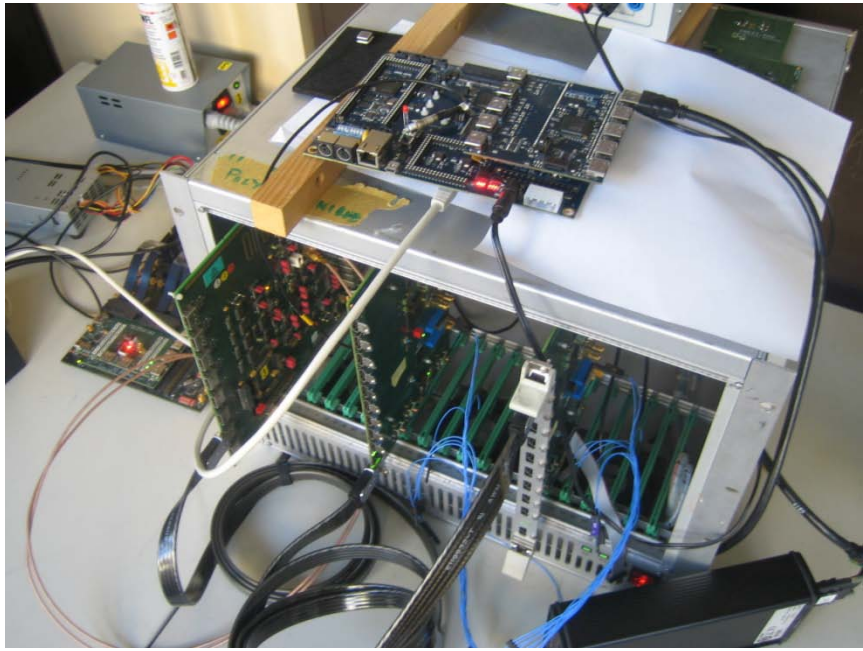
David Decotigny
Franck Gastaldi

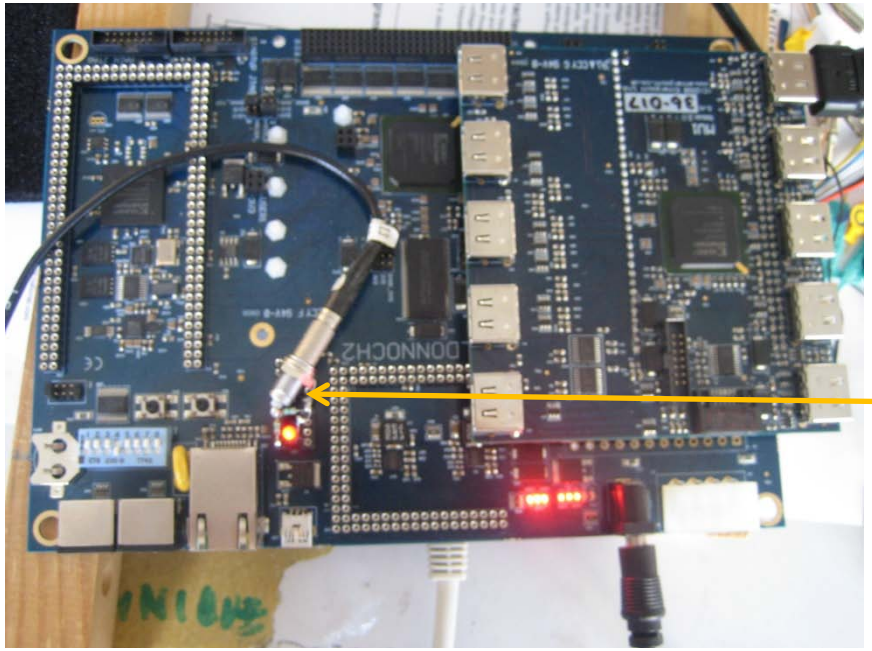
Test setup at LLR



Test setup at LLR (cont.)

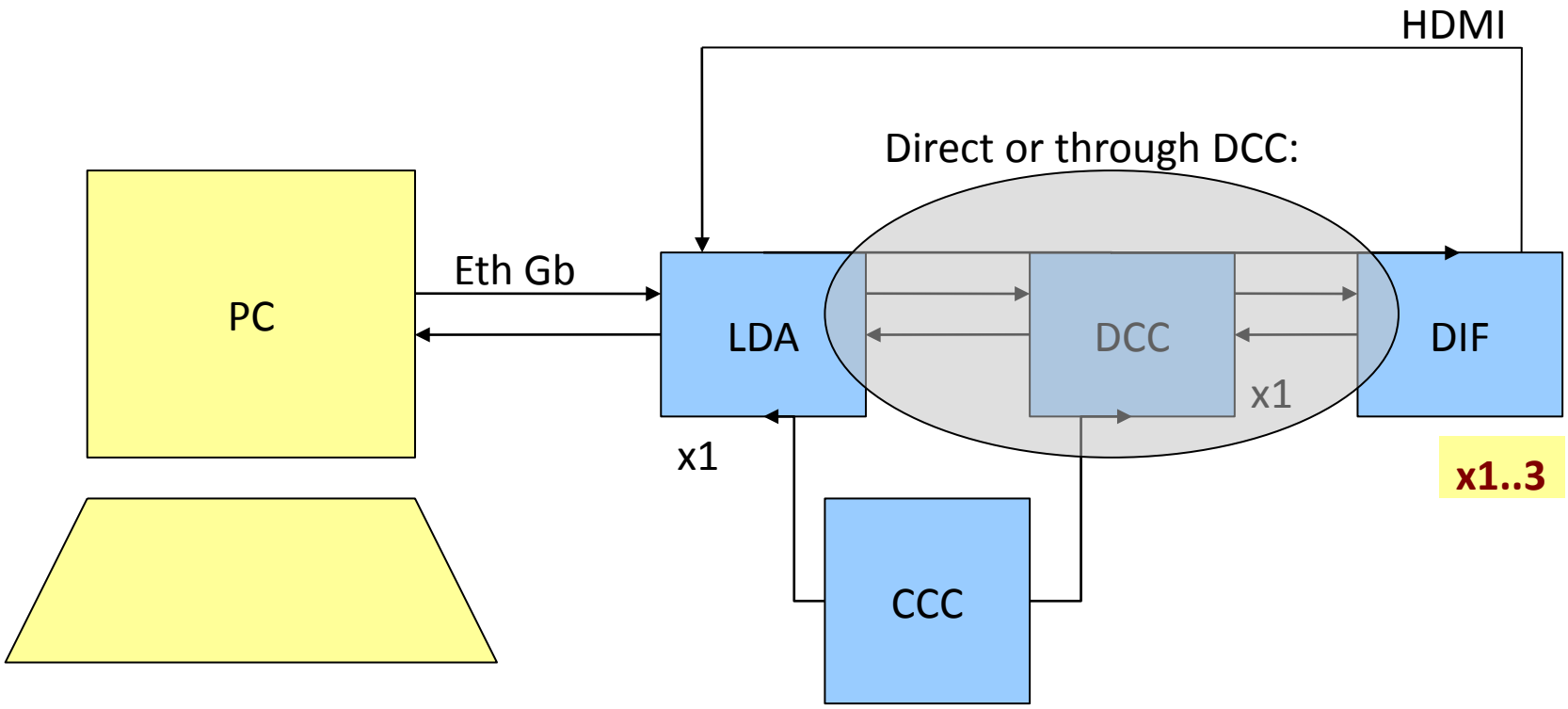
Tested data paths:
PC(Ethernet) – LDA – DIF : 1x serial link
PC(USB) – DCC – DIF : 1x serial link
PC(USB) – DCC – DCC –DIF : 2x serial link
PC(Ethernet) – LDA – DCC – DIF : 2x serial link





Clock from CCC replacing the local oscillator (TTL adapt.)

Setup overview

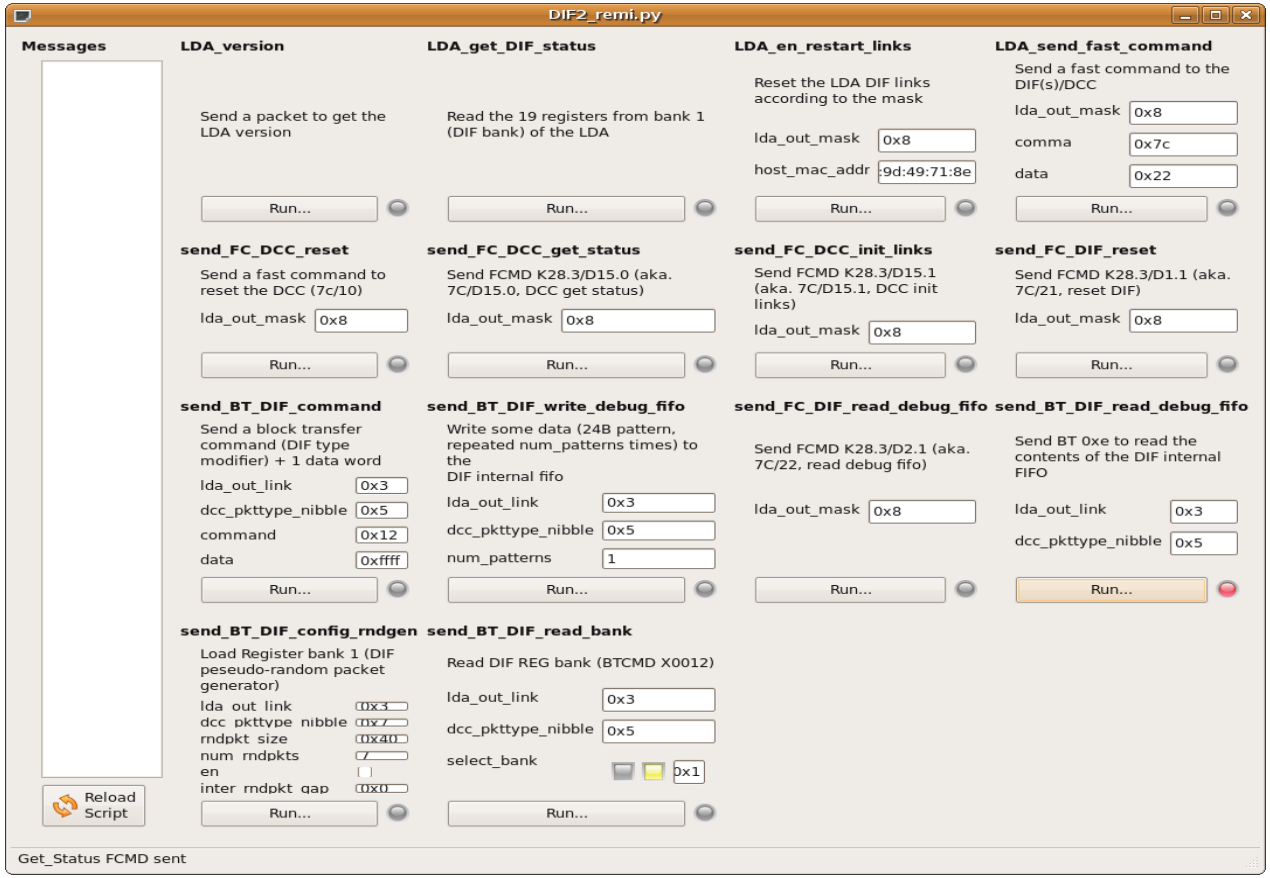


Note: everything in this talk related to the HDMI+ethernet links (USB already validated in the past)

Basic functionality tests (1/3)

Methodology

- Done by hand using a GUI



Each button = a custom python function, easy to write

Supports USB, RS232 and Ethernet devices + remotely controlled devs (XML-RPC)

Basic functionality tests (2/3)

Tests descriptions

- Implemented and validated end-to-end tests:
  - "FIFO":
    - PC sends a "WRITE" block transfer to DIF, with data
      - DIF stores data in its test FIFO
    - PC sends a "READ" block transfer or fast-command request to DIF
    - PC receives a block containing the full contents of the DIF's test FIFO
  - "RNG" (pseudo-random generator) test:
    - PC sends a block transfer to DIF to configure DIF's pseudo-random generator (nb blocks + size block)
    - PC receives the requested number of blocks + with pseudo-random sequence
      - Makes sure the pseudo-random is correct wrt RNG polynome

Basic functionality tests (3/3)

Outcome

- Validated “by hand” with the GUI:
  - Without DCC, **single** DIF:
    - Fast-Commands PC->DIF
    - Block transfers PC->DIF
    - Block transfers DIF->PC
  - Through DCC, **single** and **dual** DIF:
    - Fast-Commands PC->DIF
    - Block transfers PC->DIF
    - Block transfers DIF->PC

- Basic connectivity with LDA + DCC is here !

More intensive tests (1/2)

Methodology

- A series of C/C++ low-level tests
  - FIFO tests:
    - In a tight loop: write data to DIF test FIFO + read-back and compare
      - Data = random number of random bytes
    - Needed to insert a small delay between packets due to firmware issues (=> impairs throughput)
  - RNG tests:
    - In a loop: request 300 packets of 0x22 16b words from DIF and compare with reference pseudo-random sequence

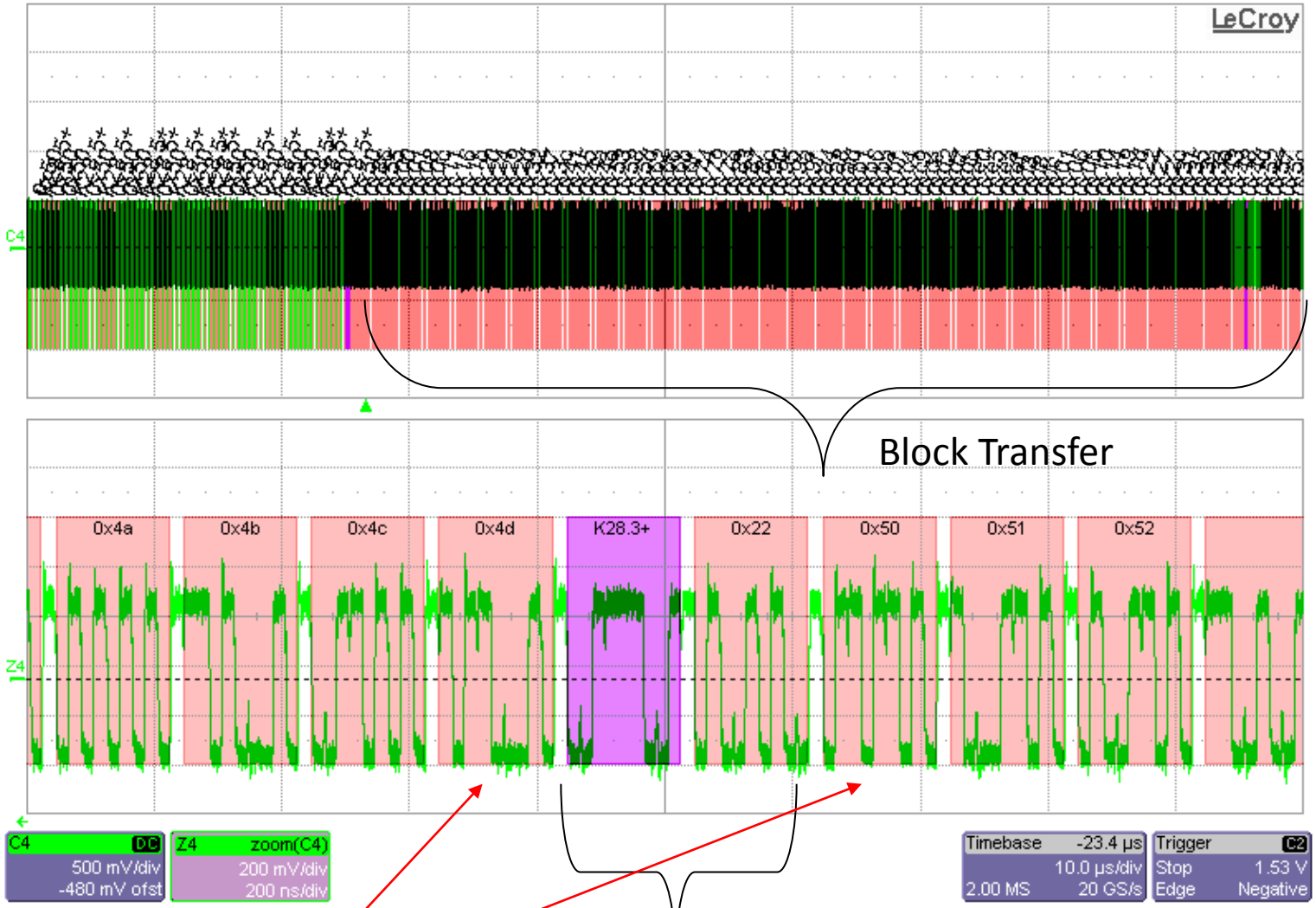
« Infinite » number of packets is being tested now at LLR

More intensive tests (2/2)

Outcome

- With and without DCC, **single** DIF:
  - FIFO test:
    - BER < 5.10^{-12} (full weekends, no error)
    - Mean throughput = 4.7 Mbps in each direction (re-adjusted to hide the 1ms delay; 3Mbps not readjusted)
  - RNG test:
    - Full weekends tests, no error

Issue 1


LeCroy
C4
Block Transfer
0x4a
0x4b
0x4c
0x4d
K28.3+
0x22
0x50
0x51
0x52
Z4
C4 DC
500 mV/div
-480 mV ofst
Z4 zoom(C4)
200 mV/div
200 ns/div
Timebase -23.4 µs
10.0 µs/div
2.00 MS 20 GS/s
Trigger C2
Stop 1.53 V
Edge Negative
Fast Command
Block Transfer altered

Issues

- Need of a mezzanine to connect LDA and CCC
  - Hardware available, require firmware modifications
  - Trigger and busy fan out/in
- HDMI mezzanine of the LDA may need some modifications to enable all the channels
  - Cable adaptation
  - Routing & Pins assignment

Our colleagues from UK are working on that

- System tests and data integrity
  - Under some condition, failure to acquire data correctly. It is under investigation (using various data generation parameters to change the mean/peak data rate).

Work ahead

- UCL/Cambridge:
  - LDA firmware updates
    - Multi-link support (for now 6 channels available, one at a time)
    - Various timing and buffer issues (data corruption observed)
    - A few features needed (eg. DIF link identification)

Our colleagues from UK are working on that

- LLR:
  - Single DIF intensive tests, ctd:
    - “Continuous” RNG: would allow to measure precise 1-way throughput
  - Multi-DIF intensive tests through DCC
    - Not working yet (data corruption), but may be a buffer or a clocking issue (will investigate with firmware triggers and/or premium scope)
  - Multi-DIF intensive tests without DCC (direct LDA)
    - Original firmware: data corruption observed, LDA freezing
    - May need to upgrade when new firmware released

But firmware of DIF, DCC and LDA is at a development stage

Outcome

- Firsts steps toward the CALICE DAQ
  - Main mechanisms of data exchange have been tested
  - 50 MHz clock
  - Data integrity with SW loop
- DIF Firmware is being developed
  - Functions to store SC data and manage ROCs
  - Common work done within the DIF task force
  - Newcomer at LLR to work on DIF & DAQ (Oct.)
- Very first detector operation foreseen this summer on Si-W ECAL prototype (1 ASU, 1 chip)
- Could be extended to other detectors
  - Please wait for the system to be fully debugged
  - Support from LLR possible
- We do not work on LDA for the moment
  - updated code ?
  - Sharing of responsibilities to be clarified