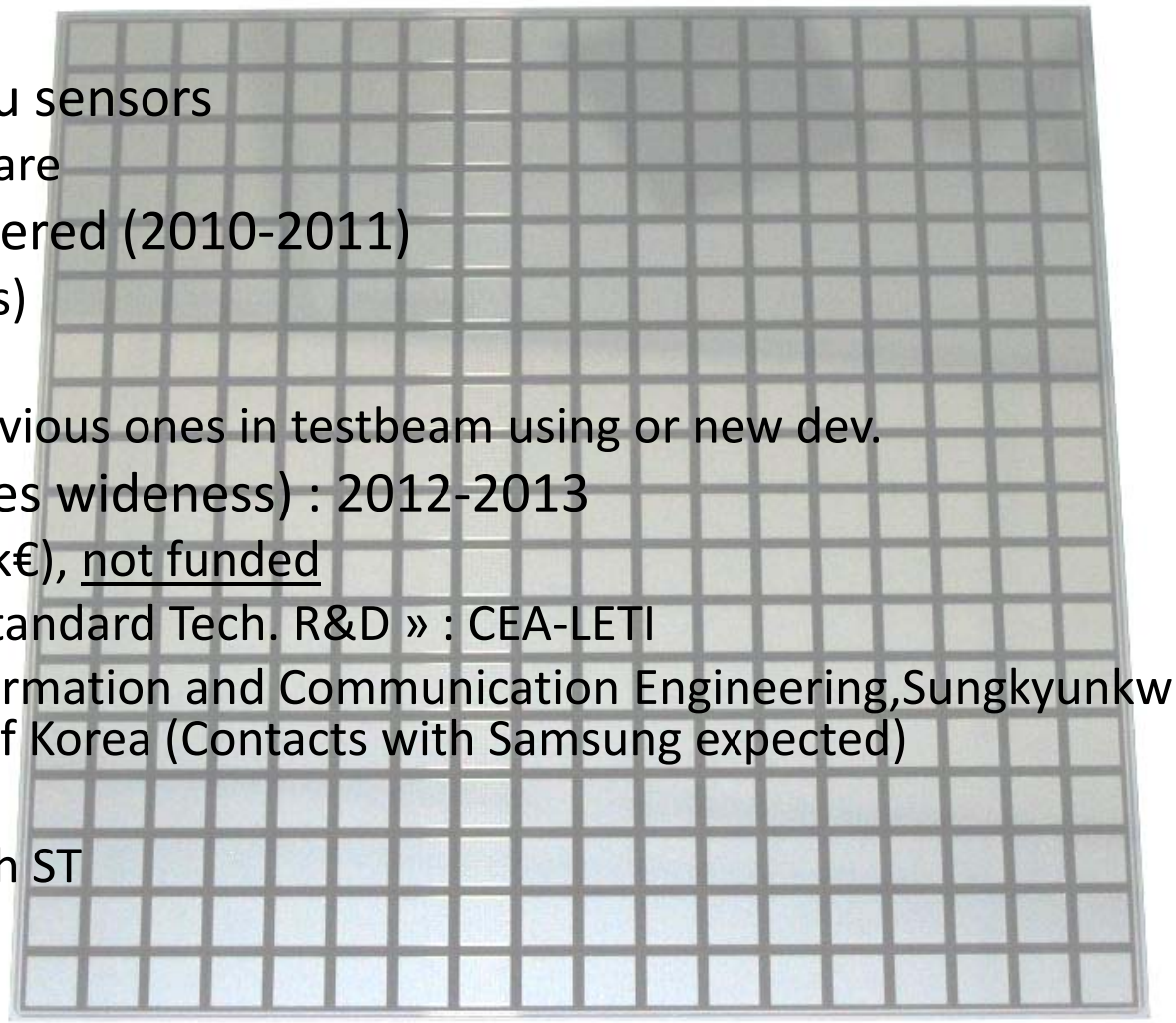

Silicon wafers for
Si-W ECAL
Rémi Cornat

Silicon Sensors (LLR)



- 40 (-1 broken) Hamamatsu sensors
  - 9 ASUs + 3 sensors as spare
- 40-50 others could be ordered (2010-2011)
  - 40-50 k€ (institute funds)
  - Not « optimized »
  - Wait for checking up previous ones in testbeam using or new dev.
- 40-50 optimized (low edges wideness) : 2012-2013
  - Costfull R&D (~100-150 k€), not funded
  - RTB program (50 k€) « Standard Tech. R&D » : CEA-LETI
  - MOU with School of Information and Communication Engineering,Sungkyunkwan University, Republic of Korea (Contacts with Samsung expected)
  - OnSEMI
  - Preliminary contacts with ST

Strategy

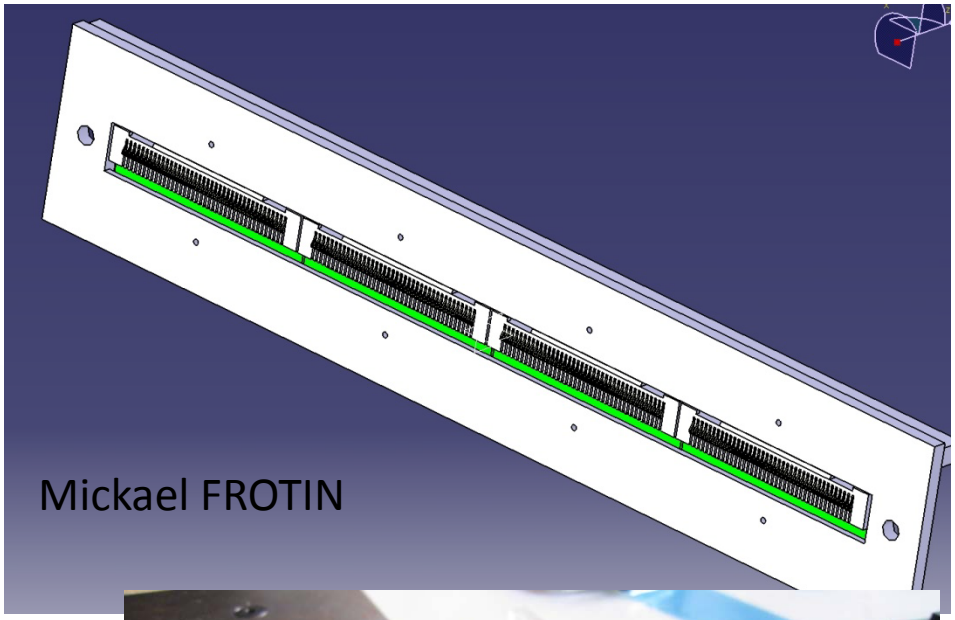
- Continue on 3x3 sensors to test new GR structures
- Gradated segmented
- Current terminating ring
- ONSEMI and BARC
- Put efforts on DAQ because it is needed to validate the designs on BEAM (+FEVx + SKIROC)
  - Hamamatsu wafers to be tested
  - Ask for quotations (SINTEF, CANBERRA, VTT, MICRON, etc…)

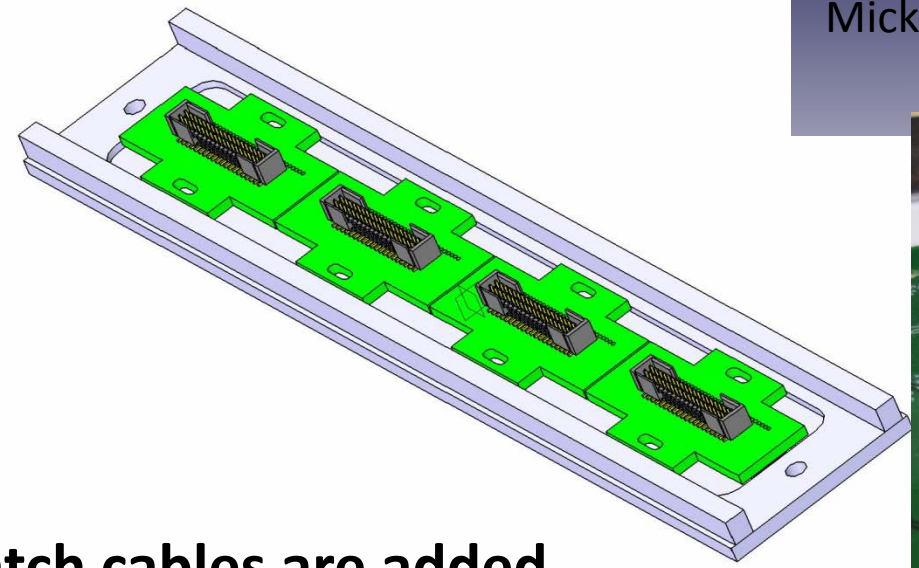
  to prepare new orders
- LETI or a technological platform (MINERVE, IMN, IEMN, LAAS)
  - Process studies, ST ?
  - Prototyping on their production line (LETI only)
  - Recipe
    - 6 cm x 6 cm sensors
    - 4 burned at the same time on a 8 inches wafer
    - Preferably on 500 µm or 700 µm tick wafer
- Backup
  - Bond the GR, feasible with FEVx and Hamamastsu
  - To be tested on 3x3 GR, test setup being duplicated at LLR (similar to the LPC one)

Solderless connector (LLR)

- Ready
- Start tests with

ASU ‘CIP’ version soon





Patch cables are added