Baseline ECal update

R. Frey (Oregon) for the ECal group

- Silicon/tungsten concept
- Baseline option: R&D progress
  - Sensors
  - KPiX readout (→ D. Freytag talk)
  - Interconnects
  - (Mechanical design for SiD)
- SiD/CLIC

- Alternative technology choice: MAPS/Terapixel progress (see Marcel Stanitzki talk)

Si/W (baseline) R&D Collaboration

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T. Nelson, M. Oriunno

Stanford Linear Accelerator Center

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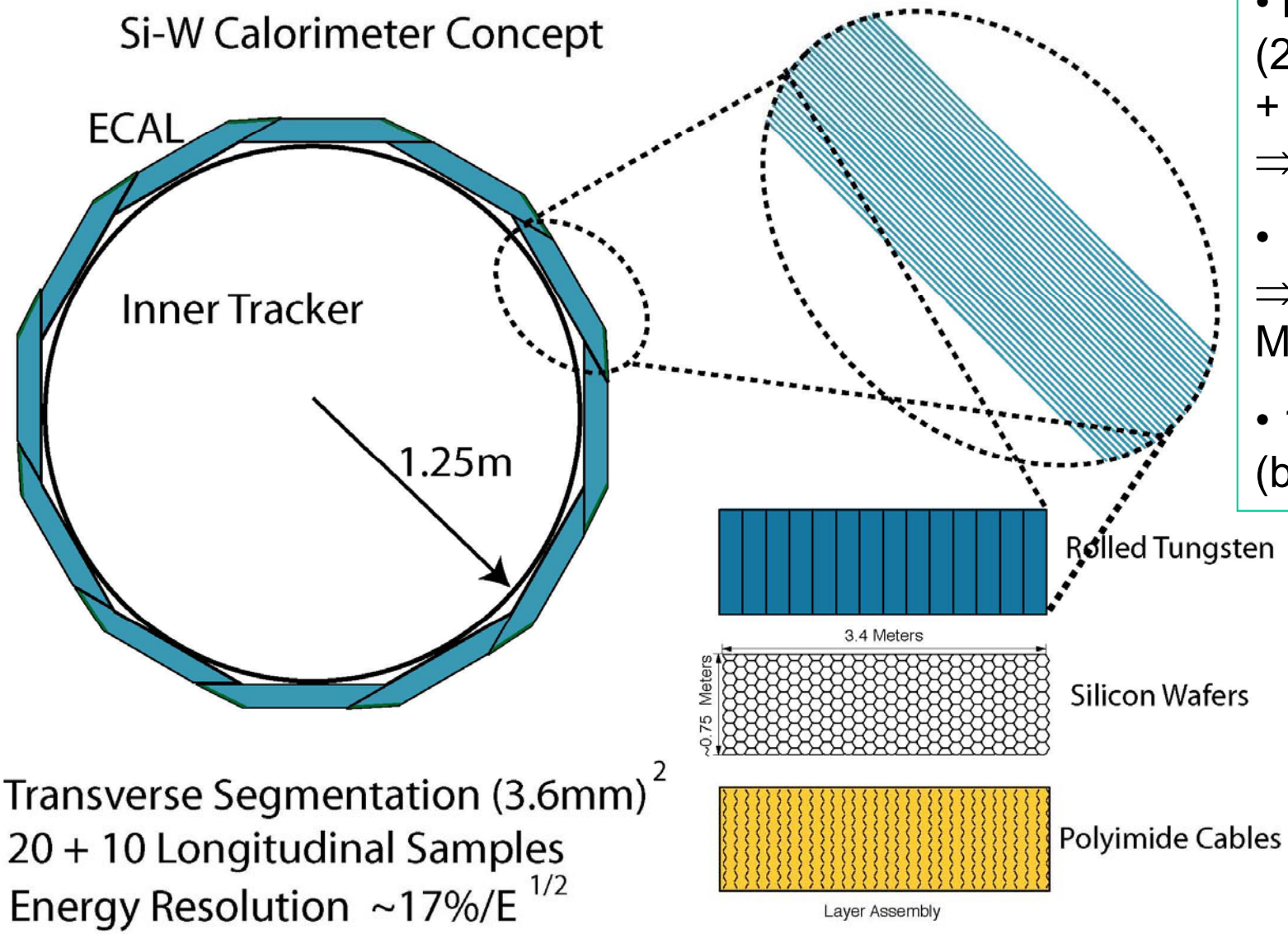
B. Holbrook, R. Lander, M. Tripathi,
M. Woods

UC Davis

- KPiX readout chip
- downstream readout
- mechanical design and integration
- detector development
- readout electronics
- readout electronics
- Interconnects: bump bonding, flex cable development

Baseline Silicon-Tungsten ECal

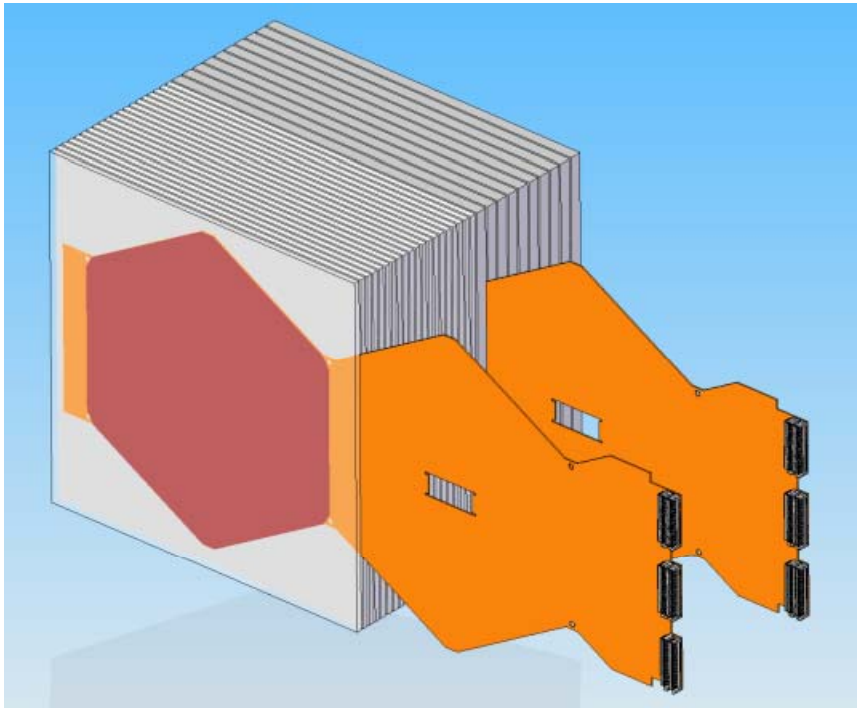


- longitudinal:
(20 layers x 5/7 X_0)
+ (10 layers x 10/7 X_0)
$\Rightarrow$ 17%/sqrt(E)
- 1 mm readout gaps
$\Rightarrow$ 13 mm effective Moliere radius
- 13 mm^2 pixels (baseline)

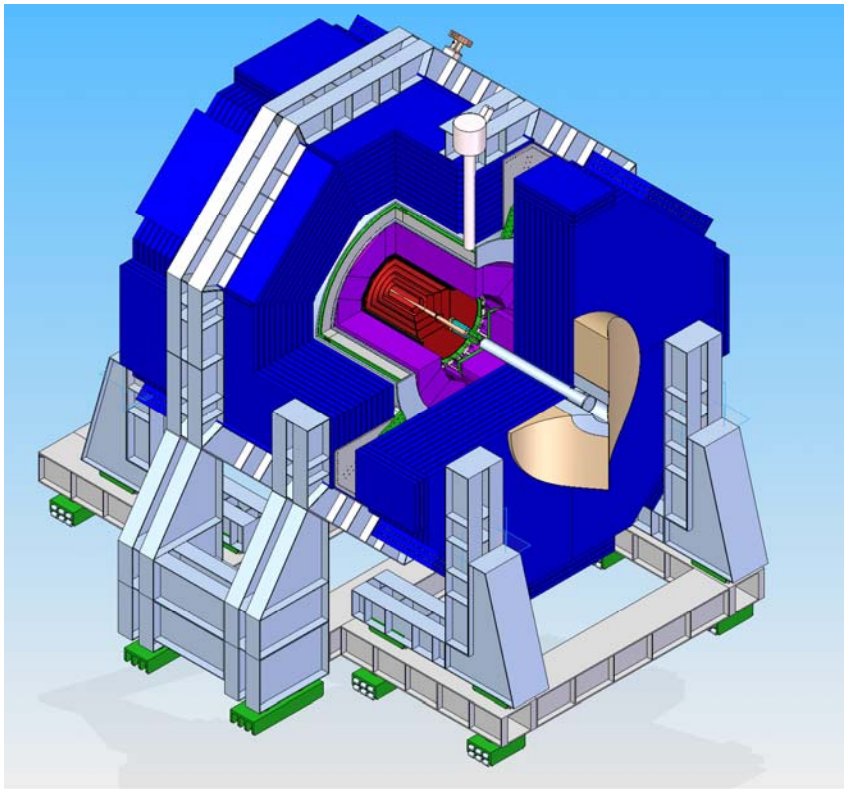
Transverse Segmentation $(3.6mm)^2$
20 + 10 Longitudinal Samples
Energy Resolution ~17%/$E^{1/2}$

Two intertwined goals

- Complete the R&D, build a test stack, and evaluate performance in a test beam.



- Fully integrate the design into SiD



R&D goals, status, plans – from ~1 year ago

	Year 1 (7/2009–7/2010)	Year 2 (7/10-7/11)	Year 3 (7/11-7/12)
Goal	Complete R&D on component technologies	Assemble test module, start beam test	Beam test, data analysis
Status	• Sensors – OK •Tungsten – OK • KPiX – 512 channel chip to be evaluated. If ok, order 1024 KPiX. • KPiX-Si bumps: need to converge on technology – gold stud thermo-compress? • Flex cable – ok • Cable-Si connect: needs R&D – ACF?	Need the integrated tests first. Flex cable can be done separately; same for DAQ	tbd
Plan	• Have 1024 KPiX and bumping technology by summer for combined testing in lab. (512 KPiX would be ok for initial combined tests.) • indium/solder bb as fallback for gold studs • Need to finalize cable-Si technology	If integrated tests look OK, begin planning for beam test. Assume SLAC beam for now.	tbd

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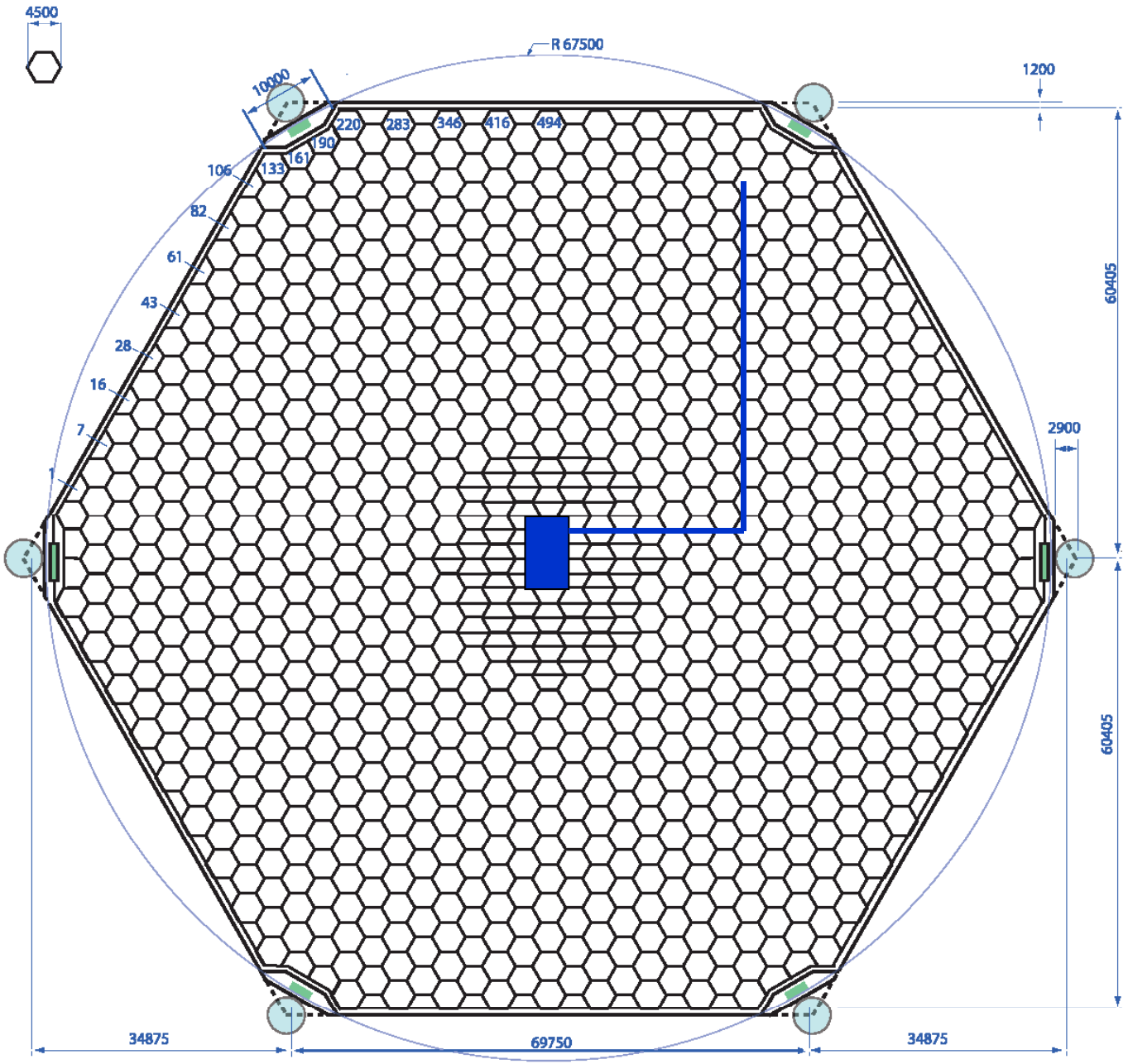
v2 Si sensors – mid 2008



- 6 inch wafer
- 1024 13 mm^2 pixels
- improved trace layout and split pixels near KPiX to reduce capacitance
- 40 good + 20 NG sensors in hand, Hamamatsu

KPiX ASIC and sample trace

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1024 chip ordered ~now

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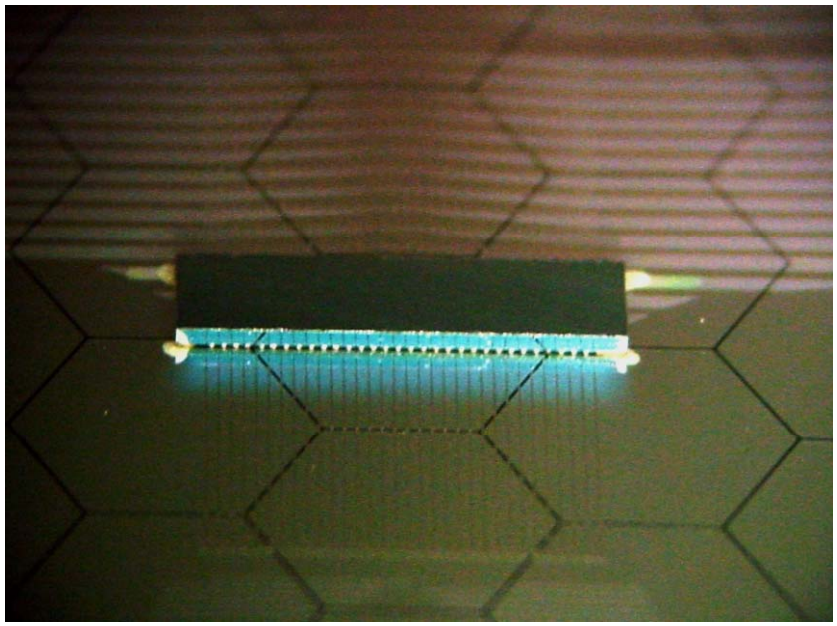
No!

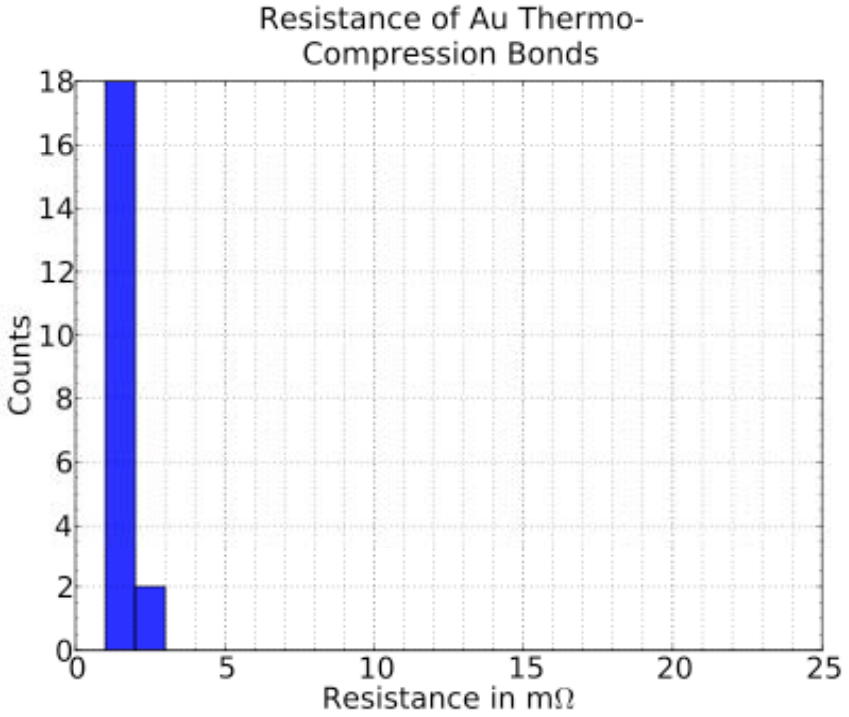
Gold-Stud Thermo-compression Bonding

Appeared to be an ideal technique for bump-bonding with prototypes:



- Complete in-house capability.
- Good results obtained with dummy chips with bump resistances <5 mΩ

- However, the same technique did not work for Hamamatsu sensor wafers because the oxide under the bump could not withstand the ~160g/bump pressure. It was crushed resulting in shorts with buried traces.



Take n: Current plan for KPiX-sensor bb

- The new version of KPiX (1024) will have solder bumps placed on it by TSMC. (!!)

- These bumps are made using the C4 process -- the solder used is high temp Pb/Sn (95/5 %).
- We (Davis) are looking to acquire an oven capable of uniform and controlled re-flow of this solder at 320° C for bonding to sensors.

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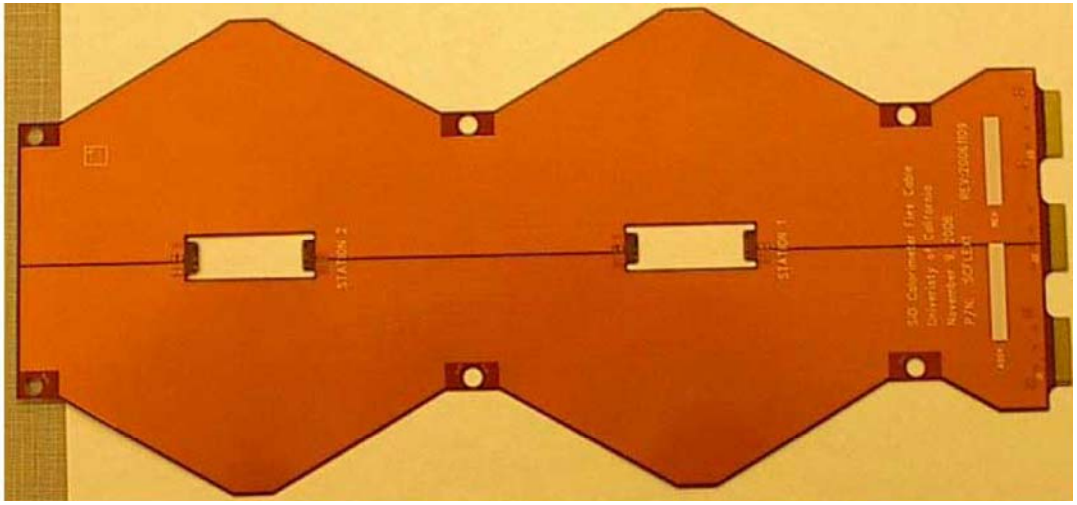
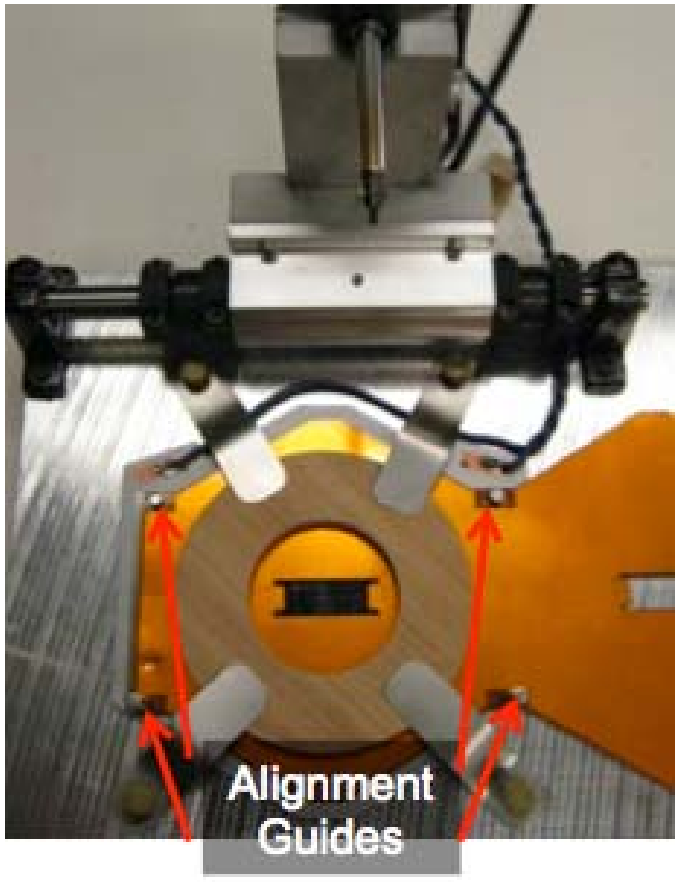
maybe

Flex cables (Davis)



Flexcables

- "OK" for test stack
- Need to check longer ~1 m cables for SiD.



Sensor connection technology:

- ACF looks promising for large-scale production
- Solder bumps – current default
  - Placed using Davis setup
  - <180 C solder
  - Trials with dummy sensors started

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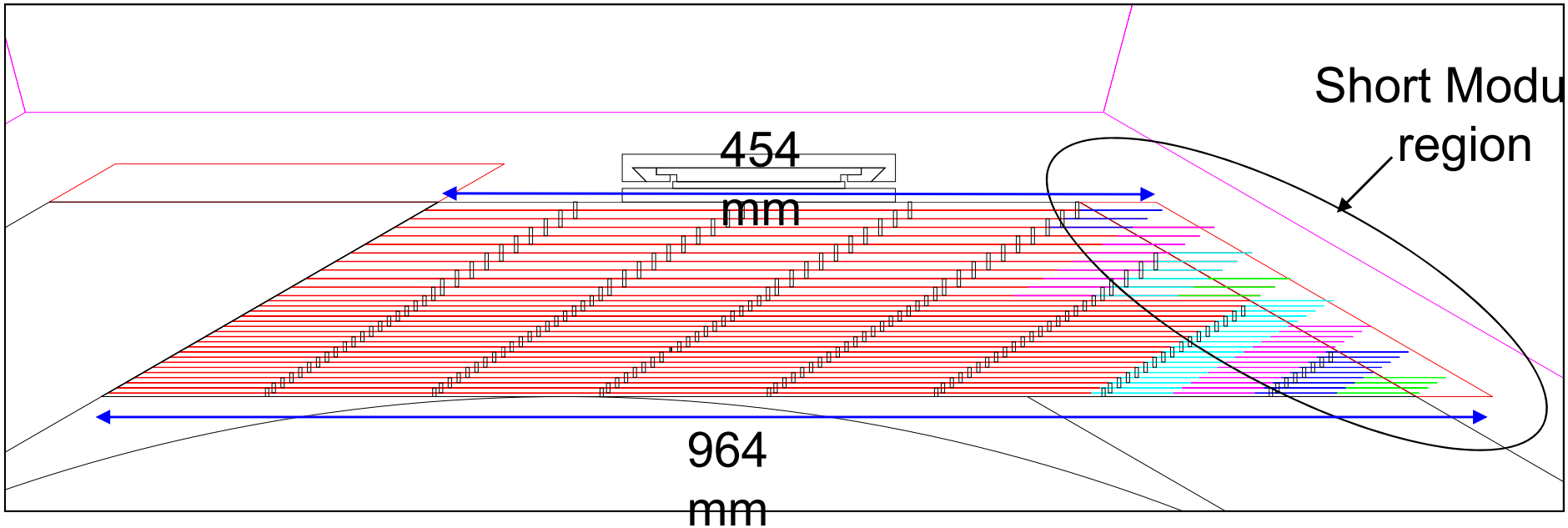
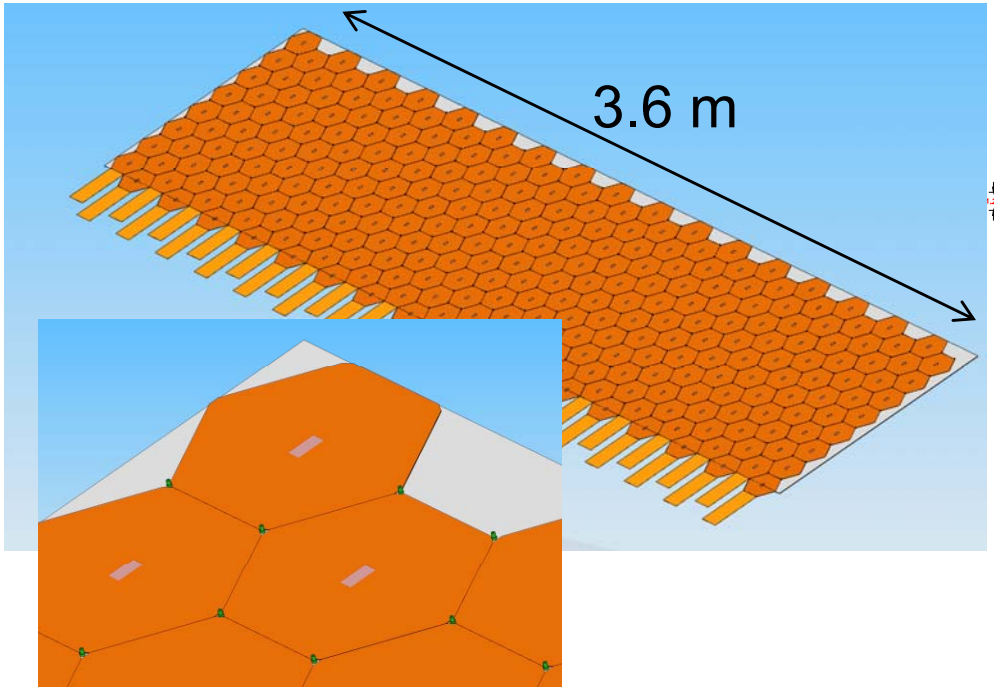
Our schedule is adjusting to that of the SLAC test beam !

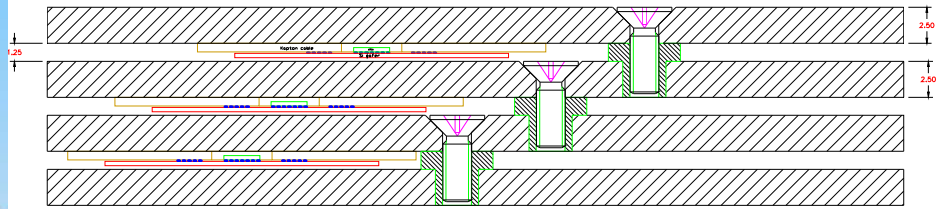
ECal barrel mech. design – Oriunno, 2008

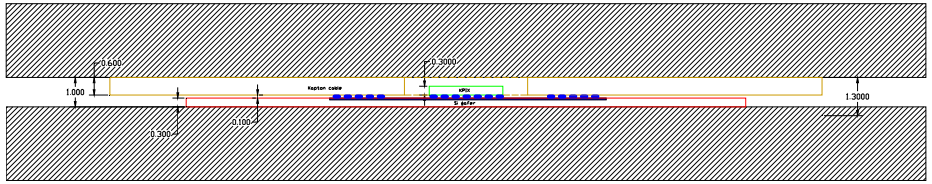




Staggered layout

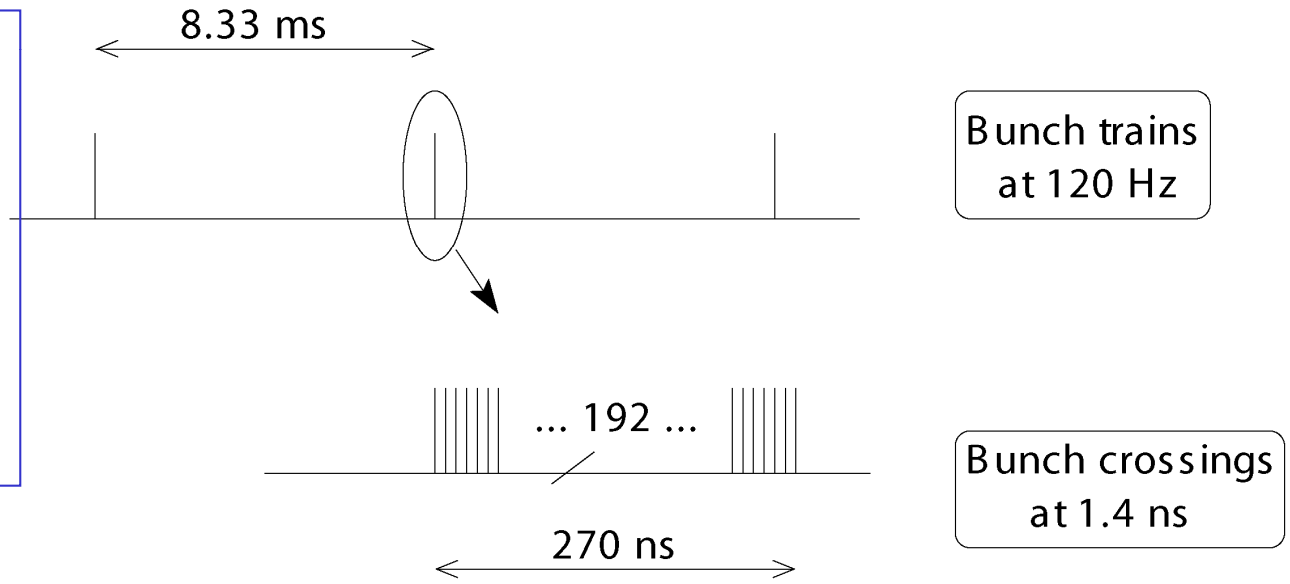
Only 2 masks for the wafer and 8 for the kapton



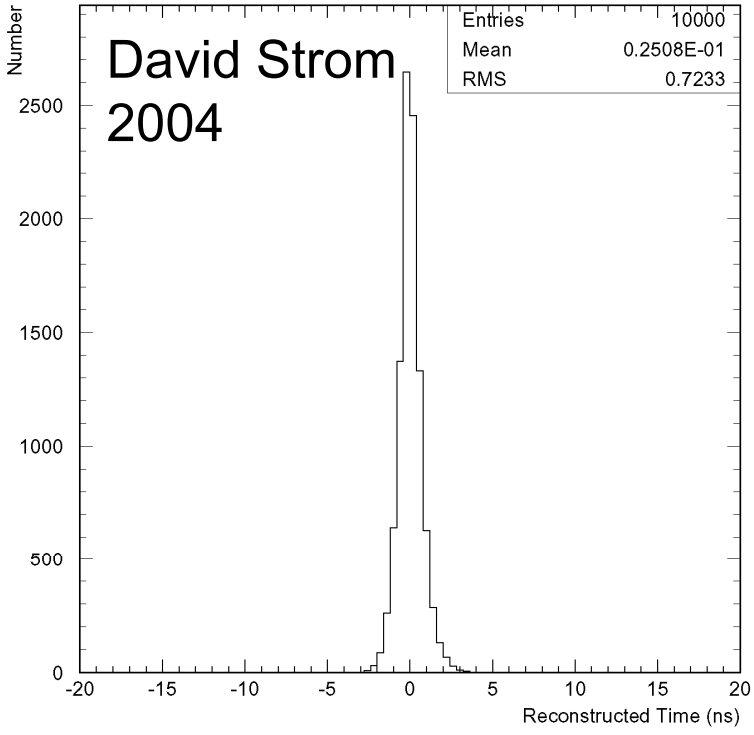


(another) CLIC connection

For warm technology, we considered the ability to do time stamping with the Si/W ECal (ca 2004)



- The ECal was ~ identical to the current baseline Si/W, but with electronics designed for warm.
- A MIP hit would give ~5 ns timing resolution per Si layer
- Result is for simulation of single MIPs (30 layers) with 50 ns time constant in preamp. →



Summary

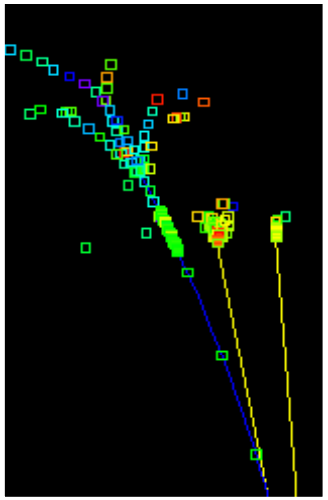
- Steady technical progress with the R&D
  - 1024-channel KPiX will be available in ~2 months
  - If bump-bonding technology works (!), we will be able to do the first system tests of the sensor+KPiX (winter 2011).
  - (Still) getting close to fabricating a test stack for a beam test.
  - (Still) compatible with schedule of SLAC test beam

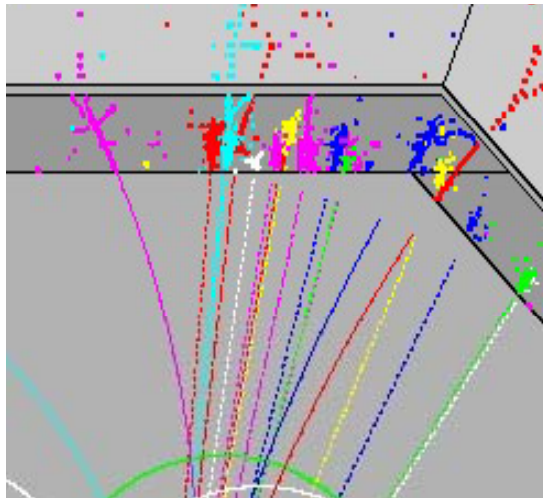
- For implementation in SiD, a number of issues to settle:
  - Finalize the mechanical design for the barrel.
  - System tests: cooling, power delivery, correlated noise, etc.
  - Need a tiling scheme and mech. design for the endcaps
  - Reconstruction effort welcome, e.g. photon id in jets

Physics, ECal, LOI

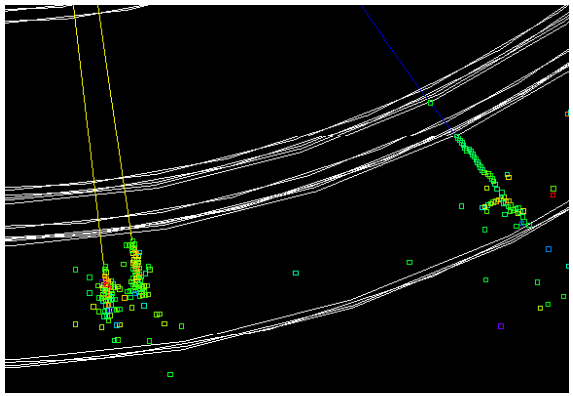
Guiding principles: Measure all final states and measure with precision

- Multi-jet final states
  - π° measurement should not limit jet resolution
  - id and measure h° and $h^\pm$ showers
  - track charged particles
- Tau id and analysis





- Photons
  - Energy resolution, e.g. $h \rightarrow \gamma\gamma$
  - Vertexing of photons ($\sigma_b \sim 1$ cm), e.g. for GMSB
- Electron id
- Bhabhas and Bhabha acollinearity
- Hermiticity



$\Rightarrow$ Imaging Ecalorimetry can do all this