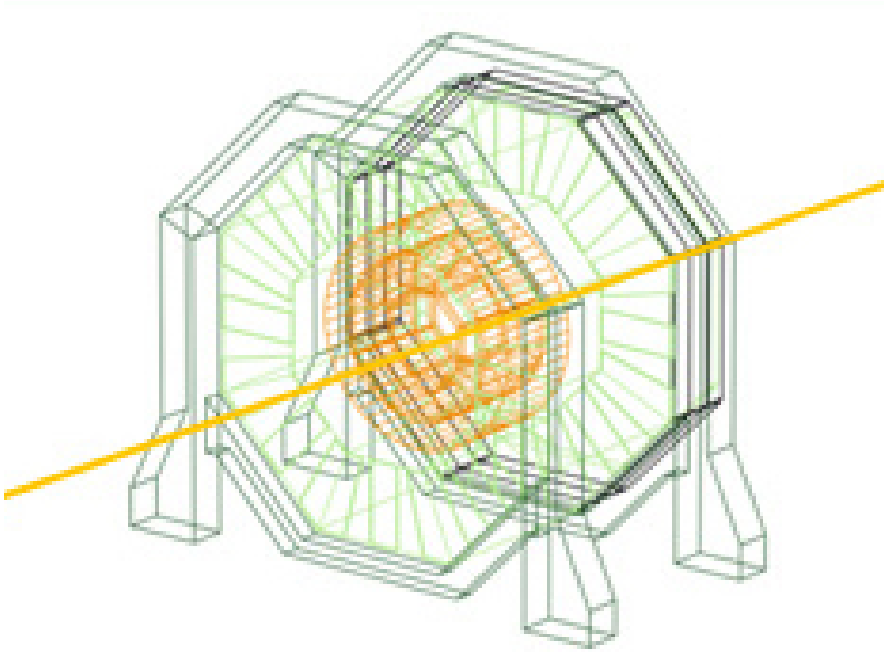
SiD Vertex Detector Technologies



Marcel Demarteau

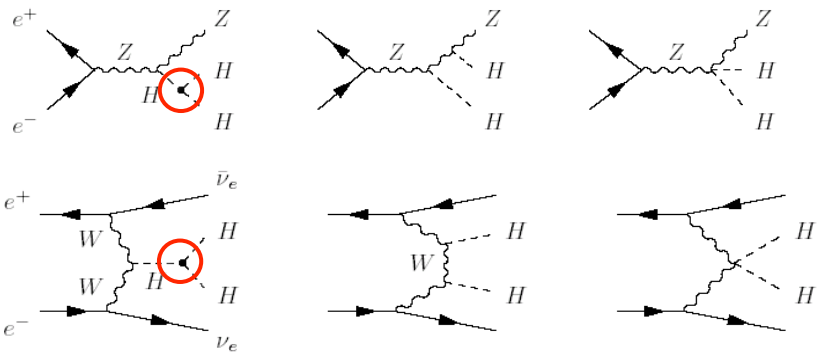
Argonne National Laboratory

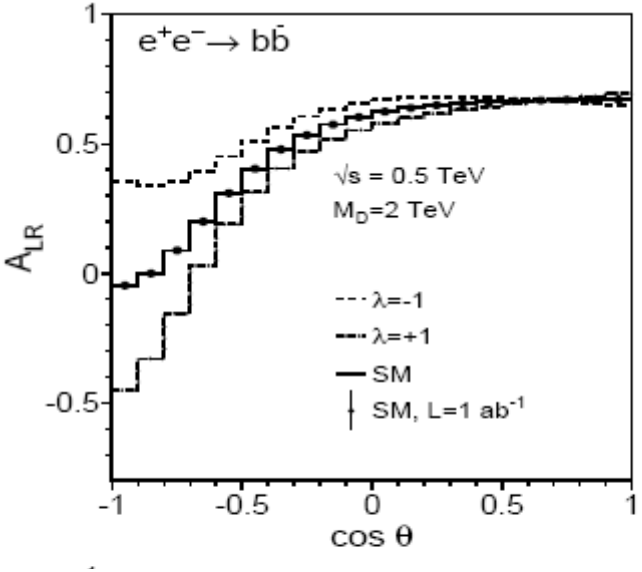
For the SiD Vertex-Tracking Group

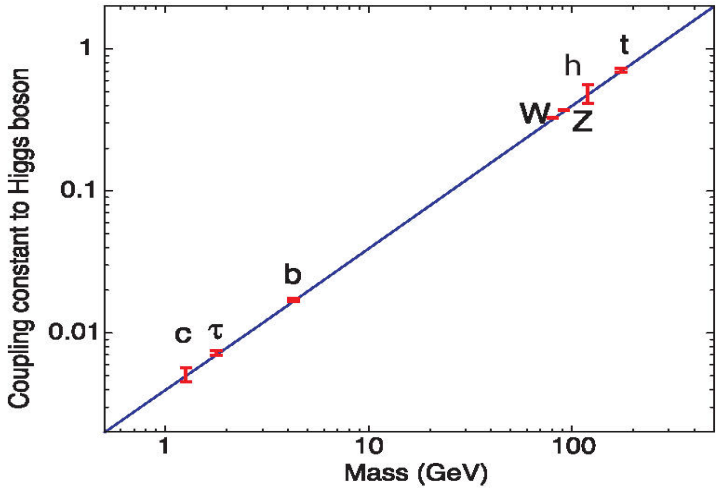
SiD Collaboration Meeting
Eugene, Nov. 15-17, 2010

Physics Impact

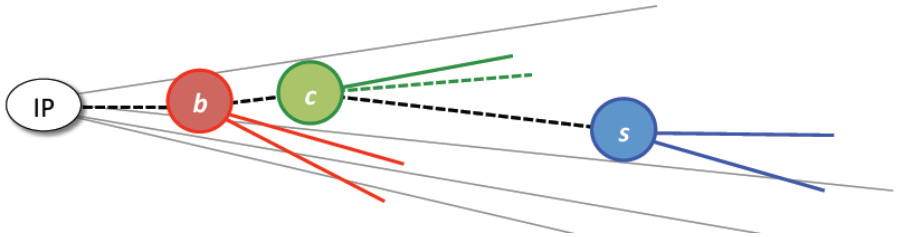
- **There are numerous physics processes where flavor tagging plays a critical role**
  - **Standard model physics: Higgs**
  - **Beyond the standard model**







- **Reconstruct the whole decay chain**



Research Thrusts

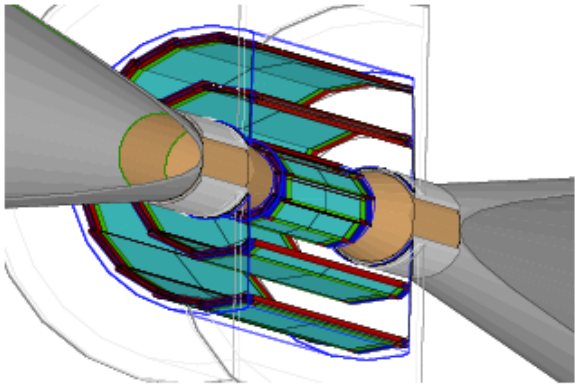
- Precision vertexing/tracking/imaging ideally requires detectors that have
  - zero mass: transparency of ~0.1% X_0
  - zero power: allow for air cooling (< 50 W)
  - zero dead zones
  - zero dead time
  - zero effective occupancy: integration over few bunches
  - zero noise susceptibility: EMI immune
  - 1/zero precision: spacepoint < 5μm,
    impact parameter $5\mu m \oplus 10\mu m/(p \sin^{3/2}\theta)$)
  - 1/zero pattern recognition capability: many layers close to IP
  - Modest radiation hardness

- These aggressive set of goals and the physics need, has led to a wide range of R&D based on established and emerging technologies

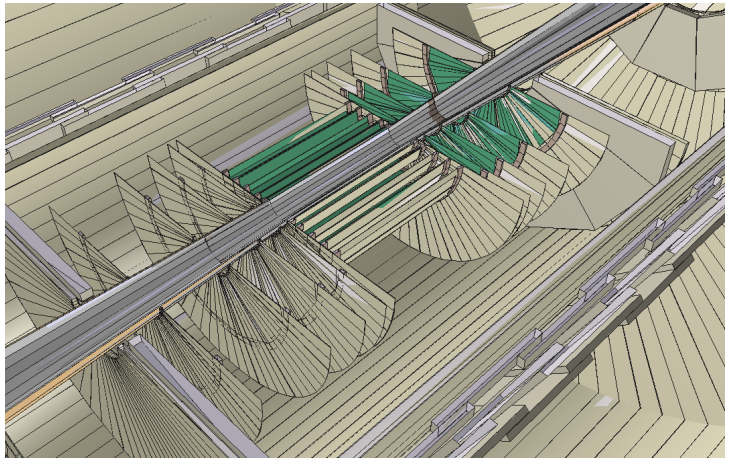
- No technology has established itself yet. It is expected that the experiments will choose the best technology that will meet their needs at the time of the technical design

Detector Design Options

- **Long Barrel Configuration (ILD)**
  - Single geometry for all layers
  - Large charge sharing at small angles and larger occupancies
  - More mass on particle trajectory at small angles (?)
  - Limited number of space points on particle trajectory at forward angles



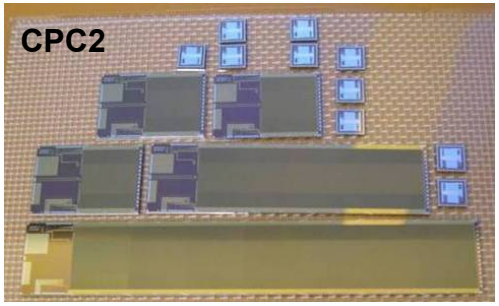
- **Barrel and Disk Configuration (SiD)**
  - No precedent for disk geometry for pixel planes and associated services
  - Uniform angular coverage and response

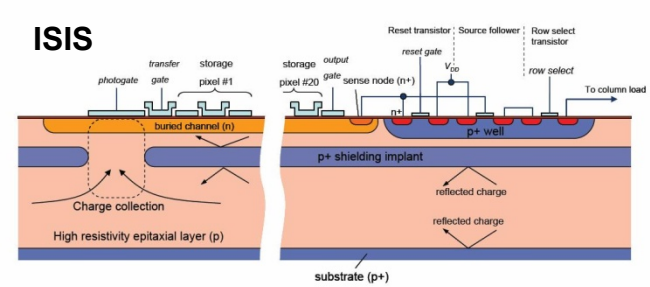


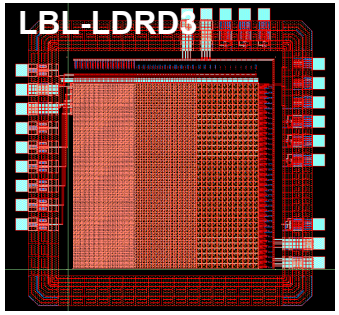
- **Support Options**
  - Carbon fiber support structures
  - Integrated support through etching of silicon sensors
  - Support provided solely by Si sensors

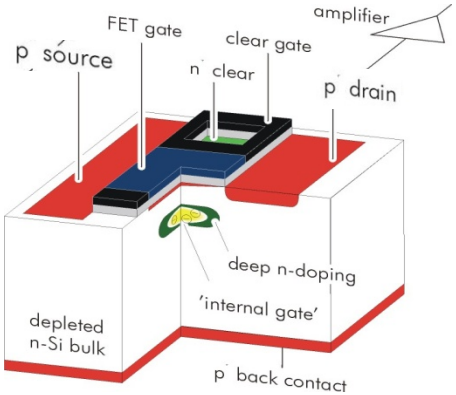
Vertex Detector Sensor Technology

- **Broad spectrum of sensor technologies are a candidate technology for the ILC vertex detectors**
- **CCD's**
  - **Fine Pixel CCD (Japan)**
  - **Column Parallel (LCFI) †**
  - **ISIS (LCFI) †**
  - **Split Column (SLAC) †**
- **CMOS Active Pixels**
  - **Mimosa series (Ires)**
  - **MAPS (INFN)**
  - **LDRD 1-3 (LBNL) †**
  - **Chronopixel (Oregon/Yale)**
  - **LePix**
- **SOI**
  - **OKI/KEK (Imaging)**
  - **FNAL**
  - **LBNL**
- **3D Vertical Integration (Fermilab)**
- **DEPFET (Munich)**

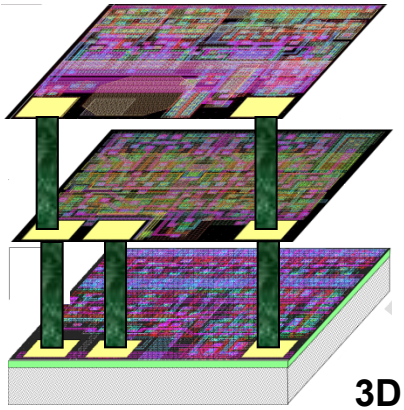






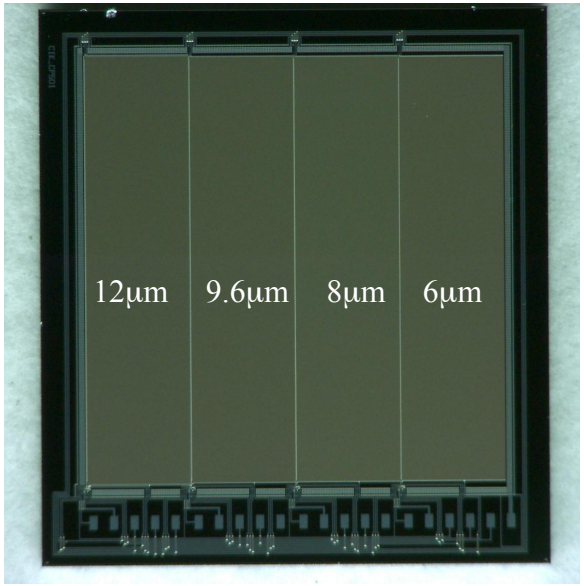


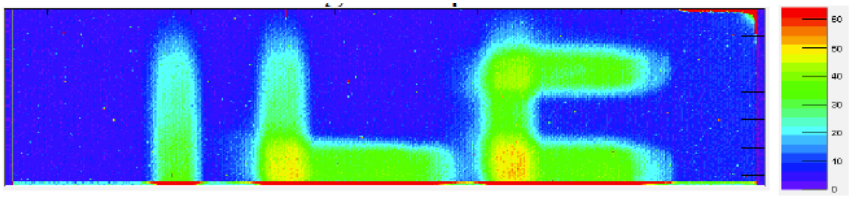
DEPFET

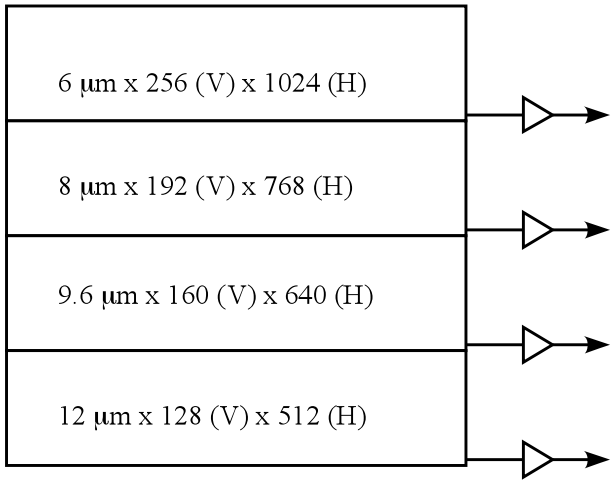


CCD Technology

- R&D is focused on fine pixel CCD sensors (FPCCD) and readout ASICs
- Goal:
  - Pixel size : 5μm× 5μm
  - Total # modules: 6080
  - 20,000×128 pixels/module → 10^{10} pixels
  - Full depleted, 15 μm thickness
  - Readout speed > 10Mpix/s
  - Readout noise < 50 e^- , Power < 100 W
- Currently produced: FPCCD #3
  - Pixel size: 12 – 6 μm
  - Sensitive thickness: 15 μm
- Tests being carried out:
  - Pixel size: 12μm×12μm
  - 4 frames with 512×128 pix/frame
- Status
  - Readout speed limited to 1.5Mpix/s

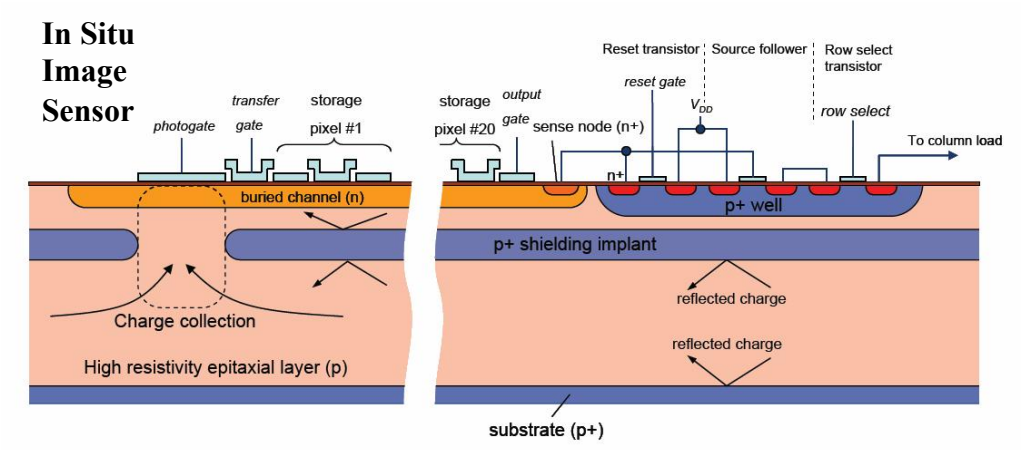


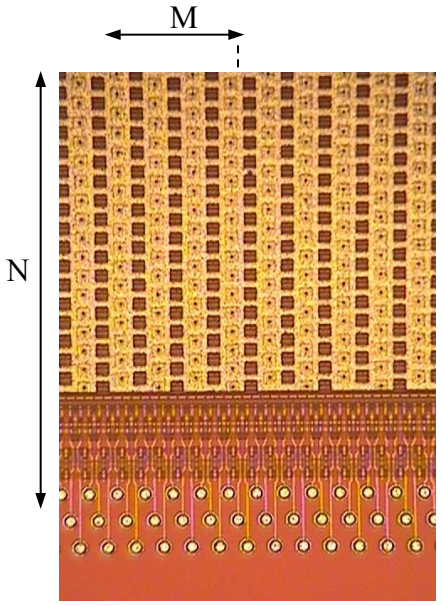




CCD Technology: UK

- The UK groups have led the R&D on CCDs for many years
- However, over the last three years all ILC-specific efforts were terminated.
- The ISIS and column-parallel CCD efforts are moribund.





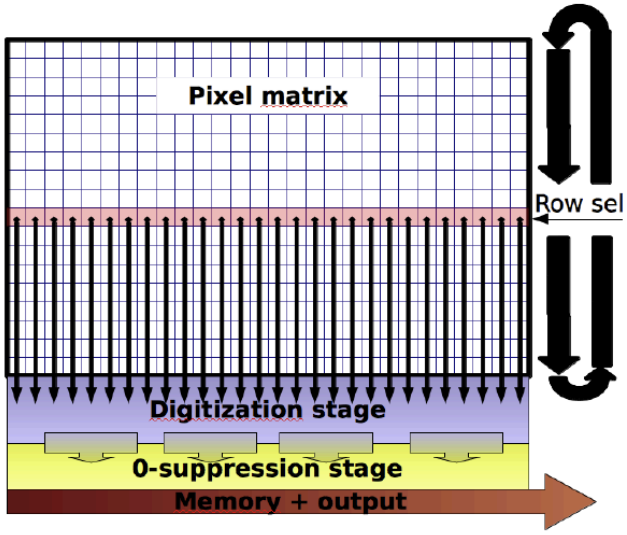
Column Parallel CCD
Readout time = N/f_{out}

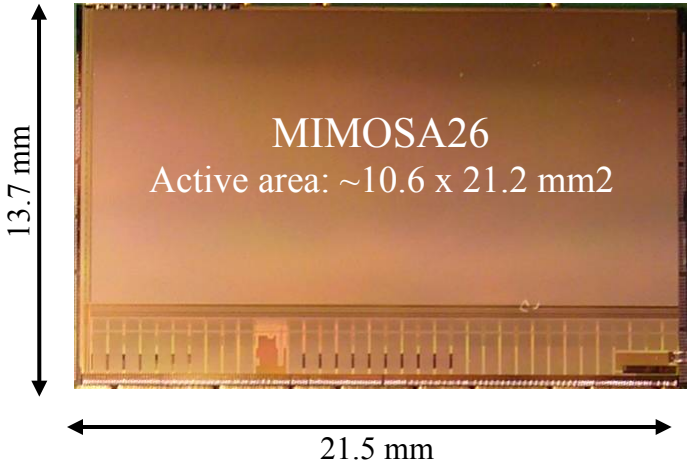
- Software:
  - Development of the vertexing software, LCFI, had become the effective standard in the ILC community.
  - Funding has stopped. Support transferred to Japan.

- R&D on low mass foam ladders is continuing and making progress.

CMOS

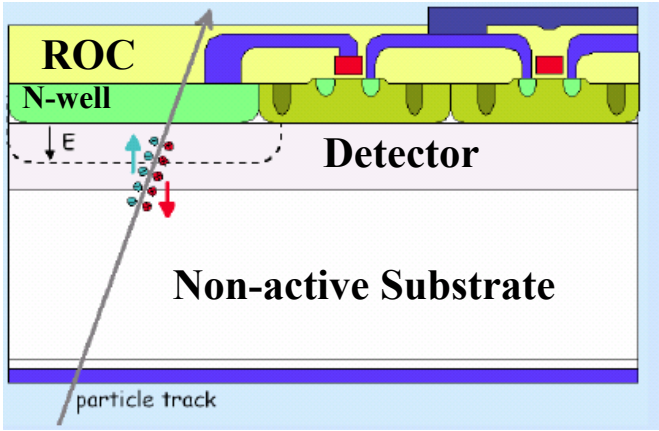
- **Strong Strasbourg group developing CMOS MAPS sensors**
- **Strategy for ILC (ILD)**
  - **Layer 1: spatial resolution**
    - Pixel pitch 16x16 μm^2, binary output
    - $\sigma \leq 3$ μm, integration time ≤ 50 μs
  - **Layer 2: time resolution**
    - Pixel pitch 16x64-80 μm^2, binary output
    - $\sigma \sim O(5)$ μm, integration time ≤ 10 μs
  - **Outer Layers: low power**
    - Pixel pitch 35x35 μm^2, 4-bits ADC output
    - 4 cm^2 of sensitive area
    - $\sigma \sim 4$ μm, integration time ≤ 100 μs
- **Proof of principle: Mimosa 26**
  - **Used in EUDET telescope**
  - **Pixel array: 1152 x 576, 18.4 µm pitch**
  - **10 k images/s**
  - **Also used in STAR VXD upgrade and for CBM MVD**

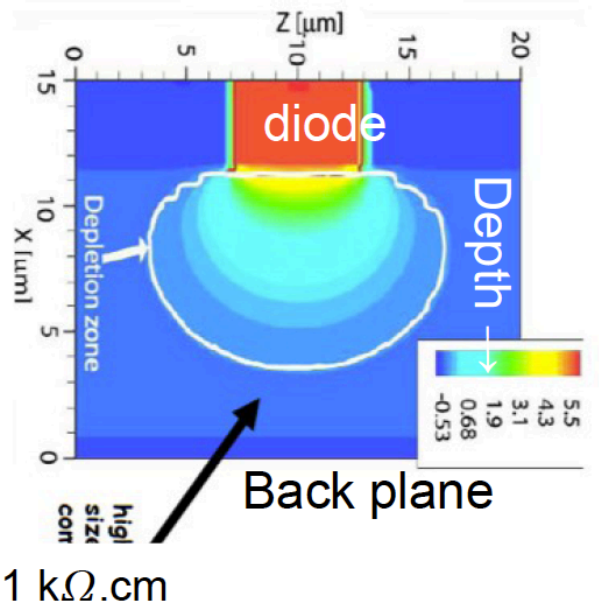




High Resistivity CMOS

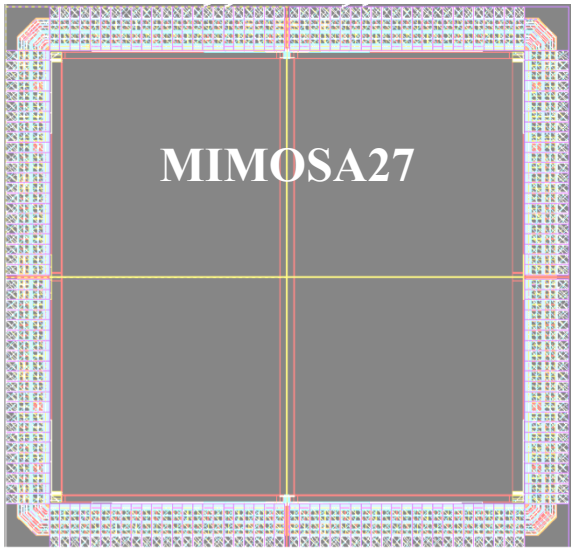
- **Standard CMOS**
  - Epitaxial layer, resistivity ~10 Ohm.cm
  - Charge collected through thermal diffusion
- **High Resistivity CMOS**
  - Low-doped epitaxial layer
  - Resitivity ≫100 Ohm.cm
  - Deeper depletion through diode voltage
  - Charge collected through drift: shorter and more spatially focused
  - More radiation hard
- **MIMOSA-26 HR**
  - 400 Ohm.cm epi layer: 10, 15, 20 mm thick
  - Exact same layout / MIMOSA 26
  - S/N is factor 1.5 to 2 improved compared to standard process with source tests



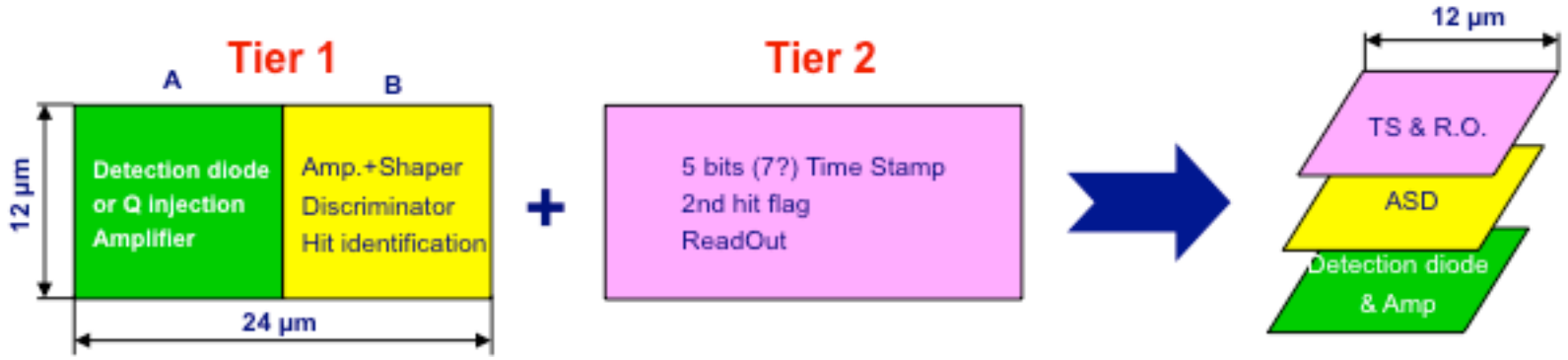


VDSM CMOS

- Exploring very deep sub-micron (VDSM) CMOS process
  - To date most Mimosa chips in AMS 350nm OPTO process
- MIMOSA27
  - 180 nm process (up to 6 metal layers)
  - 10 mm², 20 µm pitch, 4 sub-matrices of 64x64
  - In pixel amplification
- Designing large area telescope
  - Funded though AIDA project (FP7)

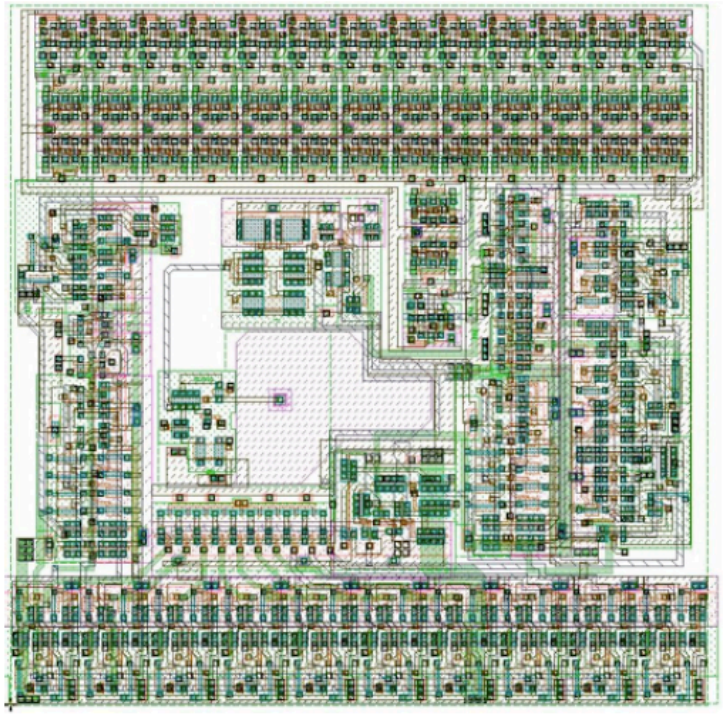


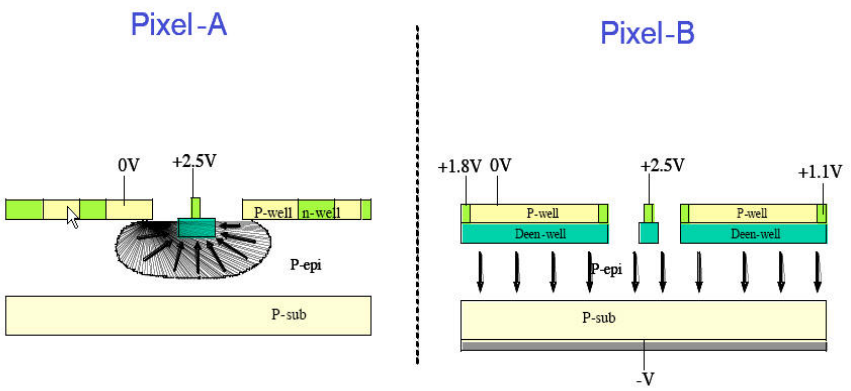
- Exploring planar 3D silicon technology
  - Participants in Fermilab 3D run
  - Porting design to 3 tiers



Chronopixel

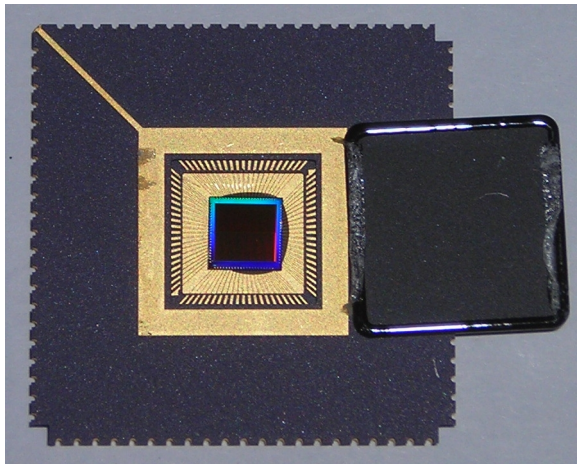
- SiD vertex detector has two baseline options
  - Chronopixel
  - 3D Silicon
- Chronopixel design provides for single bunch-crossing time stamping
  - When signal exceeds threshold, time stamp provided by 14 bit bus is recorded into pixel memory, and memory pointer is advanced
  - Comparator threshold adjusted for all pixels
- Current design
  - 50x50 μm^2 pixels
  - Two pixel architectures
    - Regular p/n-well design
    - Deep n-well design
  - Detector sensitivity: 10 μV/e
    - eq. to 16 fF
  - Detector noise: 25 e^-





Chronopixel

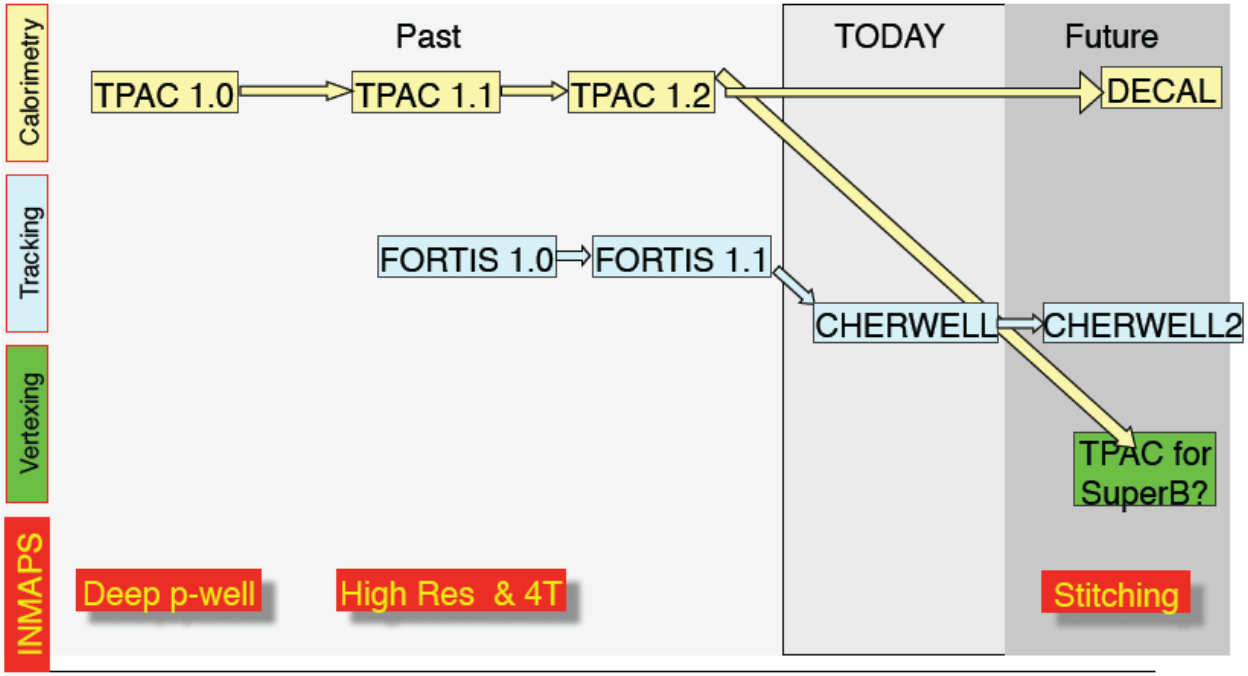
- Prototype pixels extensively tested by Nick Sinev
- Tests show that general concept is working
  - Good sensitivity ($\mu V/e^-$) as designed
  - Sensors timestamp maximum recording speed (7.27 MHz) is adequate
  - Noise figure with reset meets specifications
- Some issues with the chip
  - Faulty power distribution net on the chip
  - Calibration not fully functional
  - Comparator offsets spread across array too large



- Expect second prototypes by early next year and are ready to test them
- The approved funding is sufficient for the design and manufacturing of the second prototypes

SPIDER

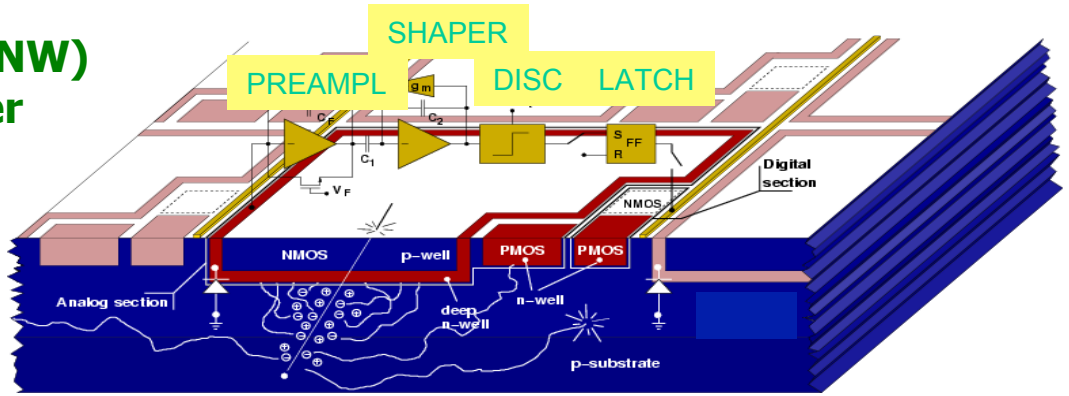
- **SPIDER: Silicon Pixel Detector R&D (UK based)**
- **Broad spectrum of applications for pixel detectors**



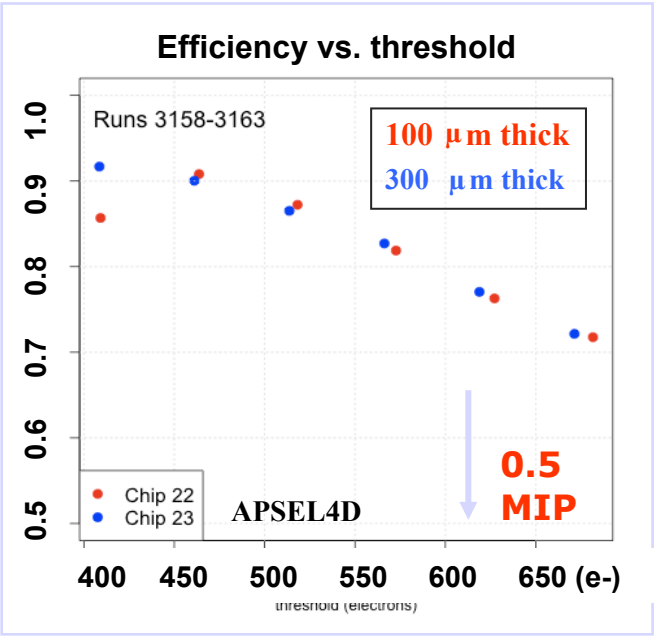
- **180 nm process, 6 metal layers**
- **5/12/18 µm high resistivity epitaxial layers**
- **Deep p-well to avoid parasitic charge collection**

MAPS

- **Strong INFN effort on developing MAPS pixel detectors for SuperB, ILC**
- **Uses Deep n-well (DNW)**
  - **The collecting electrode (DNW) is extended to obtain higher collected charge**
    - Reduce charge loss to competitive N-wells where PMOSFETs are located



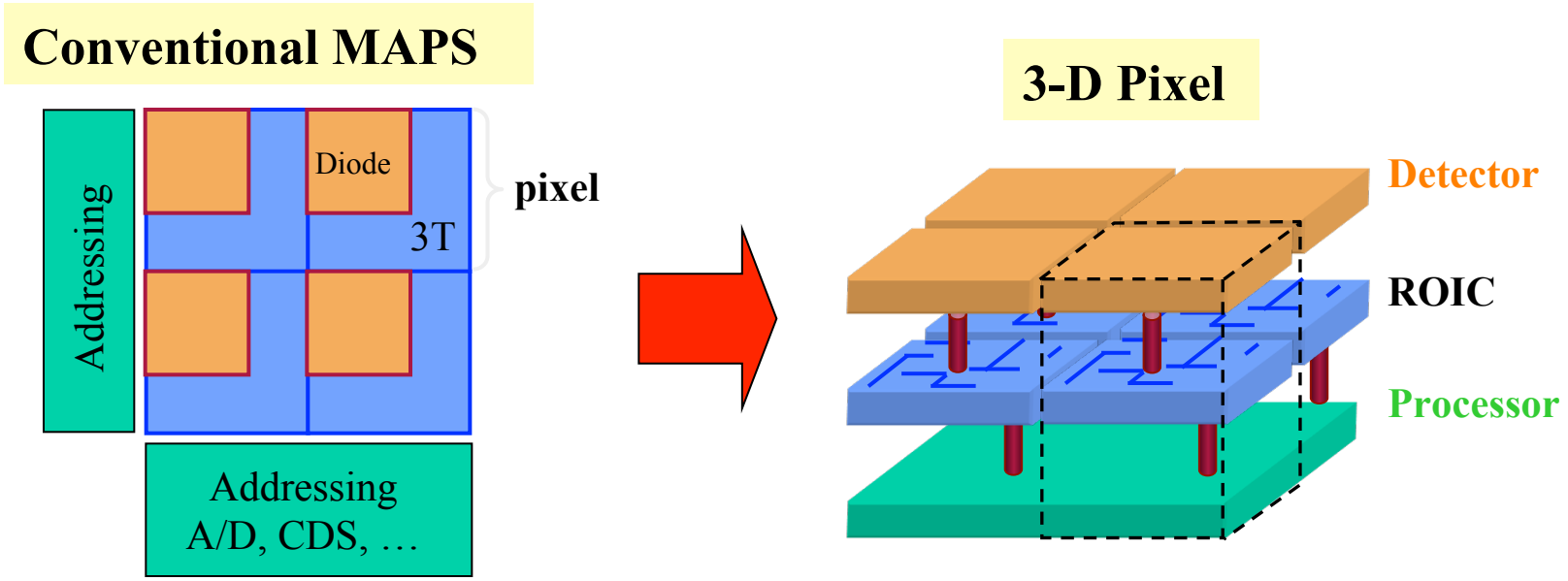
- **Many prototype matrices submitted: APSELn**
  - **APSEL4D: 4K(32x128) 50x50 µm2 matrix**
  - **Sparsified readout + timestamp**
  - **Pixel cell & matrix implemented with full custom design and layout**
- **Results**
  - **60 e- threshold dispersion**
  - **S/N = 23**
  - **Average gain = 860 mV/fC**



Vertical Integrated Circuits – 3D

- **Vertical integration of thinned and bonded silicon tiers with vertical interconnects between the IC layers**

- **Technology driven by industry; offers potential for transformational new detectors**

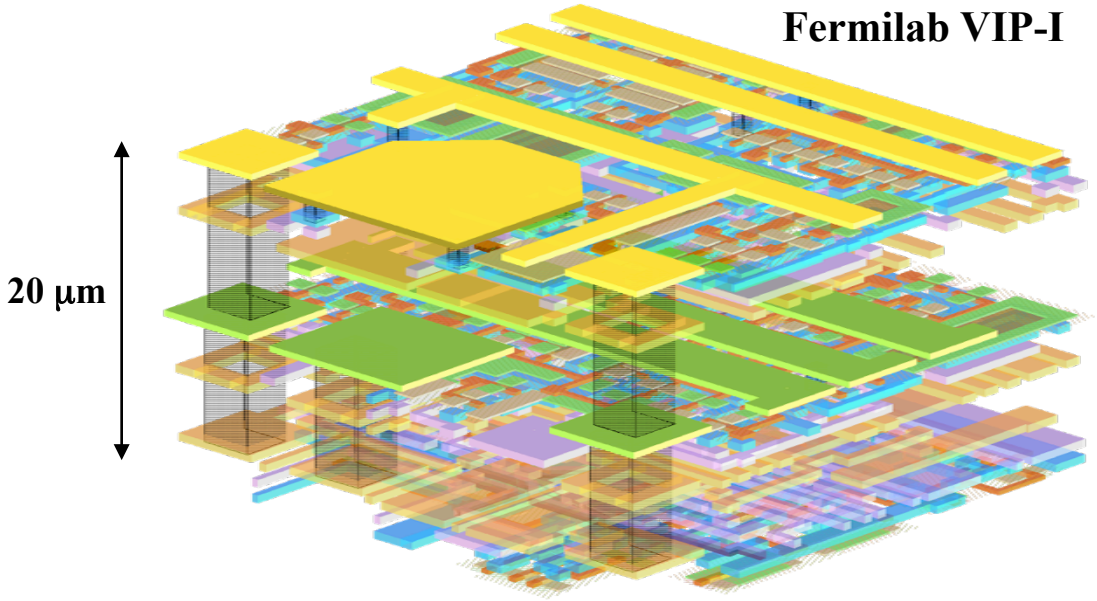


VIP Chip

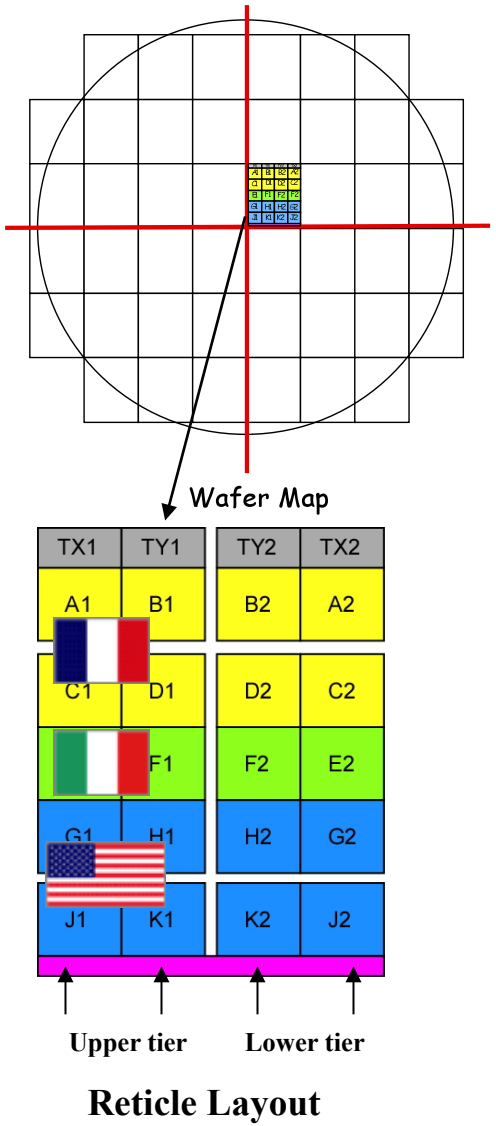
- Fermilab started to actively pursue the 3D technology, initially with MIT Lincoln Laboratories (MIT-LL), who had developed the technology that enables 3D integration
- MIT-LL offers DARPA funded 3-tier multi-project run, 180nm SOI process

- Designed Vertical Integrated Pixel (VIP) chip for ILC pixel detector
  - Pixel array 64x64, 20x20 μm^2 pixels; design for 1000 x 1000 array
  - Provides analog and binary readout information
  - 5-bit Time stamping of pixel hit
  - Token passing readout scheme
  - Sparse readout
- Chip divided into 3 tiers
  - ~ 7 μm / tier
  - 175 transistors / pixel
- No integrated sensor

- Chip works!



Fermilab 3D Multi-Project Run



Reticle Layout

- **Fermilab formed a 3D consortium and hosted a 3D multi project run with Tezzaron**
  - **Two layers of electronics fabricated in the Chartered 130 nm process, useful reticule size is 16x24 mm**
  - **Wafers will be bonded face to face**
  - **Submission closed September 2009**

- **17 Participating institutions in the MPW run**

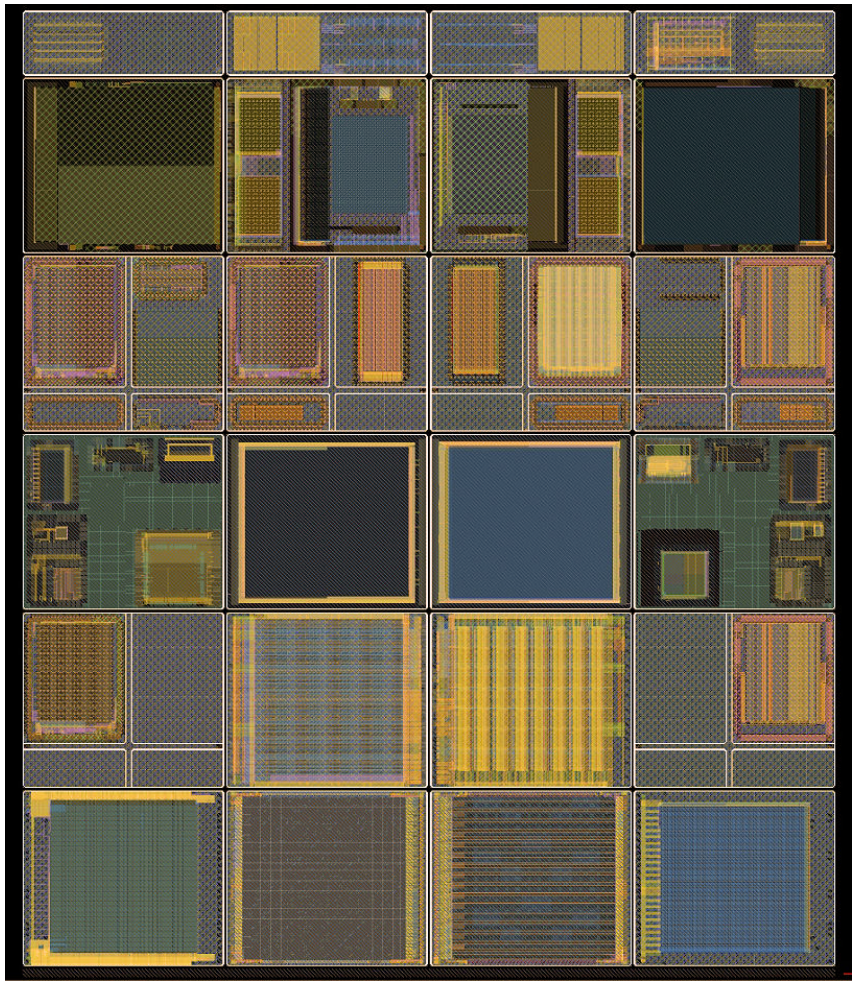
Fermilab, Batavia	CPPM, Marseilles	AGH University, Krakow
University at Bergamo	IPHC, Strasbourg	Brookhaven
University at Pavia	IRFU Saclay	LBNL
University at Perugia	LAL, Orsay	
INFN Bologna	LPNHE, Paris	
INFN at Pisa	CMP, Grenoble	
INFN at Rome	University of Bonn	

- **Frame divided into 12 sub-reticules for consortium members**

- **More than 25 two-tier designs (circuits and test devices)**

MPW Full Frame

Test chips:
TX, TY
2.0 x 6.3 mm



Notice
Symmetry
about vertical
center line

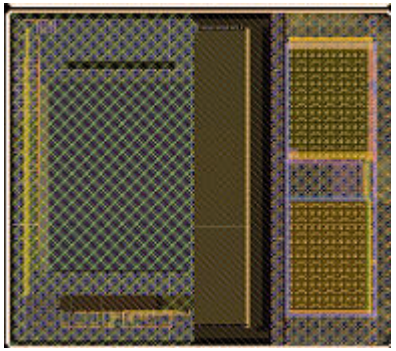
Subreticules:
A, B, C, D,
E, F, G, H, I, J
5.5 x 6.3 mm

Top tiers

Bottom Tiers

Sub-Reticules

- Sub-reticule A (Strasbourg, Saclay, Pavia) :
  - FE to be bonded to sensors from XFAB
- Sub-reticule B (CMP, Strasbourg, Saclay):
  - MAPS for ILC
- Sub-reticule C (CPPM, Bonn):
  - ATLAS 2D pixel design (FEI4)
- Sub-reticule D (CPPM, Bonn, LAL)
  - ATLAS 3D pixel design
- Sub-reticule E (Roma, Pavia, Bergamo, Pisa):
  - 3D MAPS
- Sub-reticule F (Pavia, Bergamo):
  - 3D MAPS
- Sub-reticule G Sub-reticule G (Orsay/LBNL)
  - ATLAS Pixel FE
- Sub-reticule H (FNAL/CPPM/LBNL):
  - Vertically Integrated CMS TRigger chip
- Sub-reticule I (FNAL):
  - VIP, adapted to two layers
- Sub-reticule J (FNAL/AGH-UST/BNL):
  - VIPIC: demonstrator for X-ray Photon Correlation Spectroscopy



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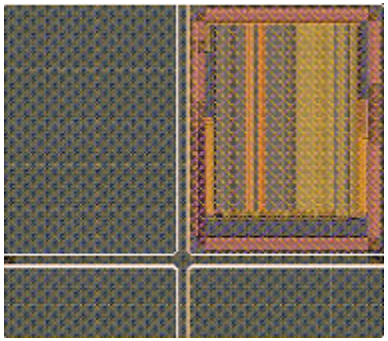


G Right

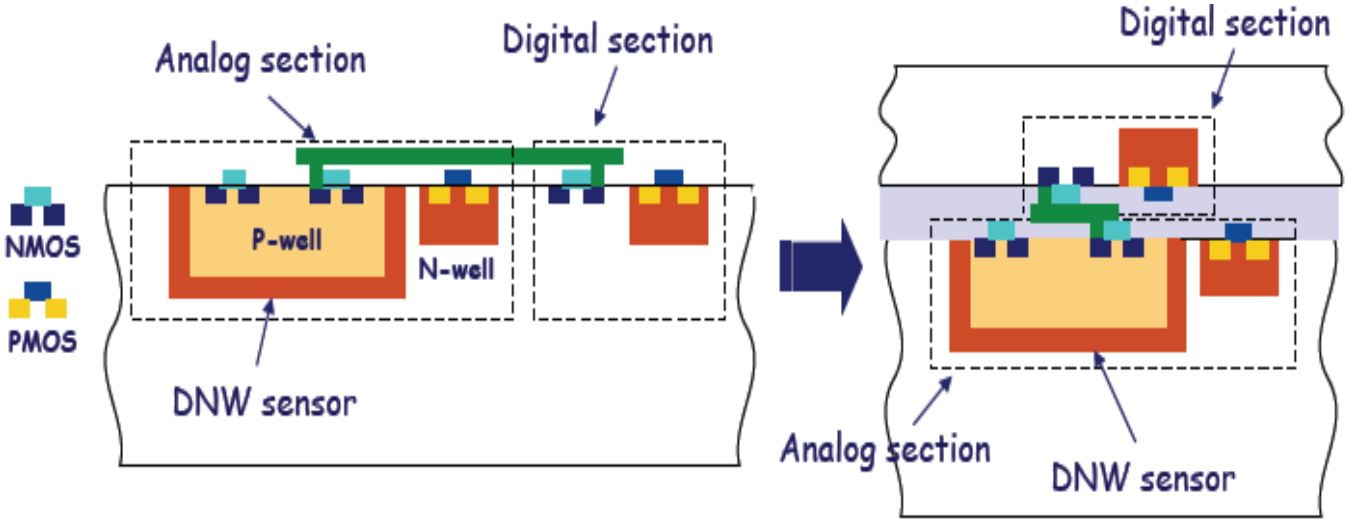
Timeline and Schedule

- All designs were received by Fermilab in May 2009
- June 2009 – March 2010 spent preparing and reviewing the submission(s)
  - Note, this was the first time for Fermilab and Tezzaron to organize a MPW run and there were a large number of 'growing pains'
  - A large number of problems were discovered
    - Frame and street definitions
    - Design kit incompatibilities, software bugs
    - TSV issues: protection, spacing, bond interface
- March 6, 2010: Fabrication started
- More problems:
  - Chartered stopped TSVs on 8 inch 0.13 CMOS wafers
  - Chartered agreed to process wafers from FEOL through M4
  - Tezzaron will add TSVs from M4 down into the substrate and complete the BEOL processing including the bond interface metallization
  - Space will need to be left open on M1-M4 for the vias to pass through.
  - Future potential benefit will be that wafers from other foundries can use the Tezzaron 3D process

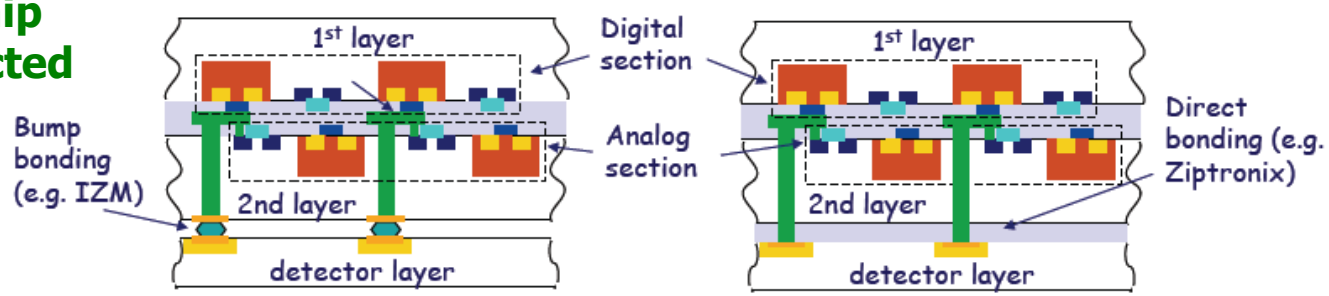
- 3D wafers should be available by the end of the year

MAPS in 3D

- **INFN has pilot project with Fermilab 3D Tezzaron project for 3D MAPS**

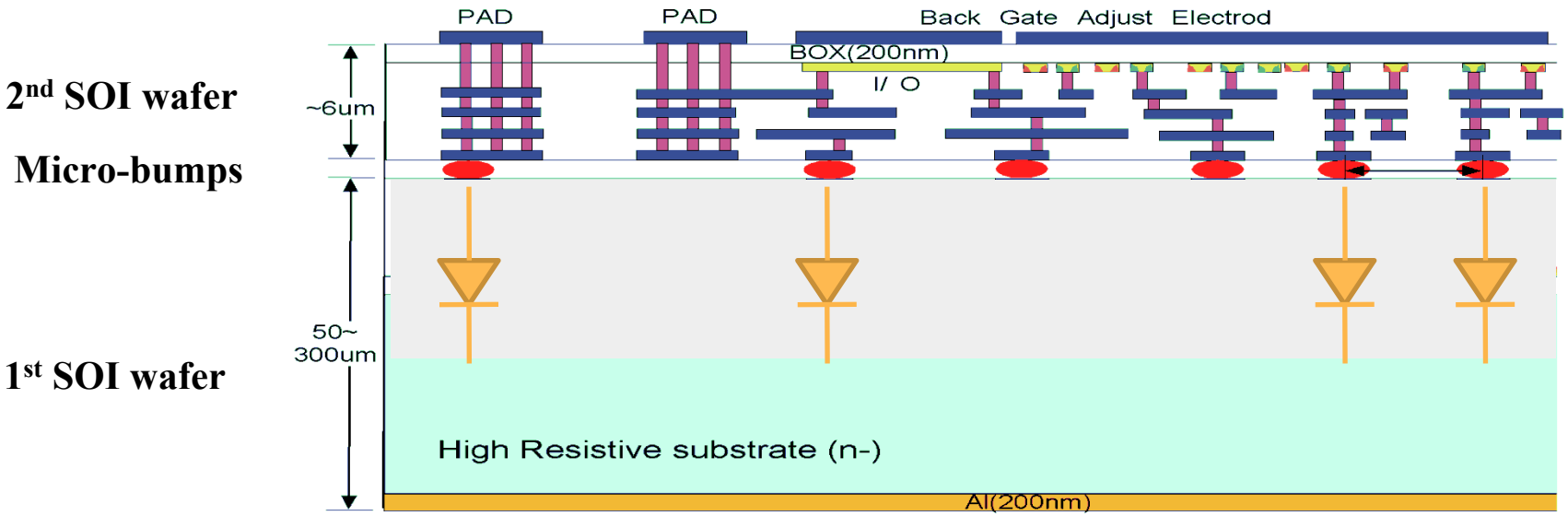


  - **Tier 1: sensor + analog FE + part of the discriminator**
  - **Tier 2: part of the discriminator, digital front-end and peripheral readout electronics**
- **Extend to CMOS FE integrated with high resistivity sensor**
  - **3D front-end chip (2 tiers) connected to HR sensor**



Silicon On Insulator

- **SOI is a 'natural' technology for integration of sensor and electronics**
  - **High resistivity substrate (sensor) isolated through buried oxide layer from front-end**
- **MAMBO III chip developed by Fermilab**
  - **Two tiers in KEK/OKI 200nm SOI process**
    - Tier one contains only diodes and shielding metal
    - Tier two contains front-end
    - Bonding through micro-bumps at T-Micro (formerly Zycube)



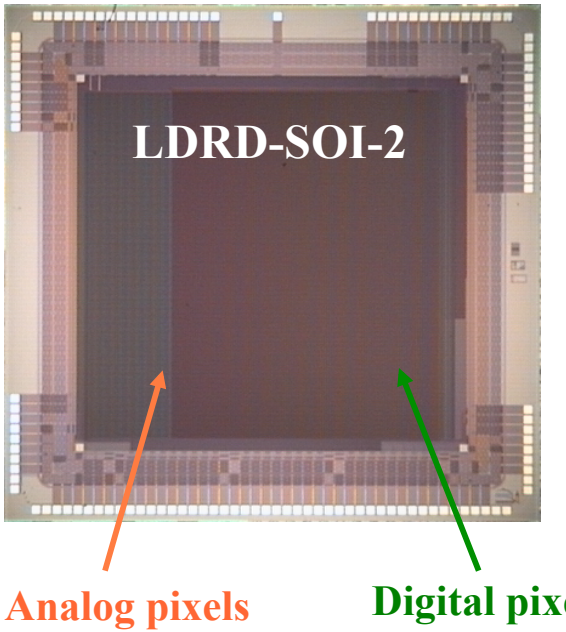
SOI

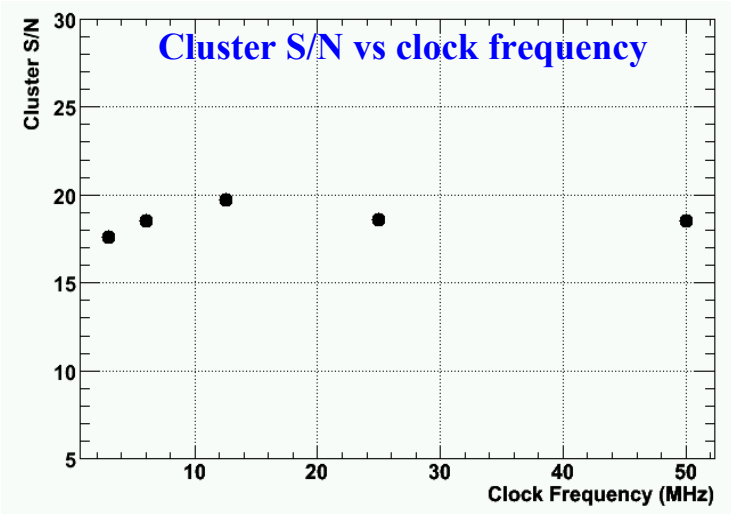
- LBNL studying SOI process for pixel detectors and imagers

- Technology
  - OKI 0.20 μm FD-SOI process
  - Prototype 5×5 mm², 20×20 μm² pixels
  - 1.8 V operational voltage
  - 40×172 analog pixels with 3T architecture

- Results
  - Up to 50 MHz readout
  - S/N ~ 17-20 at 50 MHz pixel clock (138 μs integration time)

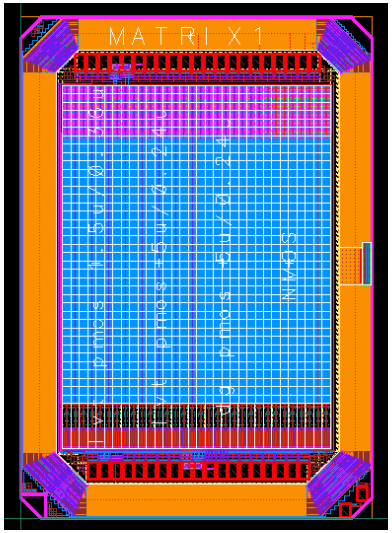
- All SOI processes suffer from "backgate effect", shift in thresholds





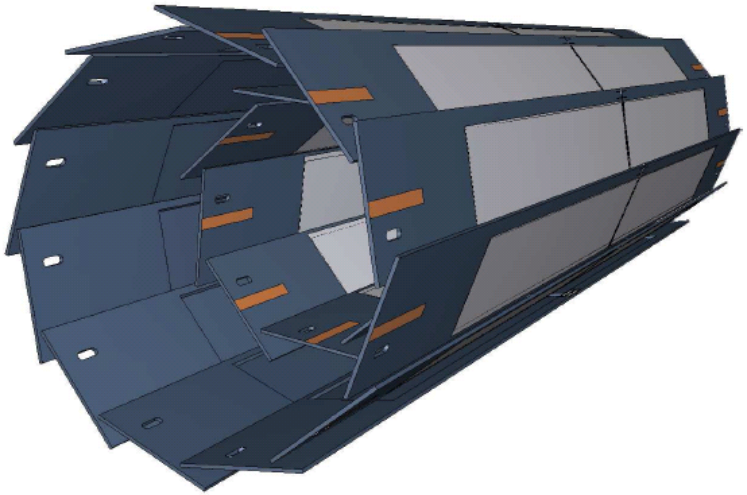
LePIX

- LePIX: monolithic detectors in advanced CMOS
  - Collaboration between CERN, IReS in Strasbourg, INFN, C4i-MIND in Archamps and interest from Imperial College, UC Santa Cruz, Rutherford
  - Group is not focused on ILC detectors per se
- MAPS:
  - Non-standard processing on very high resistivity substrate, with serial readout not always compatible with future colliders, and with collection by diffusion very much affected by radiation damage
- LePIX:
  - Develop monolithic pixel detectors integrating readout and detecting elements by porting standard 90 nm CMOS to wafers with moderate resistivity.
  - Reverse bias of up to 100 V to collect signal by drift
- Advantages:
  - Good radiation hardness (charge collection by drift)
  - High speed, time tagging at the 25ns level
  - Low power: 20 mW/cm^2 in continuous operation
  - Low cost
- Status
  - Submitted a few test stuctures

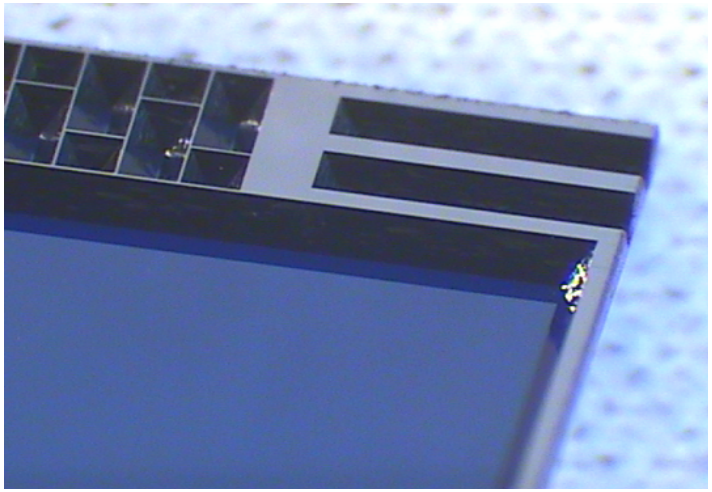


The State of the Art: DEPFET

- The R&D carried out in the framework of the ILC has led to the development of the DEPFET technology to reach a level of maturity that is now the technology for the BELLE-II vertex detector
  - Two layers at radius of 14 and 22mm
  - Pixel size 50x50 and 50x75 μm^2
  - Sensor thickness 75 μm
  - System of 8M pixels



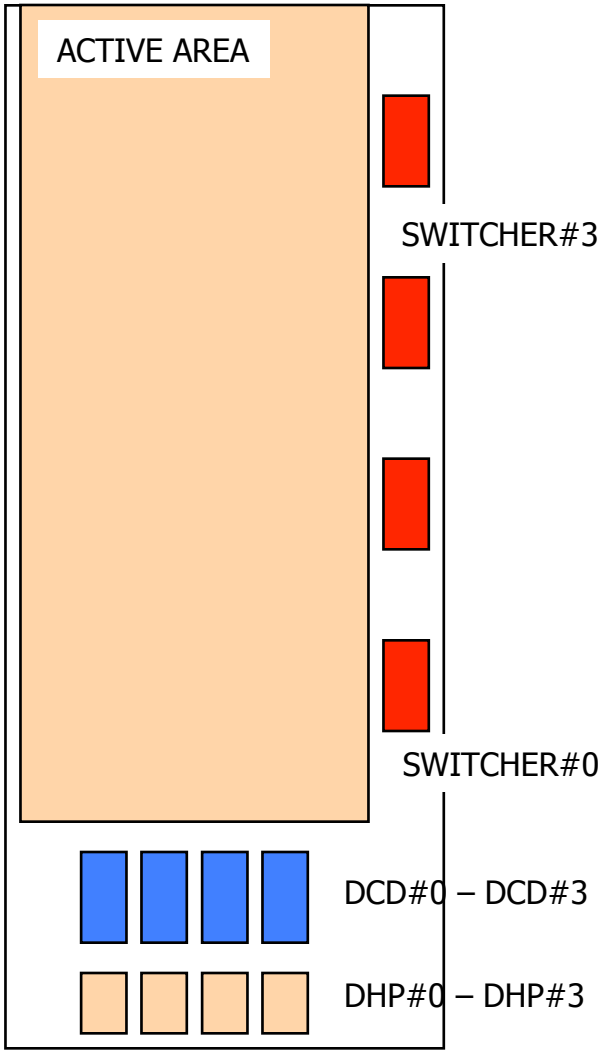
- Sensors fabricated by MPI, HLL
  - 400 μm sensors
  - Anisotropic deep etching to open window; frame provides all support
  - Etching to provide connection to other sensor at z=0



- Readout
  - Detector is always live
  - Rolling shutter readout with frame rate of 20 μs

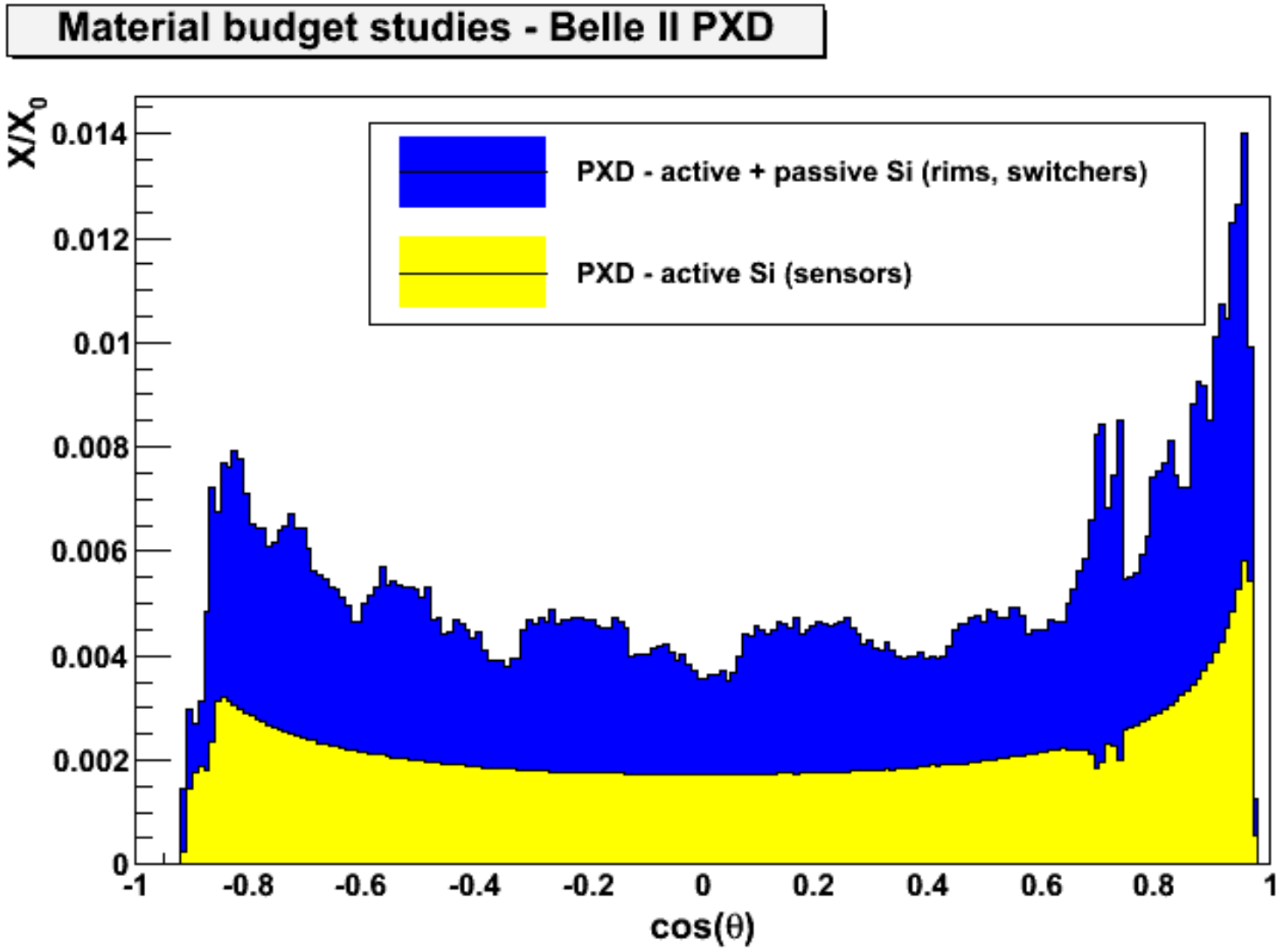
DEPFET Readout

- Three ASICs used to readout sensor
- All ASICs mounted directly on active Si sensor
  - Need to provide under bump metallization for bump bonding
- Switcher
  - Activates DEPFET transistor gates to initiate row readout and activate clear gates for the reset
- Drain Current Digitizer (DCD)
  - Drain currents are amplified and digitized
- Data Handling Processor (DHP)
  - Digital signal processing
    - Common mode subtraction
    - pedestal subtraction
    - zero-suppression
  - Controls and synchronization of the switcher and DCD
  - DAQ and trigger communication



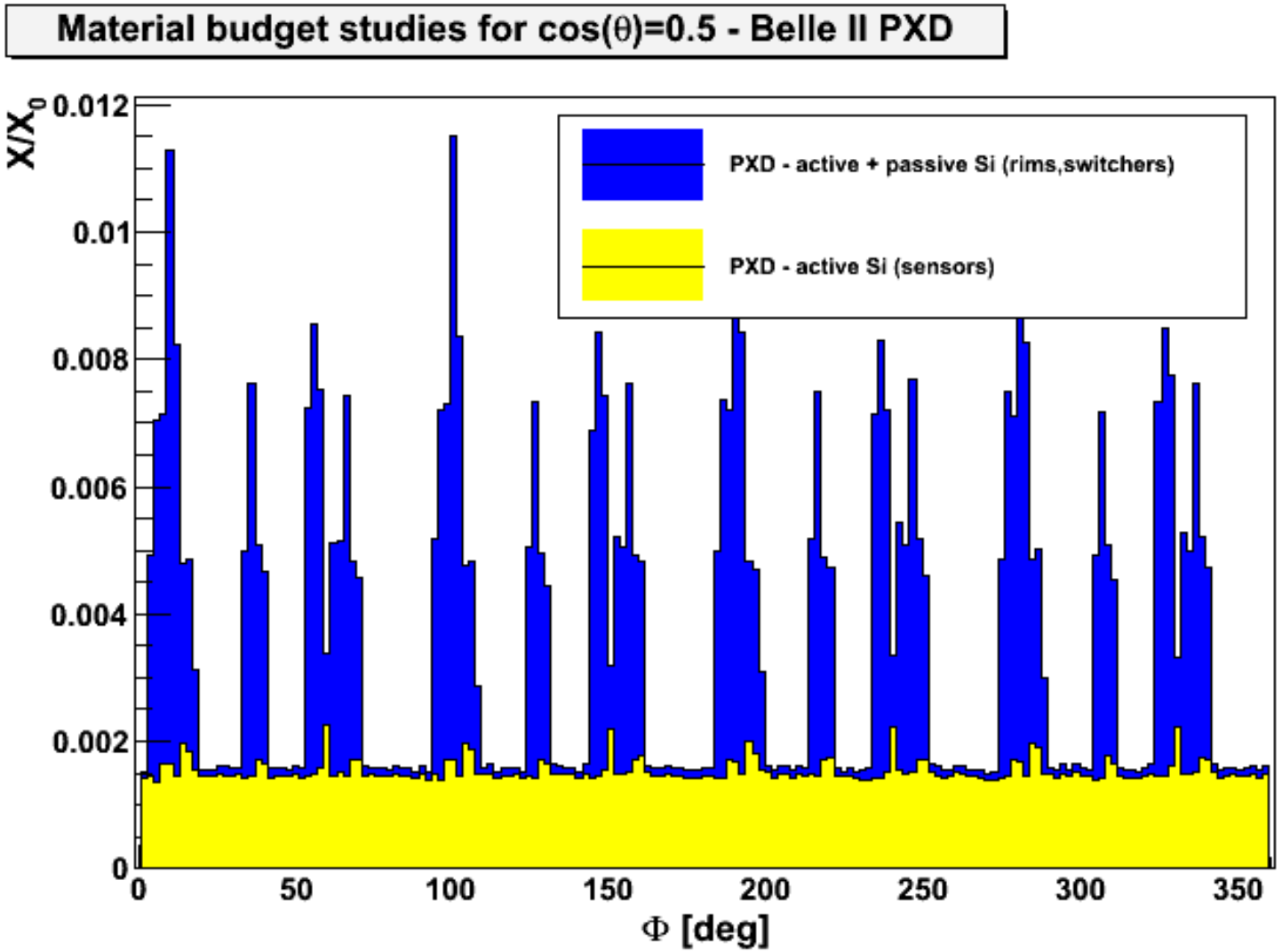
BELLE-II PXD: Material Budget

- **Impressive overall material management (recall goal: 0.1% X_0 per layer)**



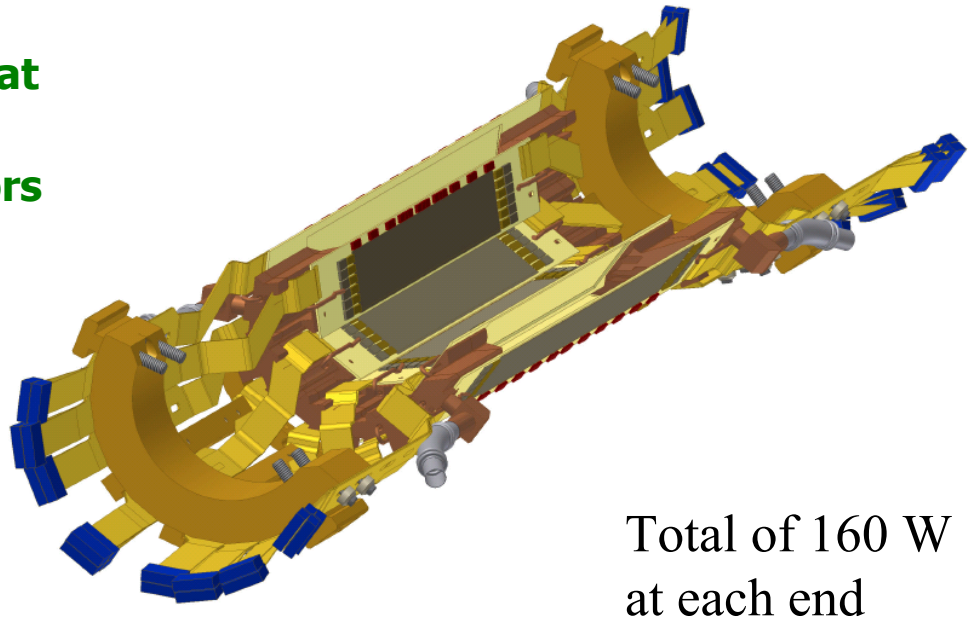
BELLE-II PXD: Material Budget

- **Azimuthal dependence of material budget**

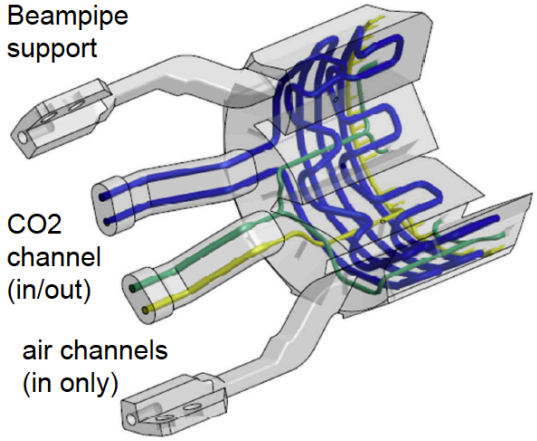


BELLE-II PXD: Cooling

- **Power consumption**
  - **Four DCD and four DHP ASICs at total power of ~7W**
  - **Four Switcher chips plus sensors at total power of ~1W**
  - **Layer 1: 8 ladders**
  - **Layer 2: 12 ladders**
- **Total power ~ 160 W per end**
  - **DEPFET technology is a very low power option**
- **Active CO_2 cooling at each end of the ladder**
- **Air flow cooling for Switcher chips**

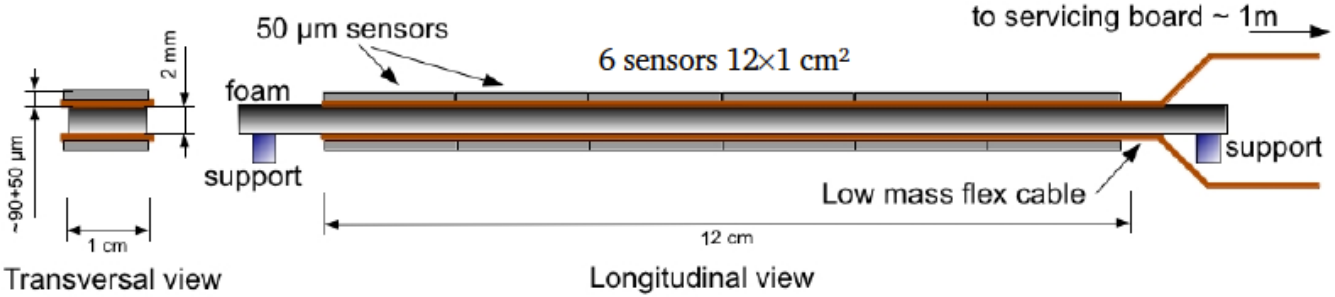


Total of 160 W at each end

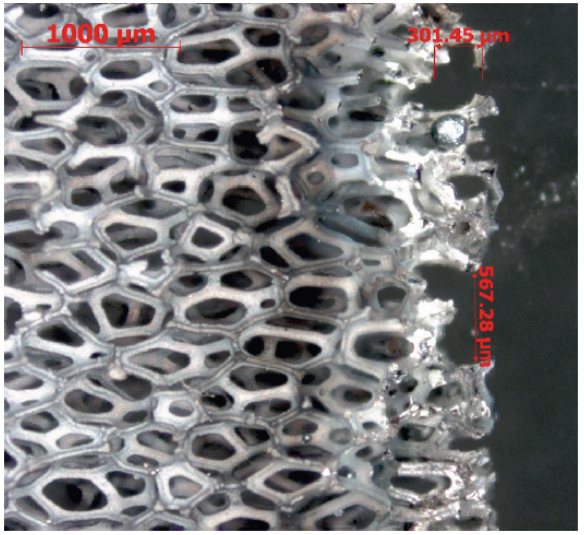


Support: PLUME

- **PLUME: Pixelated Ladder with Ultralow Material Embedding**
  - **Collaboration of Bristol, Oxford, DESY, IPHC**
- **Goal:**
  - **Achieve a double-sided ladder prototype for a vertex detector by 2012**
  - **material budget : ≤ 0.3% X_0**



- **Concept:**
  - **Six MIMOSA-26 sensors**
  - **Kapton flex cable**
  - **Silicon carbide foam (8% density), 2mm thick**
  - **Power pulsing (≤ 200ms period, ~1/50 duty cycle)**
  - **Power dissipation (100mW/cm²)**
  - **Air cooling**



Support: Serwiette

- **SERWIETE: SEnsor Raw Wrapped In an Extra-Thin Envelope**
  - **Collaboration with IK-Frankfurt, GSI/Darmstadt and IMEC**
- **Goal:**
  - **Sensor assembly mounted on flex and wrapped in polyimide film**
  - **Material budget <0.15 % X_0 for 1 unsupported layer**
  - **Evaluate the possibility of mounting supportless ladder on cylindrical surfaces**

Thickness budget :

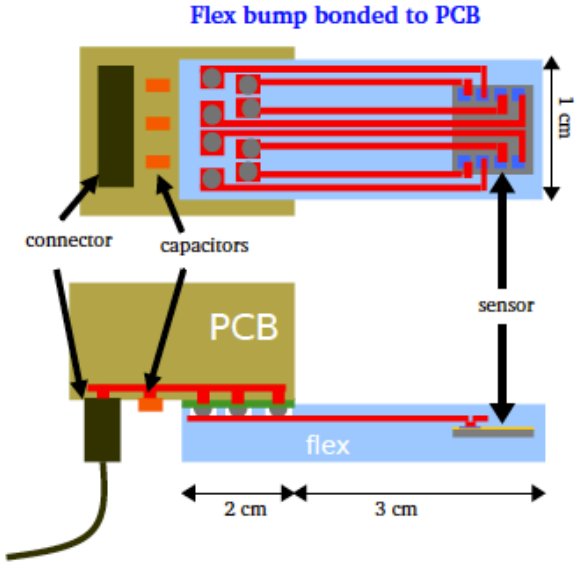
6.5 µm backend (metal and oxide on chip)
= 6.5 µm Si equivalent

20-25 µm Si (14 µm epitaxial layer)
= 20-25 µm Si equivalent

Sensor thinned down to 30 µm

2× 20 µm polyimide + Solder mask (25 µm)
= 22 µm Si equivalent

Total = 48.5 – 53.5 µm Si equivalent



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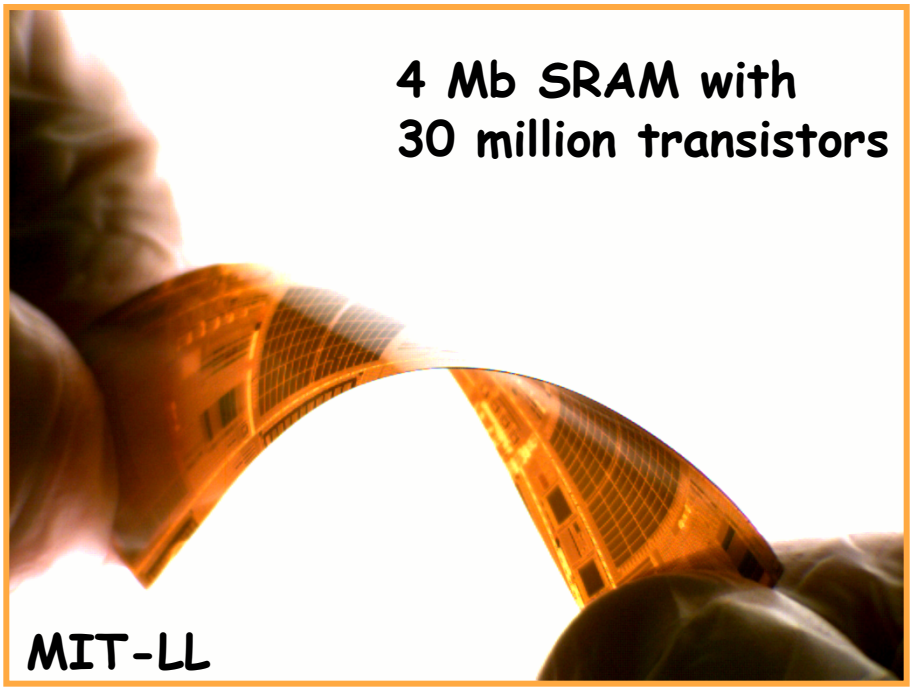

Observations

- **Many pixel technologies being pursued. Despite the major setbacks in the UK, it is a very healthy area of R&D**
- **It is an understatement to say that it is an enormous challenge to design and construct pixel detectors that meet the ILC specifications**
- **The technology, however, is becoming available to really build transformational detectors**
- **There seems to be a tendency for the pixel detectors to move towards generic pixel detector development which, I think, is beneficial to the community**
- **And, apologies to all efforts not mentioned**