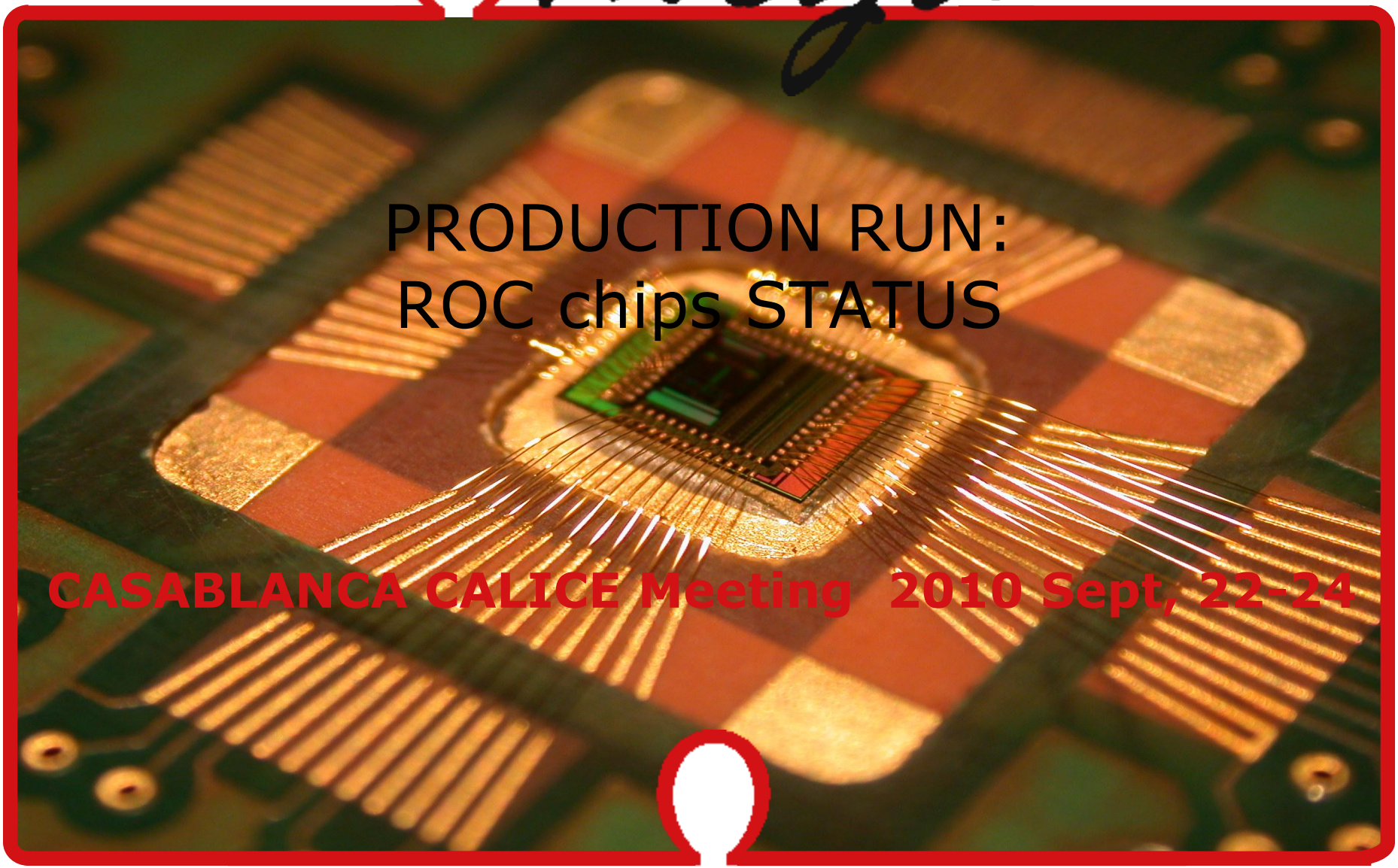
IN2P3

Omega



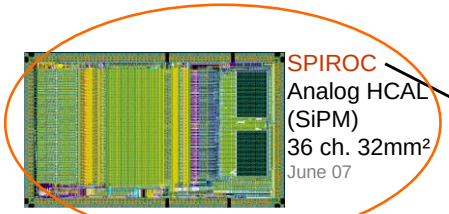
PRODUCTION RUN:
ROC chips STATUS

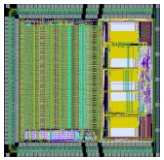
CASABLANCA CALICE Meeting 2010 Sept, 22-24

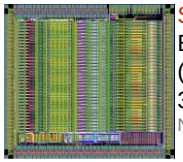
Orsay MicroElectronic Group Associated

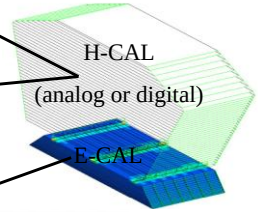
Production run

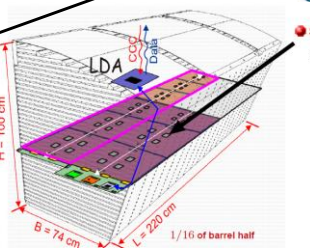
- **Production run launched in March 10**
- **Reticle size : 18x25 mm²**
  - 50-55 reticles/Wafer
  - 25 wafers needed
- **Final arrangement:**
  - **« Calice » chips produced:**
    - **7 Hardroc 2b** => ~9000 chips
    - **1 Spiroc 2a** => ~1200 chips
    - **1 Spiroc 2b** => ~1200 chips
    - **1 Skiroc 2** => ~1200 chips
  - **Additionnal chips produced:**
    - 1 Spaciroc : JEM EUSO experiement
    - 1 Maroc 3 : for PMT readout
    - 3 Spiroc 0 (SPIROC « light » version)
    - => **cost reduction** for CALICE


SPIROC
Analog HCAL
(SiPM)
36 ch. 32mm²
June 07


HARDROC
Digital HCAL
(RPC, µmegas or GEMs)
64 ch. 16mm²
Sept 06


SKIROC
ECAL
(Si PIN diode)
36 ch. 20mm²
Nov 06





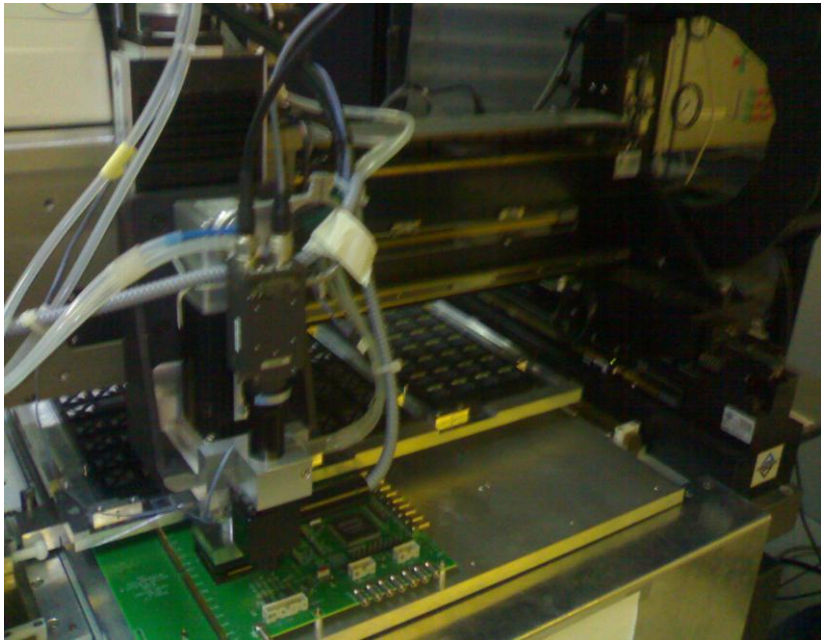
SPIROC chip:
handles signal from 36 SiPM

Packaged chips

- Received from AMS at the end of June and sent directly to I2A Technology (Fremont, USA) for packaging
- Thinning of the wafers down to 250µm
- dicing
- Packaged chips and bare dies received at the end of August
  - HR2b: **10 510** packaged in TQFP160 + **~ 1 000** bare dies
  - SPIROC2A: **973** in TQFP 208, **661** bare dies
  - SPIROC2B: **195** in TQFP208, **1 469** bare dies
  - SKIROC2: **1 671** bare dies (5 to be packaged in a QFP 240 ceramic package)

HARDROC2B: first tests

- ~9000 chips to be tested with a dedicated testbench in IPNL Lyon



- ~300 chips tested right now with a yield of 80% (See Luigi's talk)

SPIROC2A: first tests

973 in TQFP 208, 661 bare dies

- Slight pinout modification: requires only firmware modifications
- Slow Control fixed, probes are still problematic
- POD module for the 2 clock LVDS receivers
- a OR36 output on an unused pin of spiroc2: OK
- Power consumption of the low gain preamplifier decreased
- The backup SCA is OFF when unused to save power

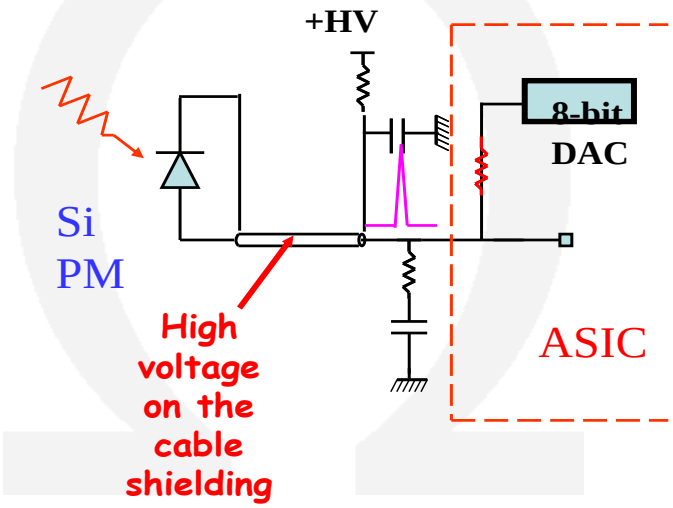
SPIROC2B: first tests

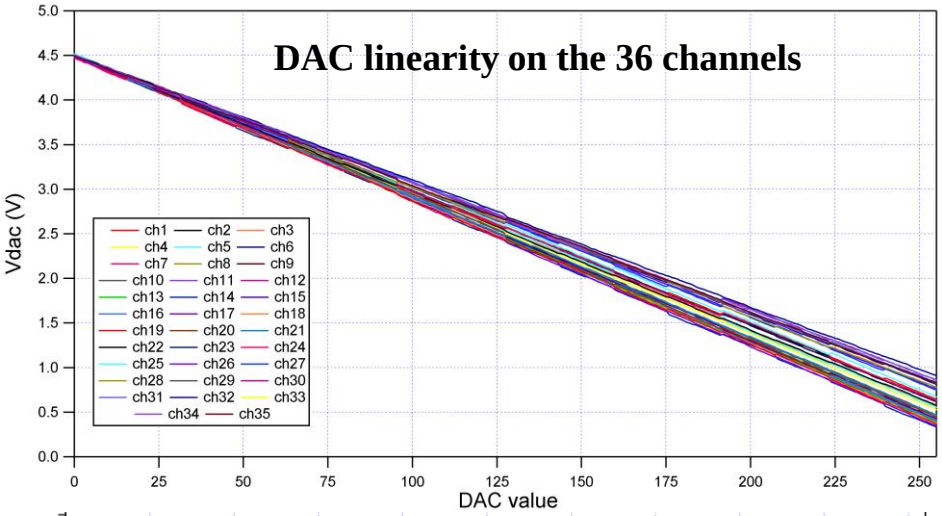
195 in TQFP208, 1 469 bare dies

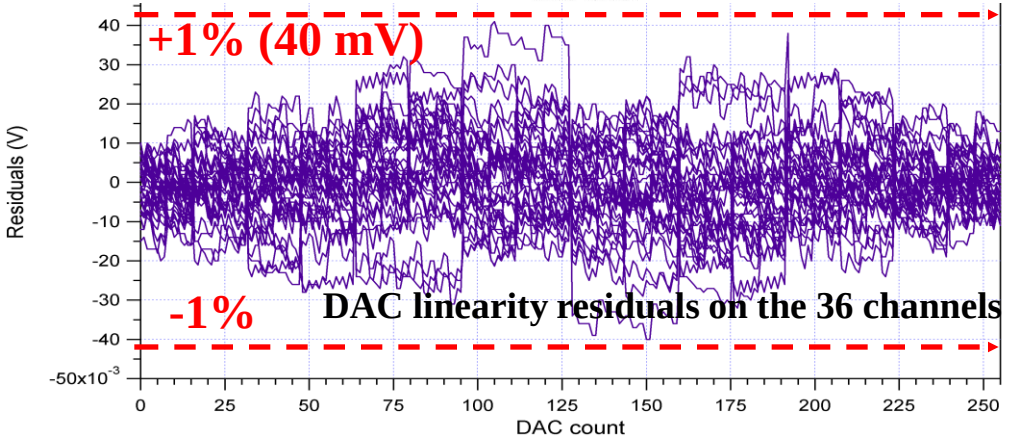
- Pinout modification: requires f/w modification and also h/w modif to use the LVDS external trigger.
- LVDS input for external trigger: “pw_on_sca” and “pw_on_dac” pins merged to free a pin for LVDS trig_ext signal
- Individual gain adjustment: 6-bit Preamplifier gain adjustment per channel (25fF, 50fF, 100fF, 200fF, 400fF, 800fF)
- The first “zero-frame”: active pull-up to reference voltage on ADC discri input. Necessity to decrease Vref_ramp_ADC
- Better input 8-bit DAC and 10-bit DAC

SPIROC2B: new Input DAC

- Input DAC to optimize SiPM bias voltage
- 8-bit DAC, 5V range, LSB=20mV
- 36 DAC (one per channel)
- Ultra low power (<1µW) : no power pulsing
- Can sink 10 µA leakage current
- Improved version : new spatial arrangement for a better matching
- Linearity : ± 1%
- DAC uniformity between the 36 channels : ~3%



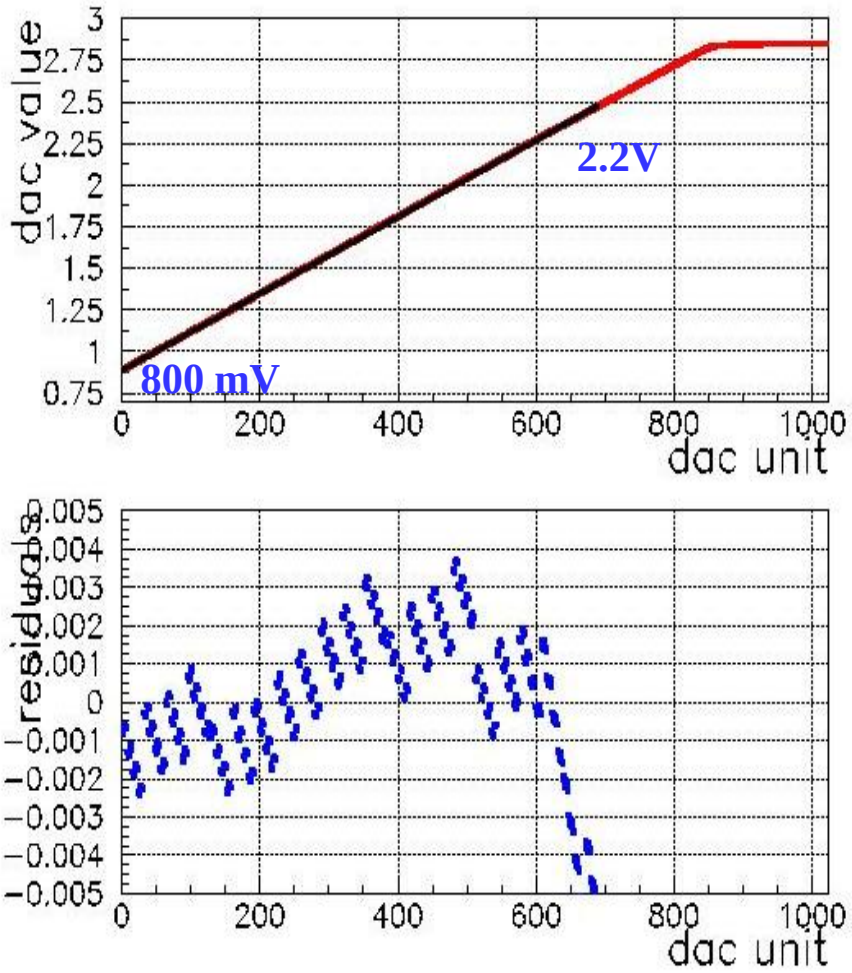




SPIROC2B: new 10-bit DAC linearity

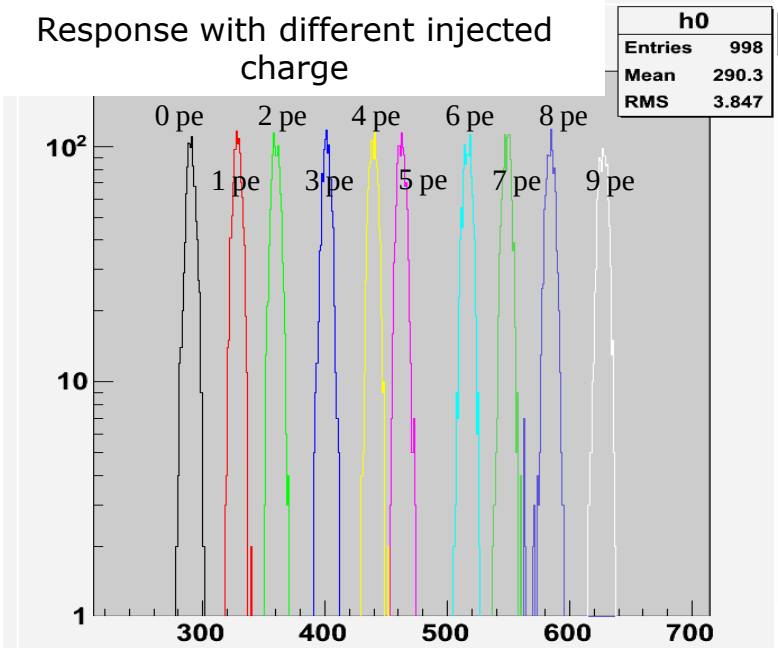
- PRELIMINARY MEASUREMENT:
  - Residuals : **±2mV** (±1 LSB or ±2%) up to DAC=600
  - Slope 2.3mV/DAC unit

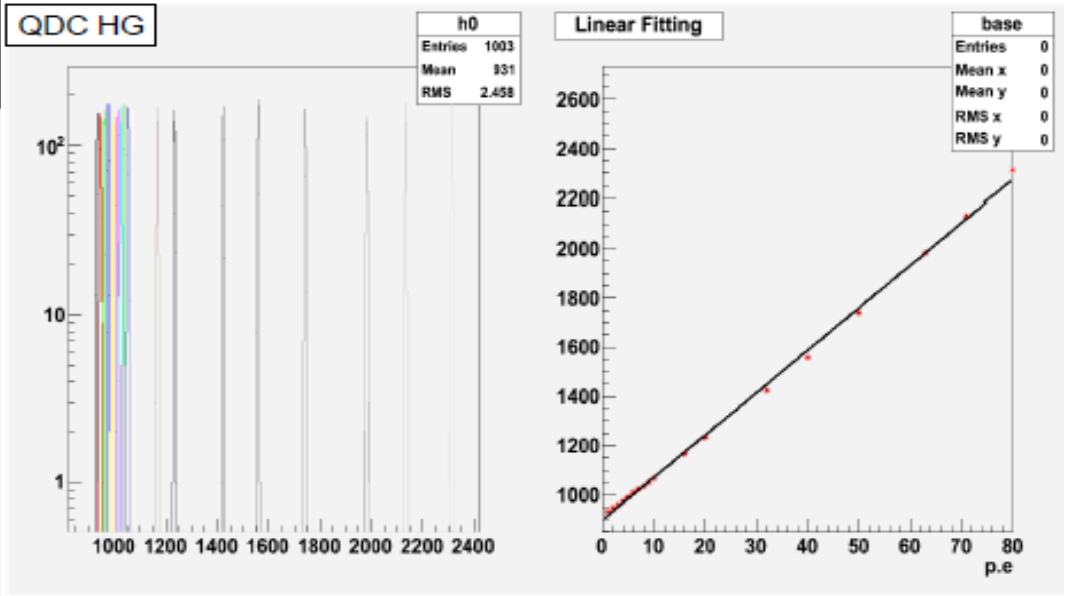
  => Measurement to be redone with a slope decreased down to 2mV/DACU



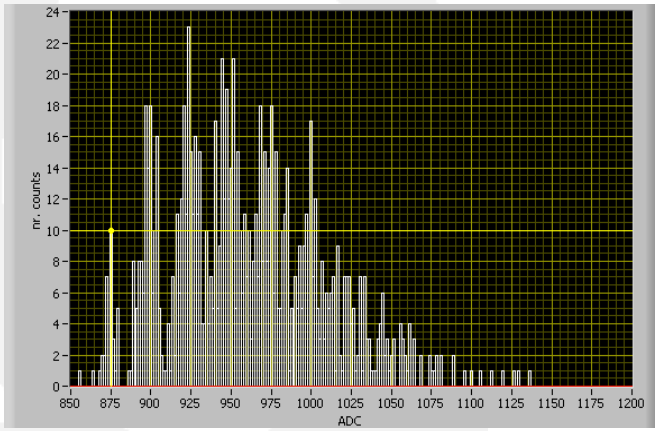
Single photoelectron spectrum in ORSAY

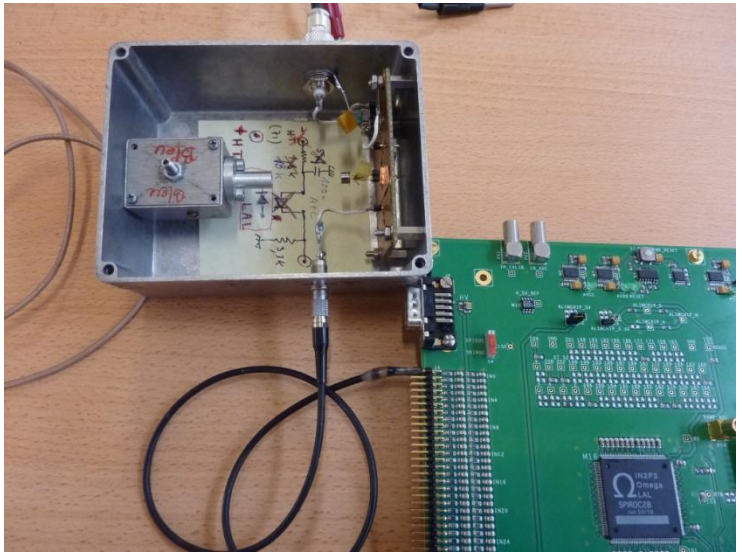
Response with different injected charge



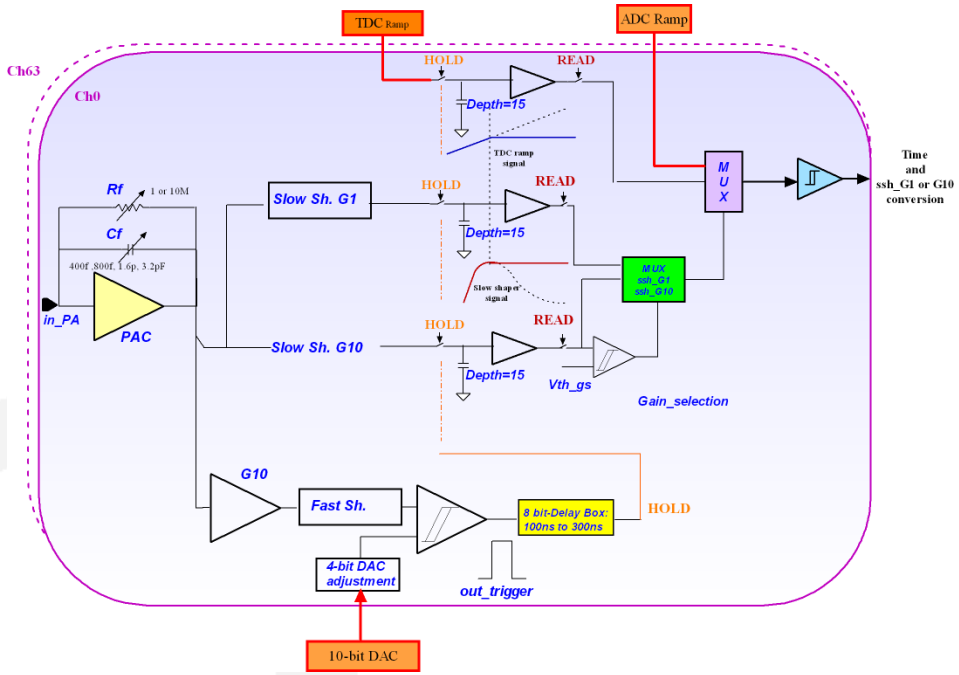


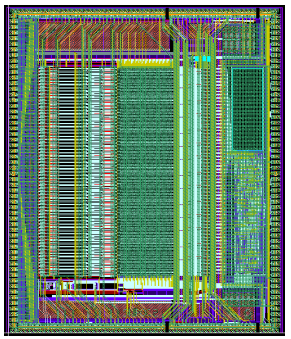
Setup: Autotrigger mode and internal ADC





- 1670 bare dies, 5 chips packaged in a 240 ceramic QFP package to be tested on a dedicated testboard (available)





SKIROC2
ECAL Si
64 ch. 70 mm^2

- Software and Labview: to be written
- Will be mounted on FEV8 once FEV7 tested

Conclusions

- ROC chips produced: packaged and bare dies
- 9000 HR2B to equip the DHCAL 1m^3
- Large quantity of SPIROC2A, 2B and SKIROC2

=> A lot of work to test and characterise these chips