Comments on the DAQv2 advancement

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Calice Week
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HW status

- 10 ECAL DIF ready and working; 10 in prod; mat for 40 in total (CAM)
- DHCAL DIF: 165/170 cards tested & ready (LAPP)
- AHCAL DIF: in design, prod in NIU → 4 unit
- CCC: 10 cards ready; 4 in use in 4 labs; 3 more shipped → LLR
- DCC: 3 prototypes ready; 2 cards being tested → 20 end of october
- LDA: 20 main board OK
  - 5 v1 + 15 v2 Ethernet mezzanine : ✔
  - 6 CCC mezzanine; clock OK — Busy & Trigger not yet tested (TBC)
  - 20 HDMI Mezzanine: faulty connectors on 8 → in repair
- ODR + PC
  - 8 ODR ready ; network card being used instead for debugging
  - 6 PC available: 1 in LLR ; 3 other ready; OS needs to be upgraded
- BIF: to be developped (part of AIDA)

~ No more basic problem with HW
Reliability of HDMI connectors mechanics ?

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FW status

LDA+CCC comm (M.Warren)

Reuse MUX from DCC (FG)

	LDA	DCC	DIF's
Ethernet	✔ at full speed		
CCC	Clk; Trig; Busy	Clk; Trig; Busy	Clk; Trig; Busy
Nlinks up	7/10 conn. no MUX	9	1
Fast Commands	✔	✔	✔
Block transfert	✔	✔	✔
Data[1)]	✔ (< 50 MHz)	✔ (< 50 MHz)	✔ (<50 MHz)
ROC			Structure ✔ Adapt SDHCAL USB Code on going...

Simple but critical

- FW have been advancing rather fast during the last months
  - effort on going (⊃ in UK) → MW, MW & BH at LLR on 28th of July
  - G.V. → integration of ROC management in DIF started but needs finalisation

Many progresses recently
End of October for first full minimal usable chain ?

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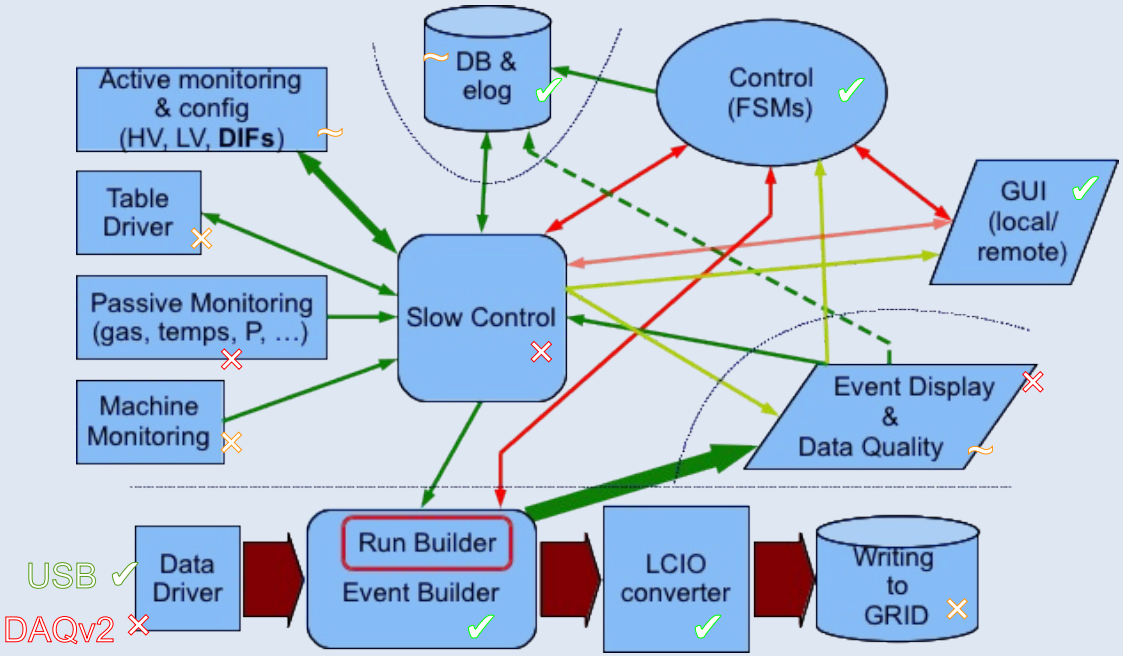
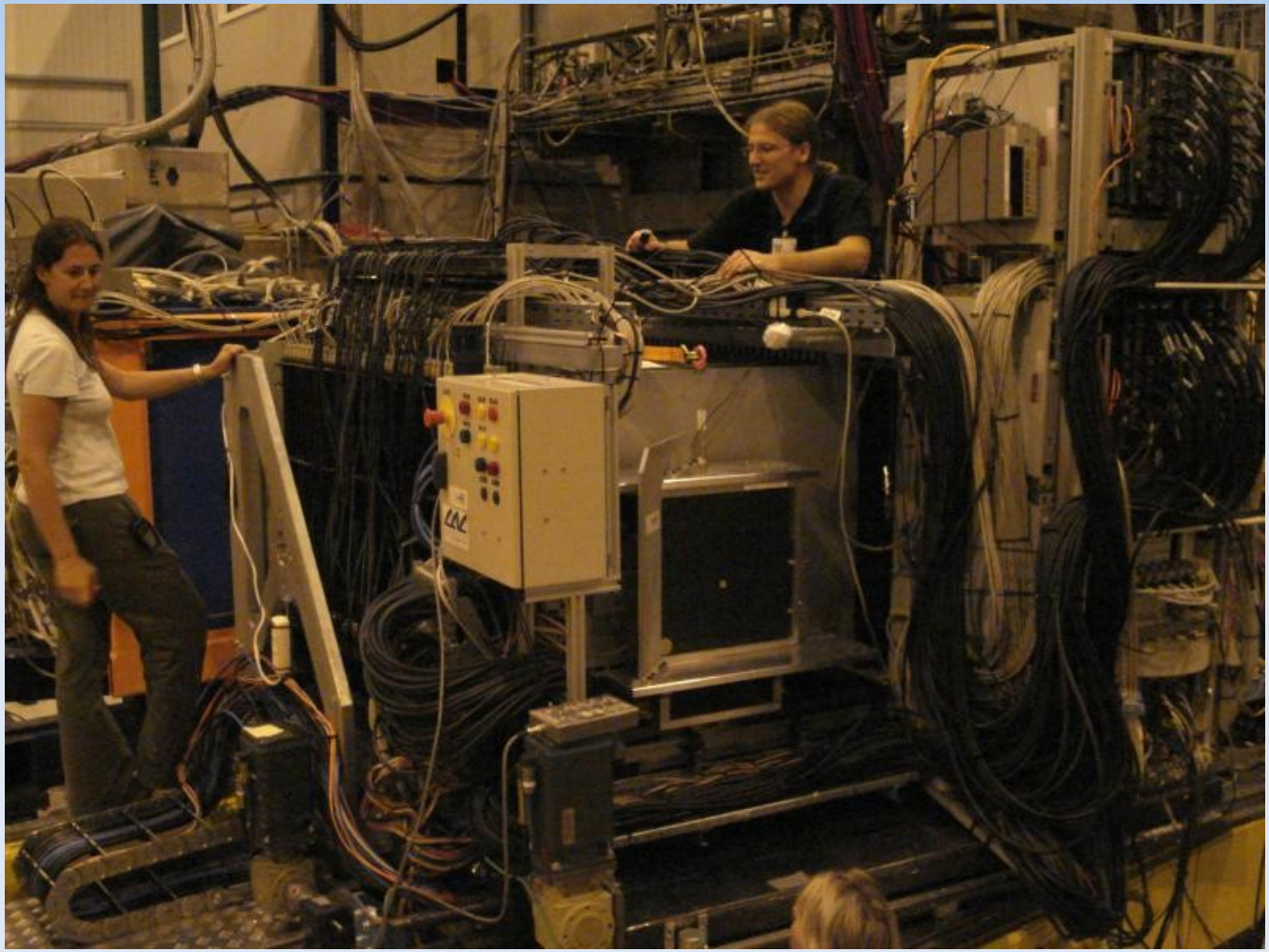
SW status

- Many progress
  - XDAQ (L. Mirabito, Ch. Combaret) “critical part“ complete:
    - Writing of LCIO data in RAW format
    - versatile online analysis framework (root histos)
  - DAQ2 interface ←→ XDAQ being worked on (D. Decotigny, G. Vouters)
- Missing utilities
  - Semi-automatic noisy channels spotting & correcting (moniting) ←←←
  - Clean Slow control
  - interface to CondDB;
  - event display (most probly DRUID)
  - interface to the GRID
  - interface to the machine
- Analysis environment (IPNL)
  - rec. data format in LCIO



Installation

- mechanics
  - mod. VME crate for
    - DCC
    - CCC
  - Special box for LDA
  - Support for cables
- Final set-up not yet known:
  - stand alone SDHCAL
  - stand alone ECAL
  - Stand alone AHCAL
  - Combined test
- → 5 m long HDMI cables
  - halogen free;



Plans

1) Critical: Complete the FW → full acquisition chain & check perfs (stability)
    1) Trigger logics → M. Warren
    2) LDA MUX → F. Gastaldi
    3) Finish adaptation of USB FW → DAQv2 FW → G. Vouters
        1) Adapt SDHCAL DIF FW → ECAL DIF & AHCAL DIF
2) Complete the SW critical part
    1) Integration of DAQv2 in XDAQ → D. Decotigny
3) Continue development SW of utilities
    1) Define optimal PC configuration: Stand alone SDHCAL → Combined tests
    2) Writing to GRID; interface to beam → L. Mirabito, Ch. Combaret
4) Prepare the set-ups
    1) SDHCAL m^3 TB
    2) Electronics & Cosmic ECAL test bench in LLR
    3) µMegas, ECAL & AHCAL TB (to be defined): brute perf to be ×-checked