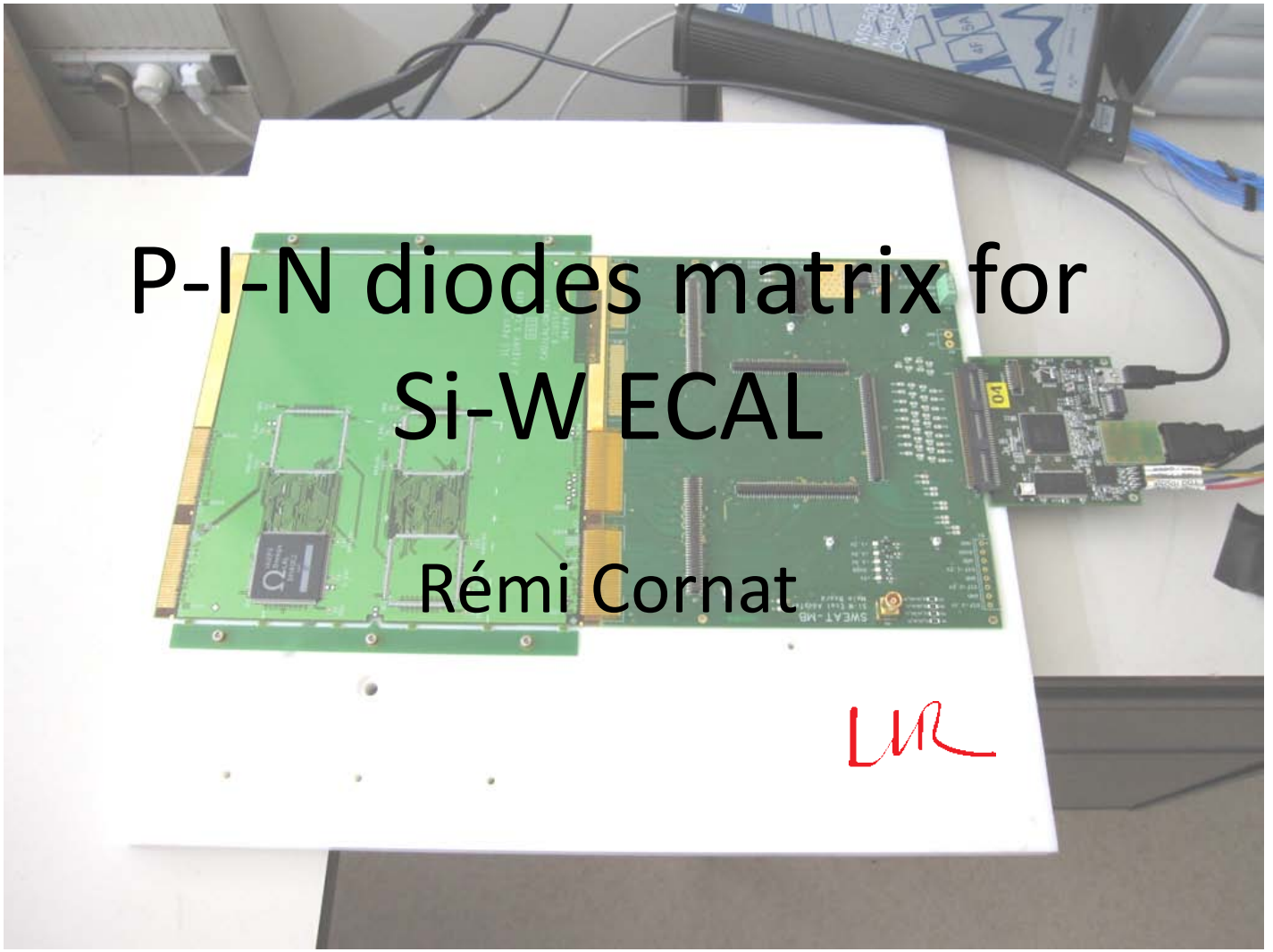
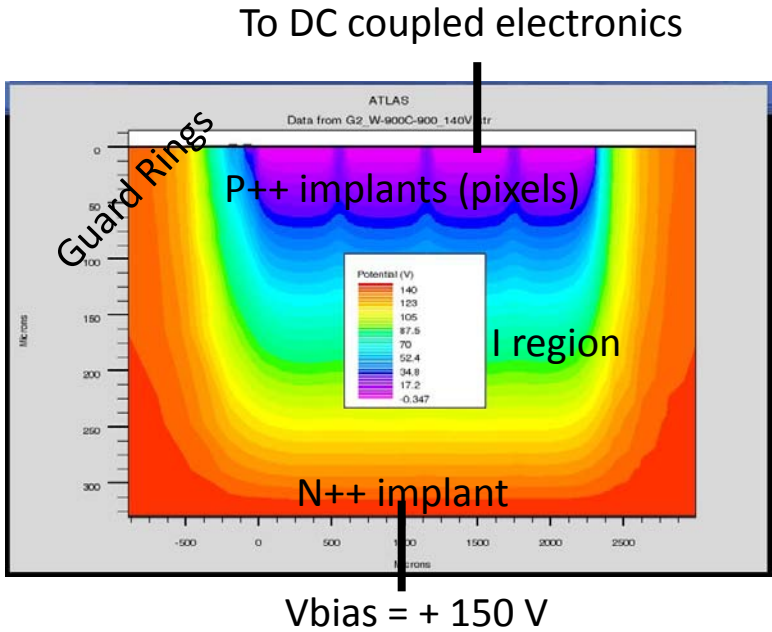


P-I-N diodes matrix for Si-W ECAL

Rémi Cornat

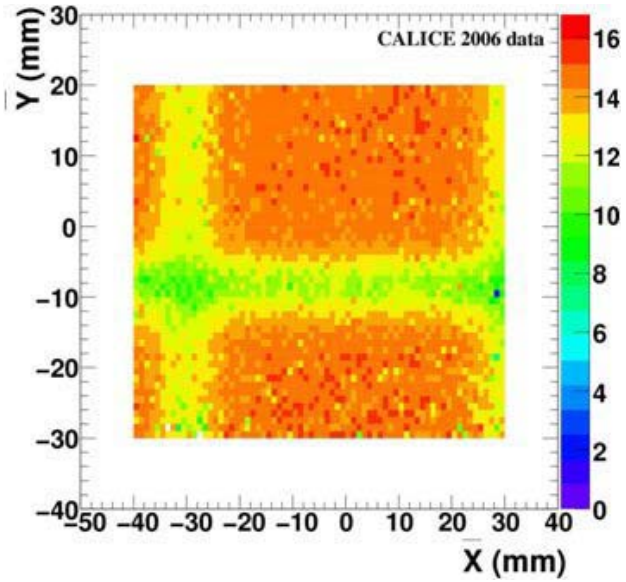
Sensor Design

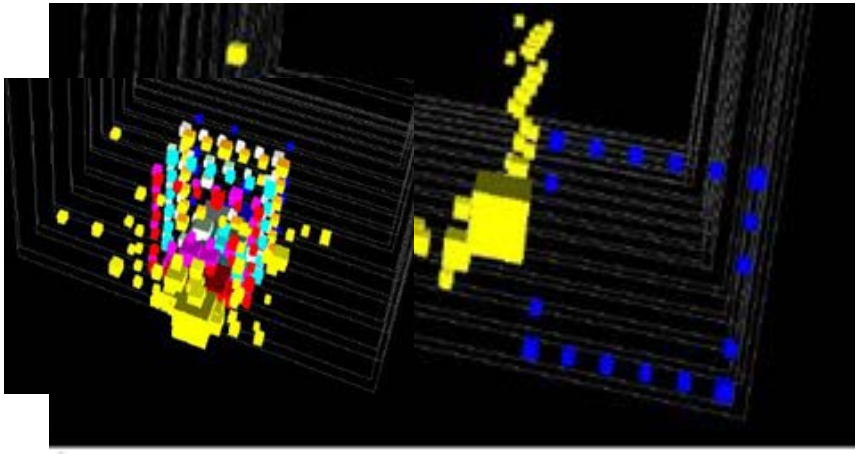
- Glued on PCB
- <u>Guard rings are not biased</u>
- Possibility to wire bond the GR
- New versions should optimize
  - Width of the dead zone at the edges
  - Crosstalk level between GR & pixels (Square Events)
- In touch with HPK France (J.-C. Lefort)
  - 70 k€ (including NRE) for 40 pcs of this prototype = 22 € / cm2 (14 € w/o NRE)
- Assumption that the simplest design allow to control the cost
  - Few thousands of m² needed for ILD
  - Up to 400 000 matrices
  - Financial viability would be insured for costs of about a few € /cm²



9x9 cm², 324 or 256 pixels

2 effects





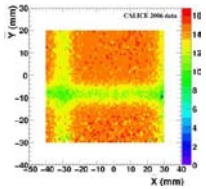
Peripheral dead zone : -20% of detection efficiency due to GR and mechanical structure

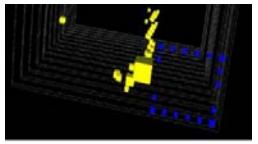
Can be compensated (off line)

« square » events : crosstalk between guard rings and peripheral pixels

Should be reduced by a factor 50 to 100

Ideas





Decrease the width of the dead area
⇨ Lower the thickness ☹ yield
⇨ reduce the bias voltage ☹ depletion , dC/dV
⇨ sawing technology (laser)
⇨ edgeless sensor ☹ cost

Collect charges generated in the dead space
⇨ read-out GR ☹ integration, data analysis

Bond the GR ☹ integration
⇨ Feasible with FE boards

Edgeless sensor ☹ cost
⇨ Various techniques

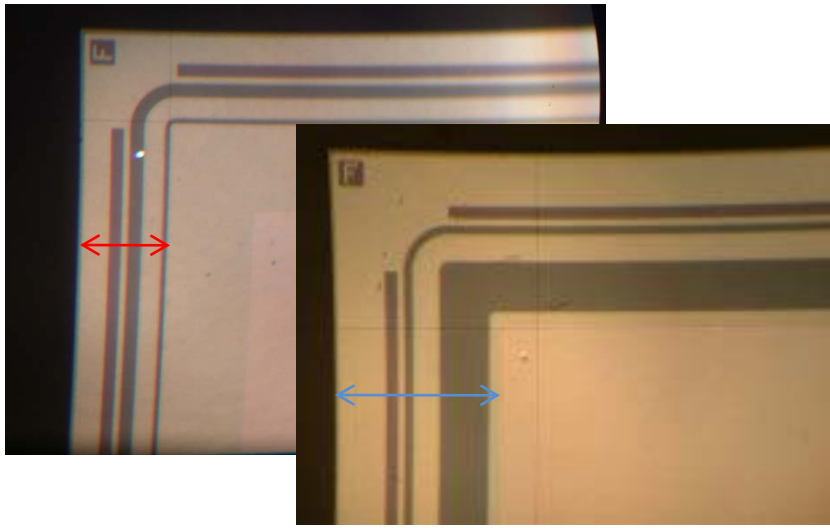
Segmented GR ☹ breakdown, yield
⇨Tested, need improvements
⇨ 2 IEEE papers
⇨ New tests with 300 um thick wafers from Anita Topkar (BARC), higher breakdown voltage, simlar Xtalk reduction.

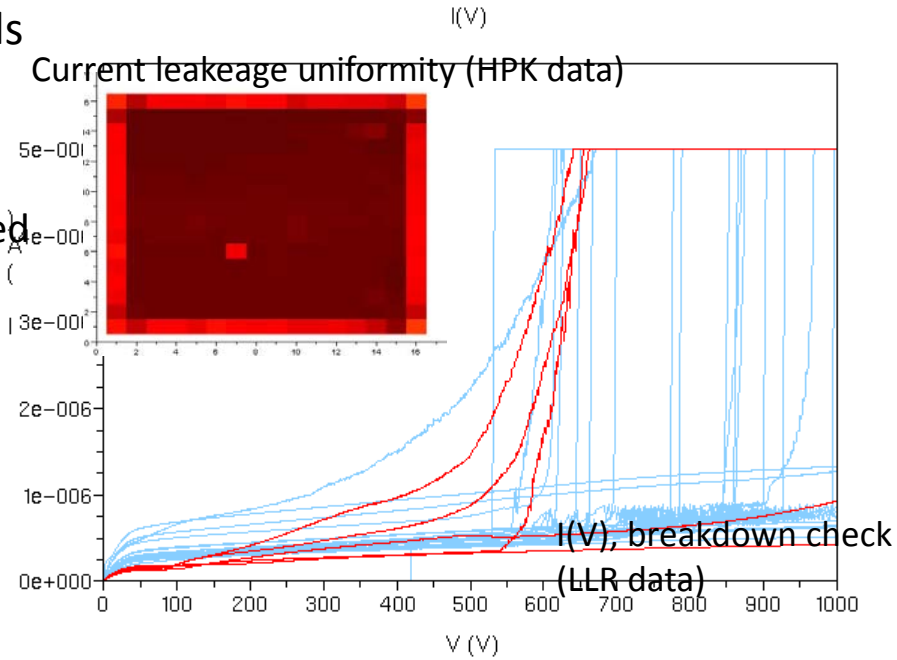
Future prototypes

- Wish to control overall cost
  - Alternate designs are possible
  - Appropriate selection of raw substrates
  - Process cost
  - Yield (overall)
  - Find best suited set of constraints set in the call of offer
- Changes in dimensions
  - 6x6 cm or smaller but with small dead space at the edges
  - Thickness up to 1mm (change in electronics gain)
- Relaxed constraints on electrical properties
  - Current leackage up to 10 nA per pixel
  - Vbreakdown =~300 V
  - Accept spread or non uniformity (if random) but with sorting (done at LLR)

HPK sensor V2

- 5 samples + production batch of 35 pcs
  - EUDET project needs 160
- “Dead area” decreased to 750 µm (1200 µm previous)
- Leakage current issue seen at Hamamatsu
  - Level: x 5-10 wrt previous sensors ,
  - non uniformity
  - Measurement procedure : adjacent pixels are tied to gnd
- Checks at LLR :
  - Global IV and CV (all pixels are shorted and tied to GND)
  - Will be improved : individual IV and CV
  - Breakdown ok but seems to be slightly lower





Industrialization

- Discussions with CEA/LETI (november 09)
  - 8 inches wafers, 4 matrices, 700 um thick (yield)
  - ST microelectronics
- Visit to HPK this month : confirm and complement what learned from LETI
  - Will use 6 then 8 inches wafers
  - 4 matrices processed at the same time (yield improvement)
  - R&D on laser sawing
  - Optimized thickness (yield vs width of dead space)
  - Optimized call of offer
  - ILD = 400% of production capability of a year (solid state devices division)
- Firsts contacts with VTT, SINTEF, MICRON semicond.
- In touch with PERKIN ELMER US & EU : both integration and manufacturing
- Not forgetting our historical collaborators : FZU (ONSemi), MSU, BARC, …
- More discussions needed but a strategy is being build on “real” inputs from manufaturers

Outcome

- Si-W ECAL : A large amount of the critical components of the detector have been validated individually
- Assembly and tests at system level should follow
- Some issues are remaining
  - Power pulsing & power supply
  - Long SLAB
  - High voltage (bias)
  - **DAQ** & Test beam setup
  - Sensors development plan
- Sustained efforts to

start SLAB assembly not too late