Laboratoire d'Annecy-le-Vieux de Physique des Particules

Calorimeter for ILC

DHCAL Electronics and DAQ at LAPP

Guillaume Vouters for Linear Collider group at LAPP

Casablanca - 23 septembre 2010

CENTRE NATIONAL DE LA RECHERCHE SCIENTIFIQUE

IN2P3 Institut National de Physique Nucléaire et de Physique des Particules

UNIVERSITE CHAMBERY SAVOIE ANNECY

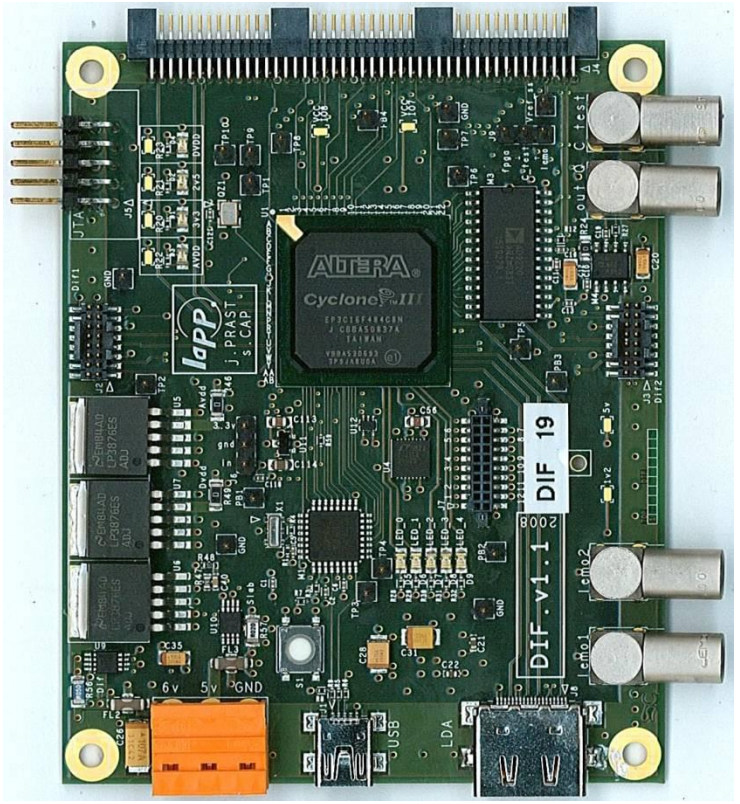
Outline

I. DIF
II. DHCAL MICROMEGAS Square Meter
III. DHCAL Square Meter assembly
IV. DHCAL DAQ
V. MICROROC
VI. WHCAL DAQ

I. DIF

DHCAL DIF production for the Cubic Meter

- **170 DIFs have been produced**
- Boards have been tested at LAPP with a special Test bench (Boundary scan + functional tests).
- 165 out of 170 DIFs are fully operational
- **DIF Boards are now available**



I. DIF

Test Bench and test procedure

1) Verifier les courts circuits entre les alims

➔ 15 combinaisons à effectuer

2) Brancher le connecteur **ALIM** et alimenter la carte

Vérifier le courant !!

3) Verifier les valeurs des alimentations

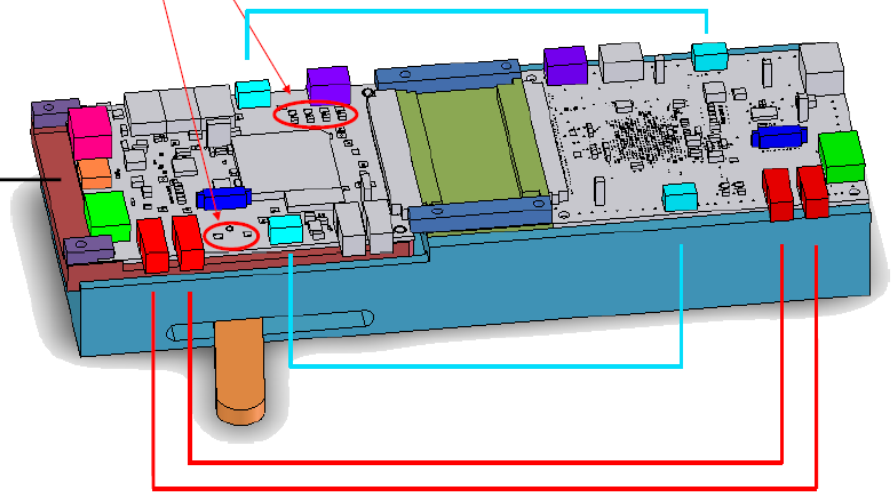
1v2 5v 3v5 3v3 2v5 3v3

4) Couper l'alimentation

5) Brancher les autres connecteurs :

- Dif-dif
- Lemo
- HDMI
- USB
- JTAG
- mezzanine

voir couleur



PC

6) Plugger la carte en tirant la poignée vers la droite.

7) Alimenter la carte de nouveau

8) Lancer le test

PASS

FAIL

T) Trouver la cause et recommencer au 8

9) Débrancher le **JTAG** et brancher celui de Quartus

10) Programmer le FPGA

11) Tester la liaison USB avec le programme en LabView

12) Couper l'alimentation

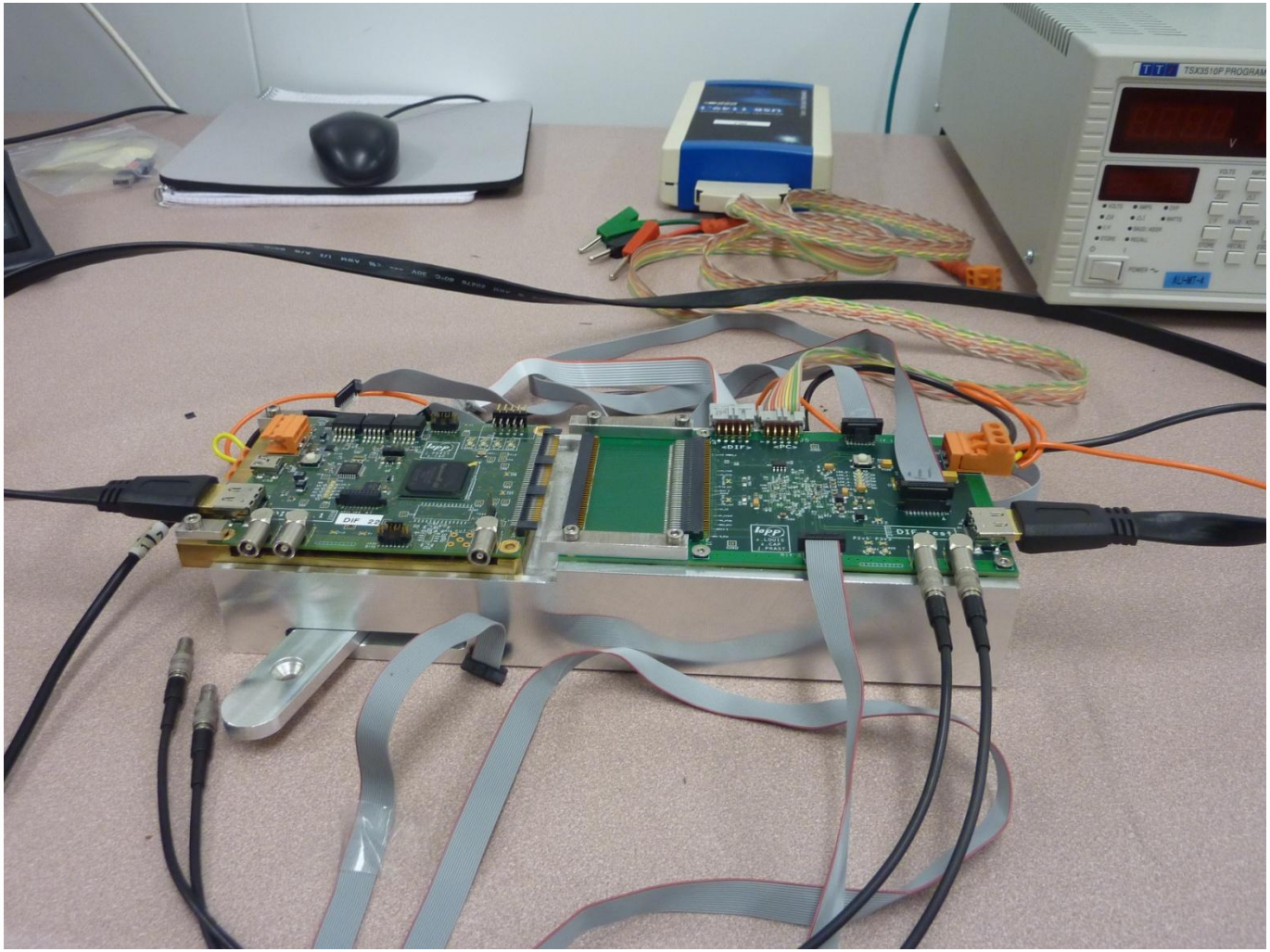
13) DéPlugger la carte en tirant la poignée vers la gauche.

14) Débrancher les connecteurs

!!! NE JAMAIS DEBRANCHER LES CABLES DE LA DIF-TEST (carte de droite)

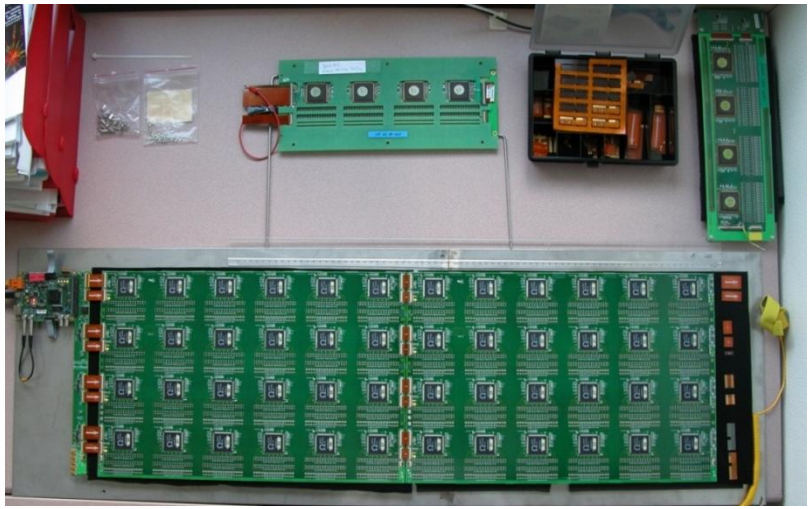
I. DIF

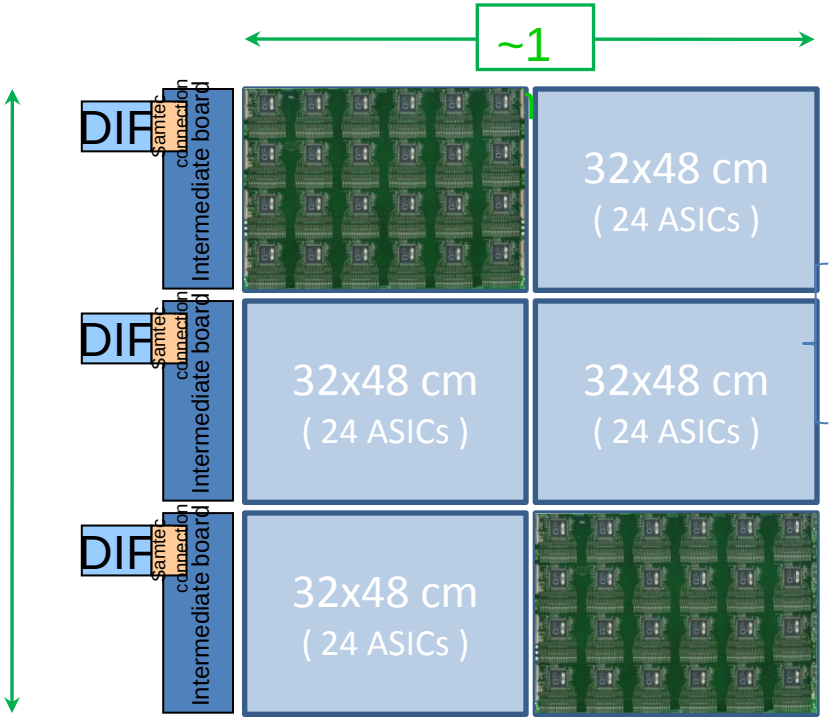
Test Bench and test procedure



II. DHCAL MICROMEGAS Square Meter

ASU 32x48 with HARDROC v.2





A SLAB : 2 chained ASU

→ We managed to control 48 HARDROCs v.2 with 1 DIF

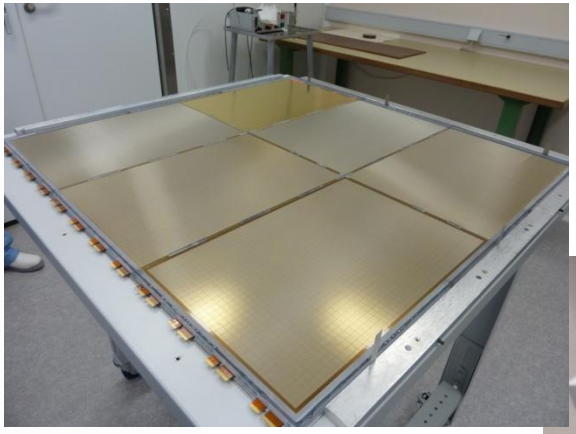
Square meter

→ 4 SLABs with HR2 (with Slow Control bug)

→ 1 SLAB with HR2b

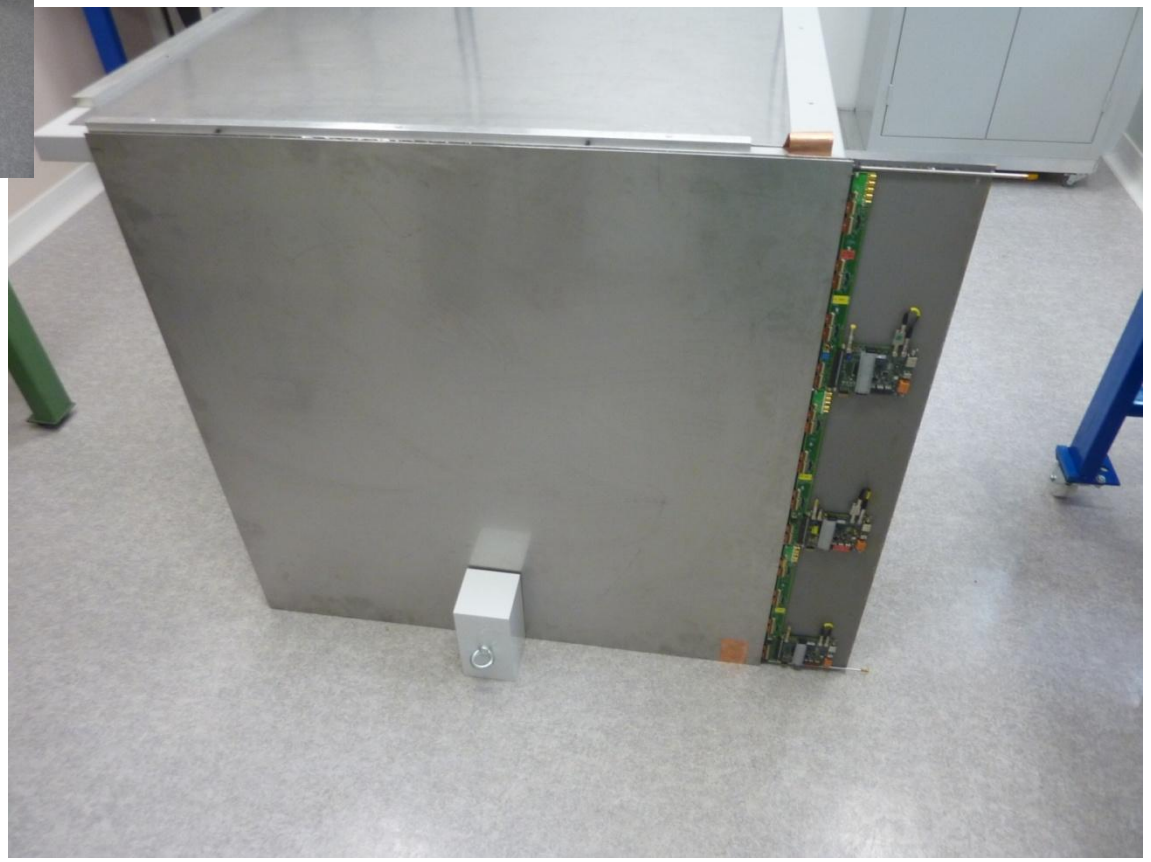
III. DHCAL Square Meter Assembly

MICROMEGAS Square Meter



Inside the square meter

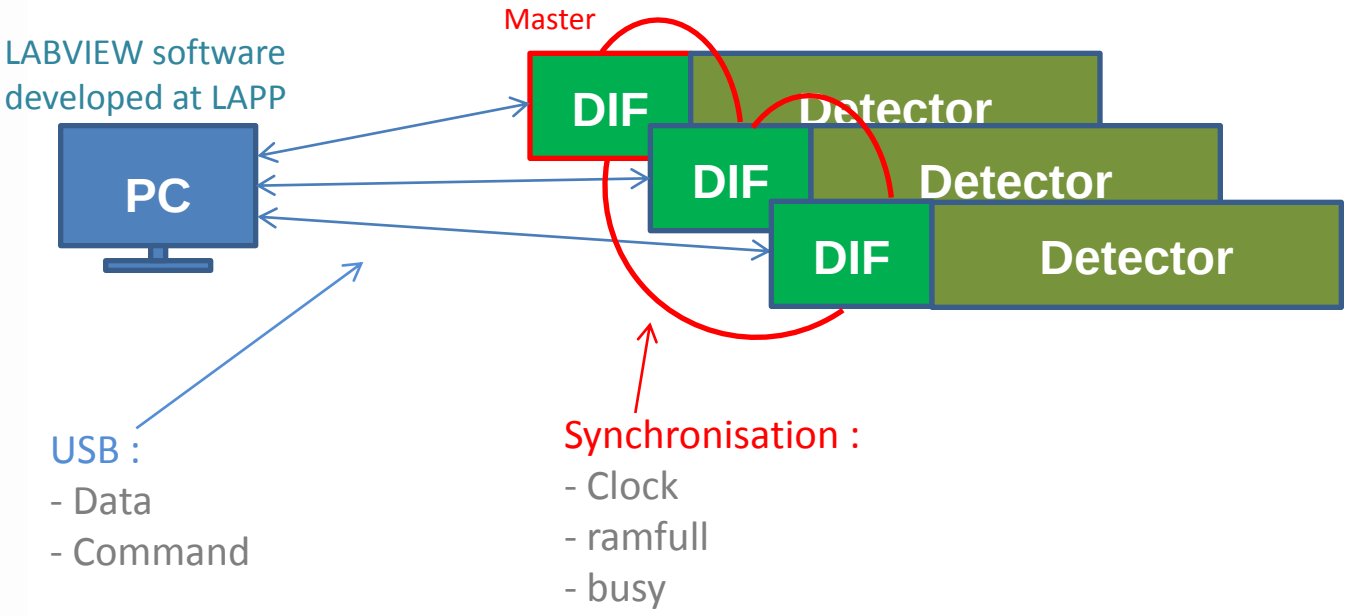
MICROMEGAS square meter structure



See Jan Blaha's talk for results on Beam Test on DHCAL session

IV. DHCAL DAQ

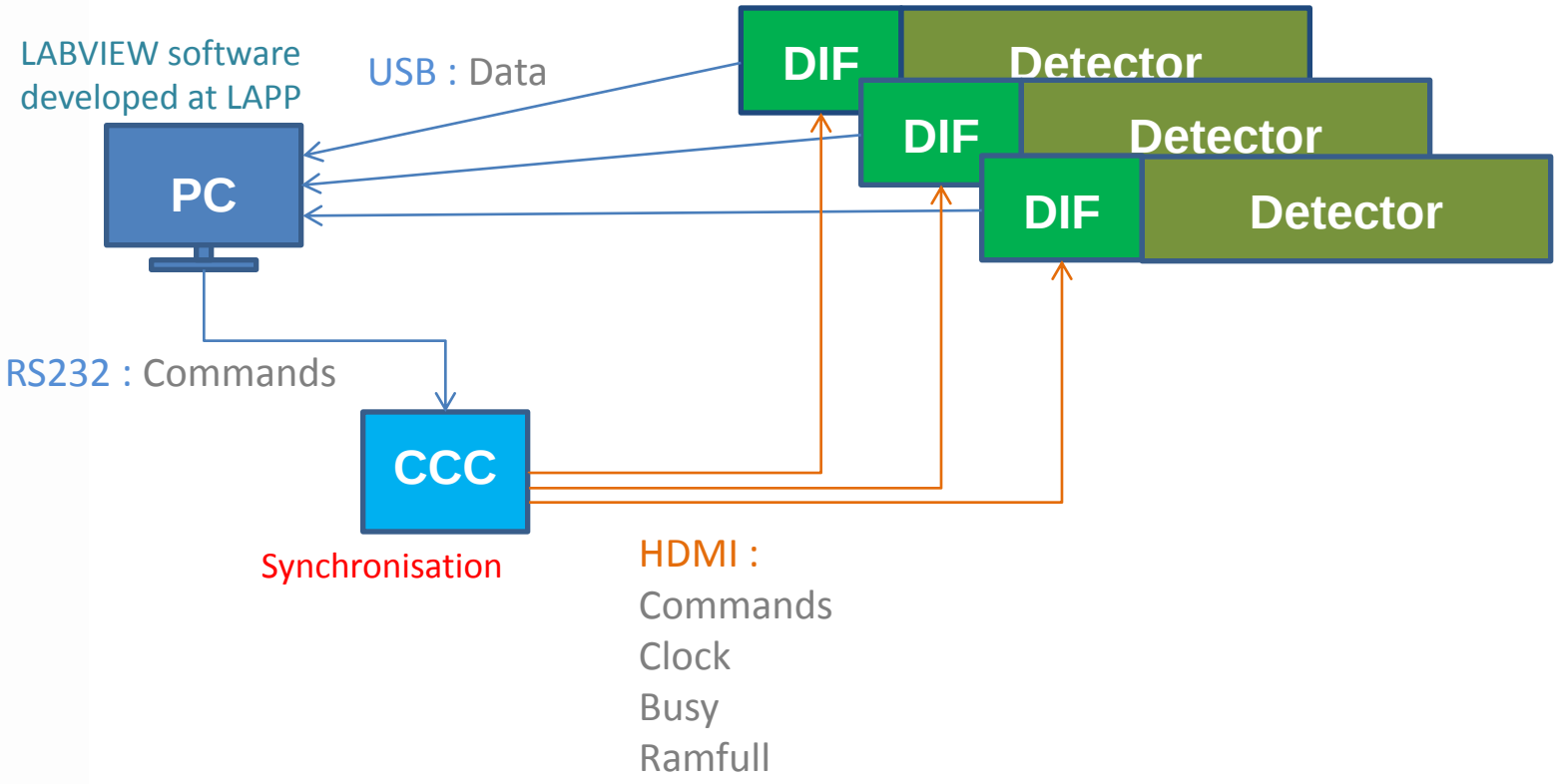
Past Architecture



Not suitable for lot of DIFs…

IV. DHCAL DAQ

Intermediate Architecture

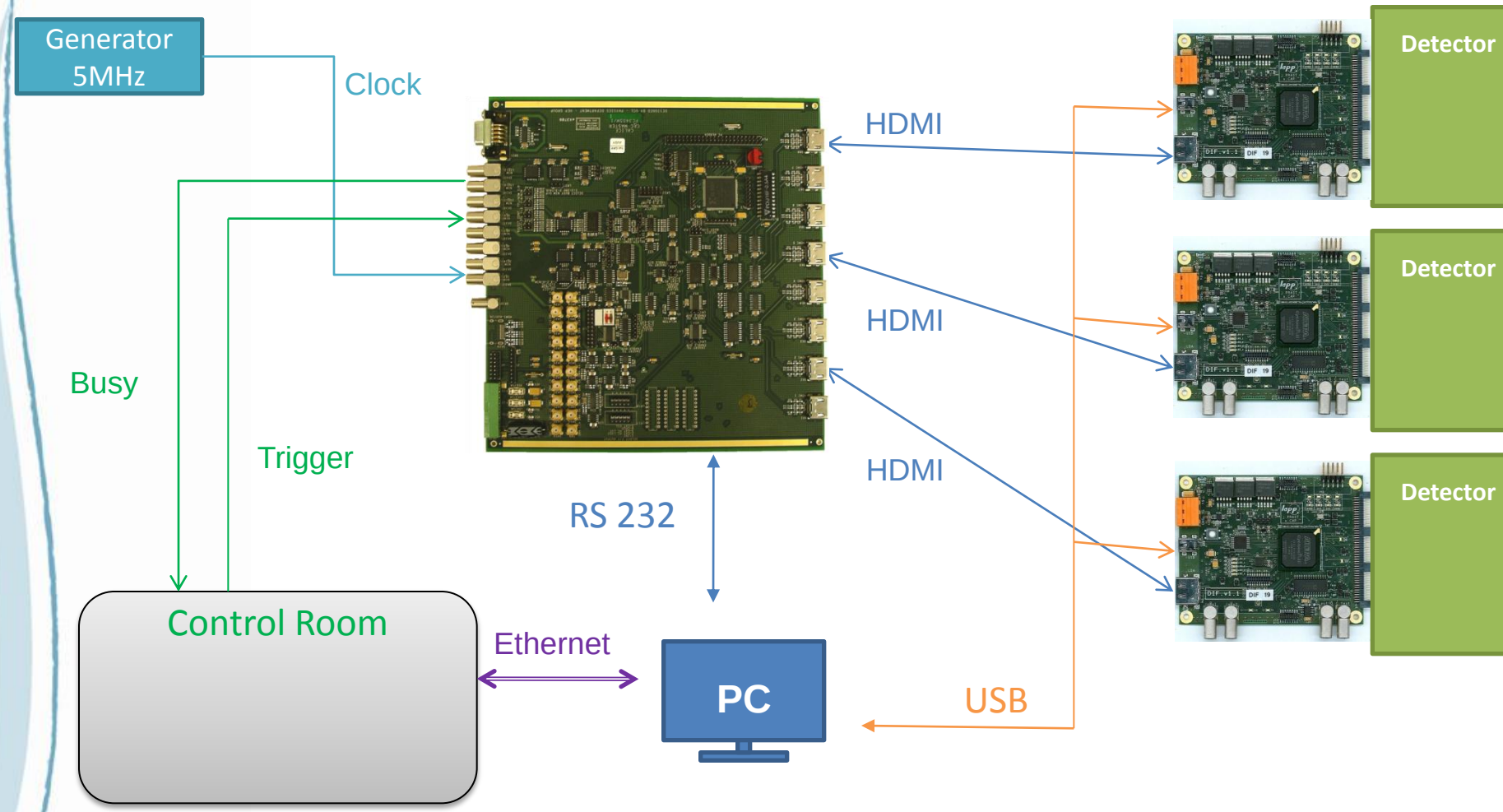


Before the DAQ CALICE is ready, we need to be able to synchronize more than 3 DIFs.

- New specific firmware for CCC
- Perfectly synchronized
- Easy to use up to 8 DIFs (or more using CCC in cascade)
- Limiting factor : USB communication

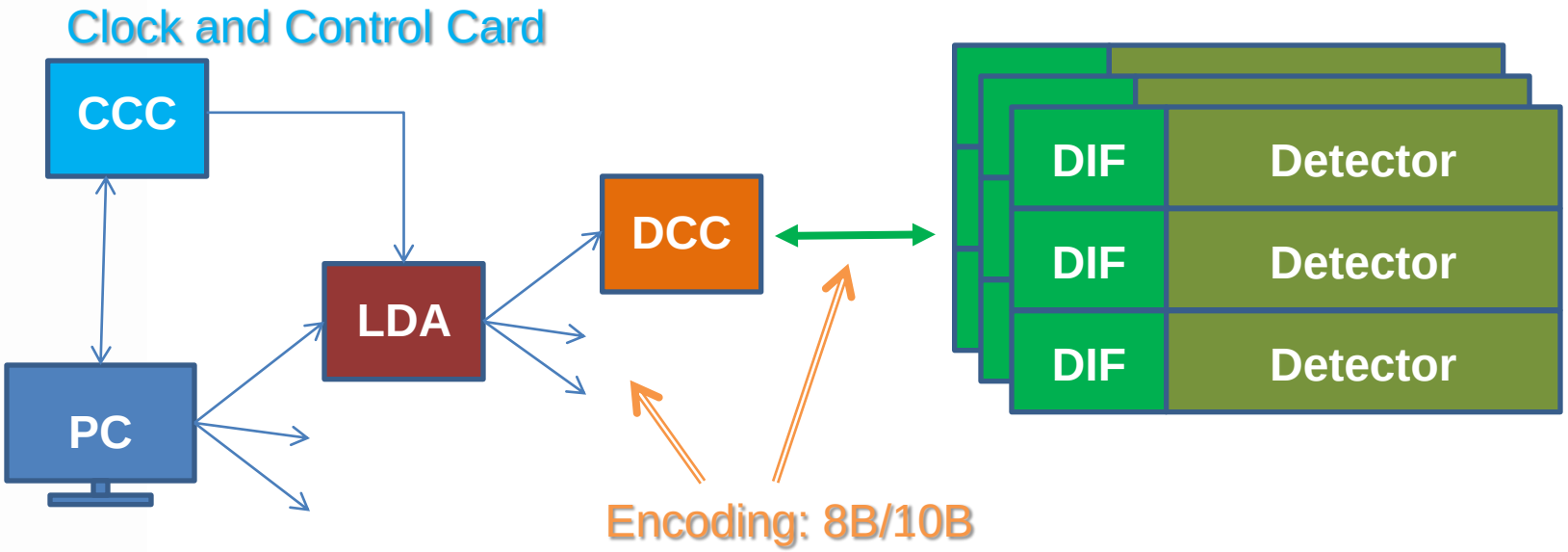
IV. DHCAL DAQ

Use of the CCC for the intermediate DAQ



IV. DHCAL DAQ

Future CALICE DAQ Architecture



The 8b/10B encoding/decoding has been tested with the DHCAL DIF. This board has been developed with an Altera FPGA whereas the 8B/10b has been coded with a Xilinx FPGA as target. But the conversion was a success and data was sent and received between the DCC and the DIF.

Data for Slow Control have been sent from a PC to DIF through all the CALICE DAQ with VHDL code shared between LLR and LAPP. In both sides.

Next Step is to configure ASICs on detectors with those data.

V. MICROROC

MICRO MEsh GAseous Structure (MICROMEGAS) and Gas Electron Multipliers (GEM)

MICROROC is a fruit of the collaboration between LAPP and LAL/OMEGA based on the experience of previous ASICs (DIRAC and HARDROC) and on multiple test beam results

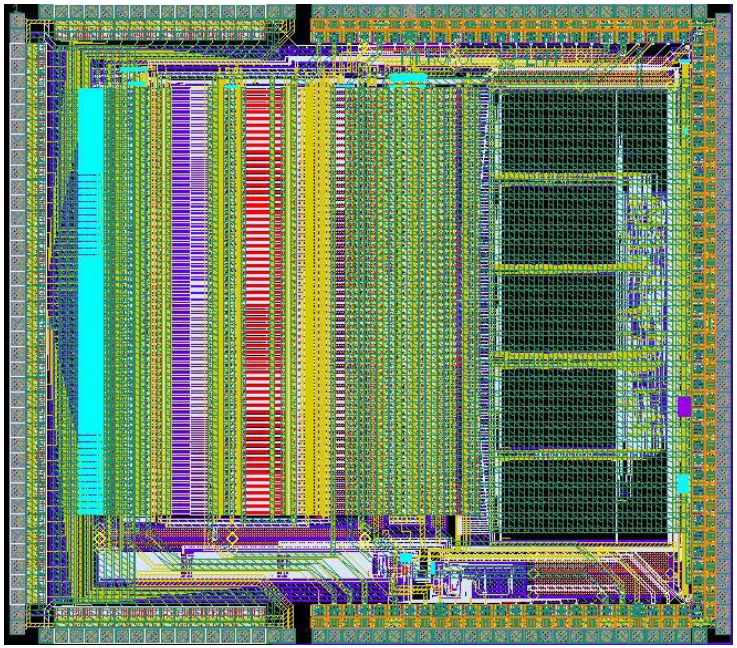
MICROROC is a 64 channels integrated circuit packaged in TQFP160.

- Same Digital part than HARDROC2 :

Same Acquisition and Readout feature than HARDROC2

- MICROROC is pin a pin compatible with the HARDROC2 :

very few development to do on firmware, software or test board



V. MICROROC

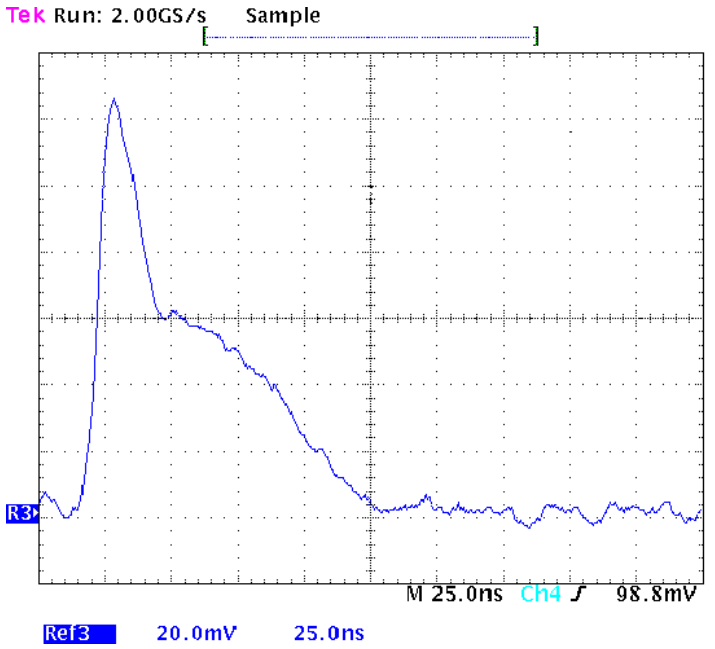
What's New comparing to the HARDROC2 ?

- A new Shaper

Possibility of a short or a long shaping : 50 to 200ns by 50ns step

- New protections against Sparks

- Slow Control a bit different



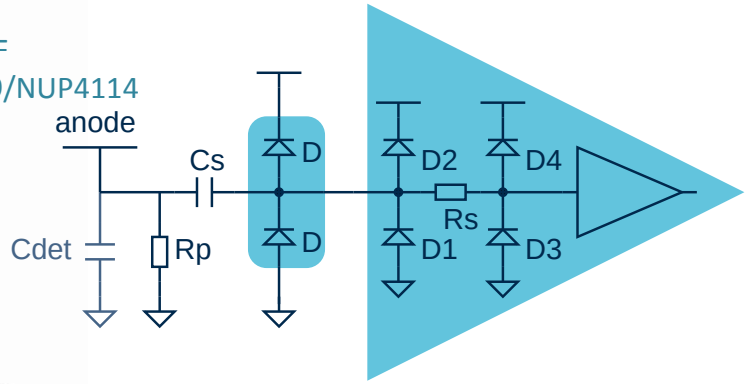
Protection network :

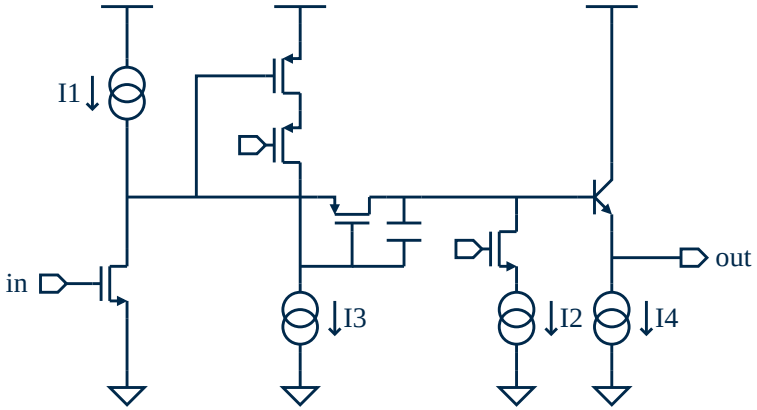
Cdet=80pF

Rp=1MΩ

Cs=470pF

D=BAV99/NUP4114



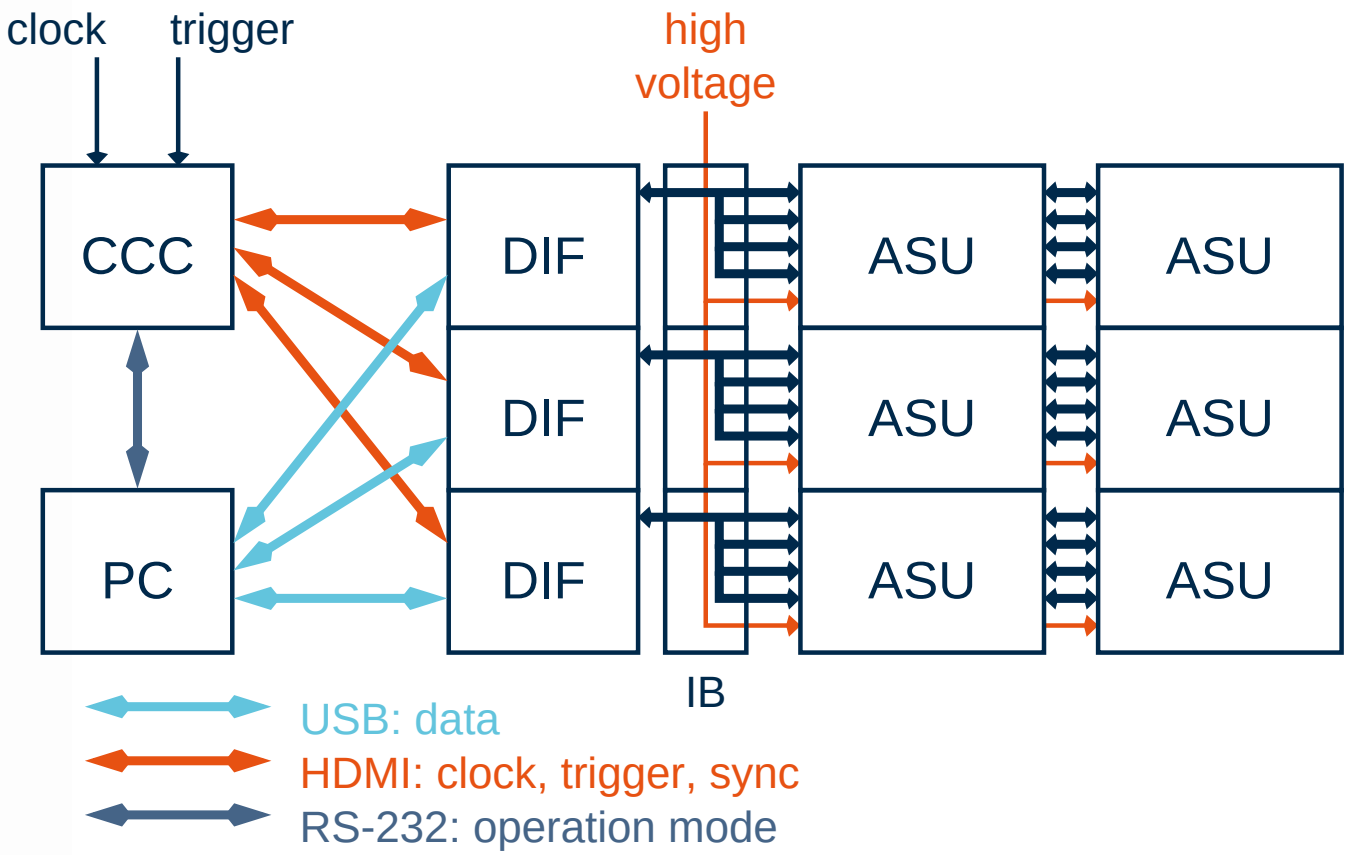


Consumption : 1.1mA

V. MICROROC – Based ASU

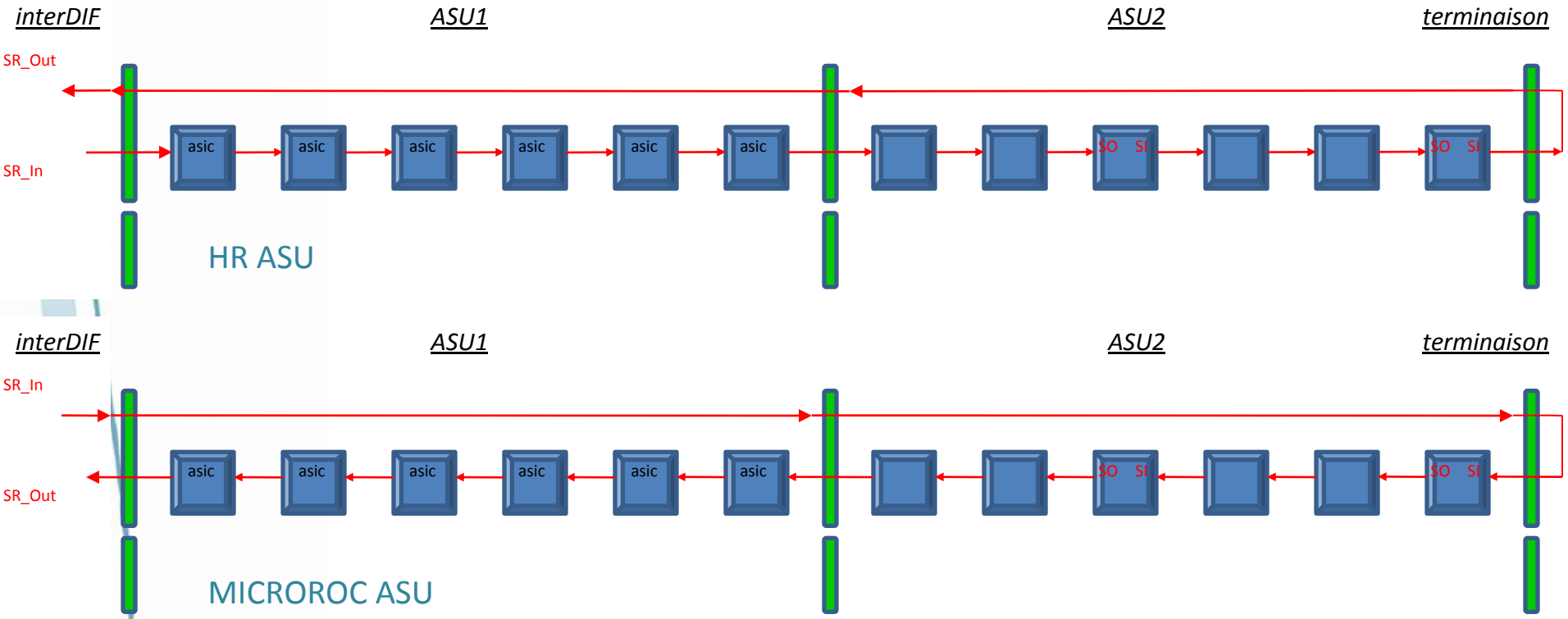
ASU Modification, What's New ?

Experiences with actual HR2 ASU leads us to modify the next MICROMEGAS ASU and intermediate board.



V. MICROROC – Based ASU

Slow Control modification

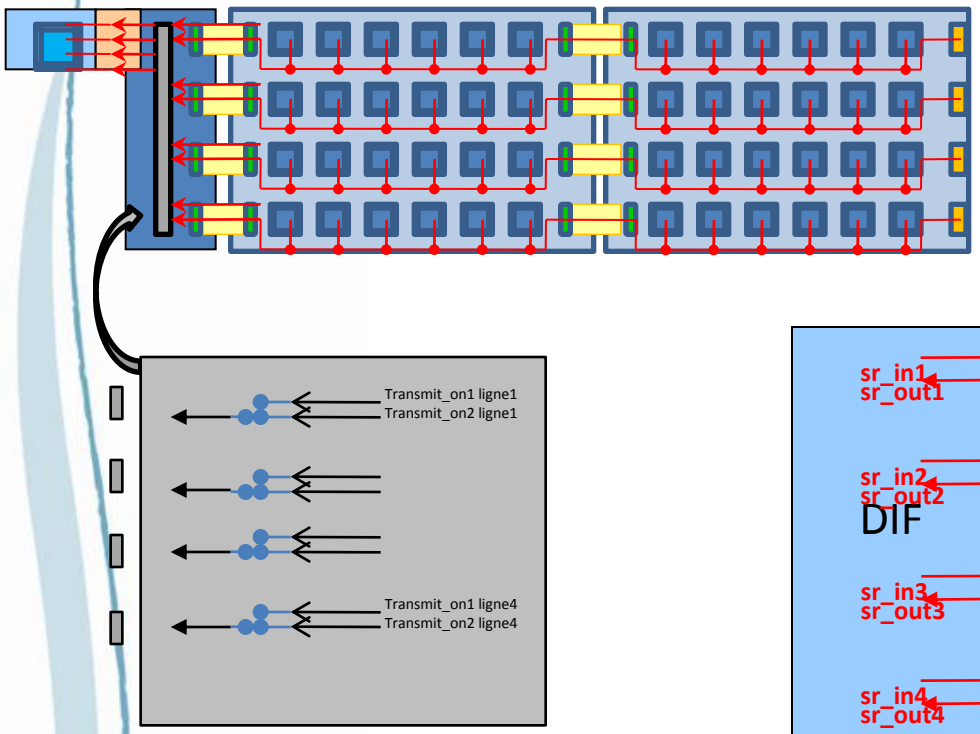


This ligne will serve to Slow Control or Analog Readout according to the state of the signal « SC_Select »

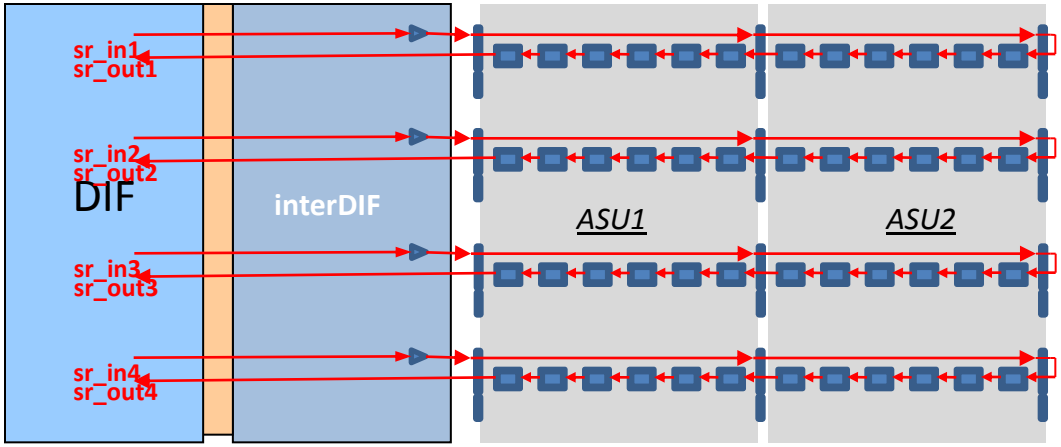
The aim of this modification is to avoid adding drivers on the ASU

V. MICROROC – Based ASU

ASU modifications



Transmit_on / Dout



Pullup signals like transmit_on will be received independantly

The aim of this modification is to perform a faster readout : the four lignes will be read in the same time.

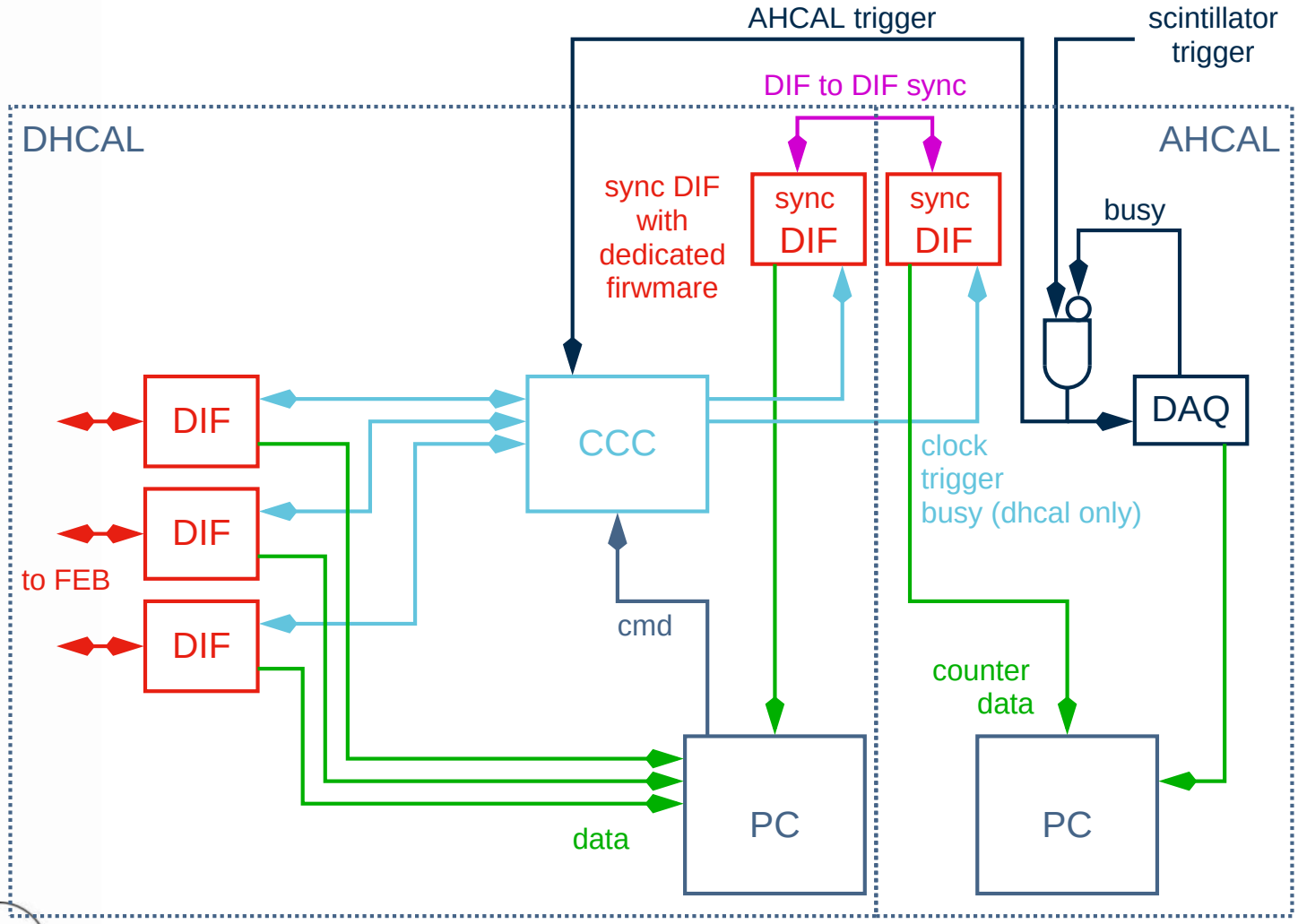
The DIF will control the four ASU lignes independantly

The aim of this modification is to be able to bypass a ligne where a CHIP could be not working anymore. We should be able to configure all the other lines.

VI. WHCAL DAQ

Should synchronize 2 DAQs (W-AHCAL, W -DHCAL)

Synchronization : Common event number (AHCAL trigger), not all events are recorded by DHCAL



IV. Conclusion

DIFs for the cubic meter have been produced and successfully tested :
97% of the DIFs are fully operational

DAQ intermediate architecture is fully operational :
- It has been used in June MICROMEGAS Beam Test
- It's available for RPC acquisition

DIF VHDL for the future CALICE DAQ is on going, Slow Control feature is almost working.

The MICROROC ASIC, dedicated for large area MICROMEGAS readout has been produced and soon ready to be tested.

Next step for MICROMEGAS detectors is the WHCAL Beam Test