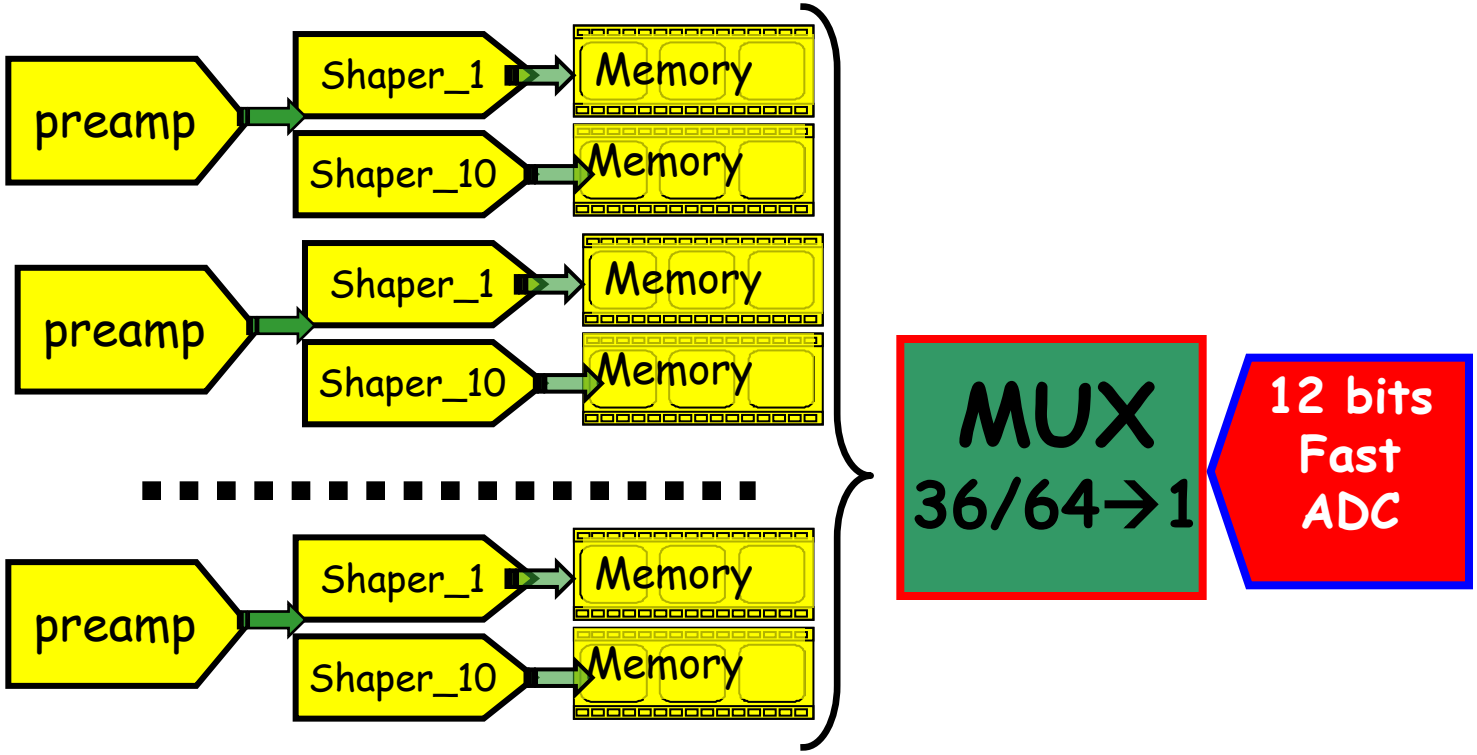
Status on contributions from Grenoble

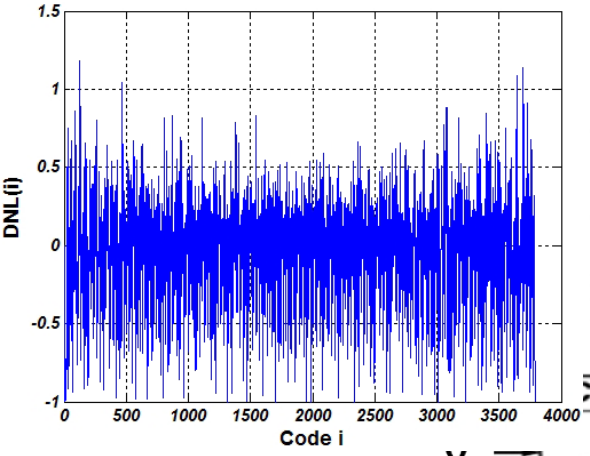
1. Pipe line converter design for high speed digitizer configuration
2. 14 bits DAC for integrated calibration issue
3. DAC extension to SAR ADC => new proposal

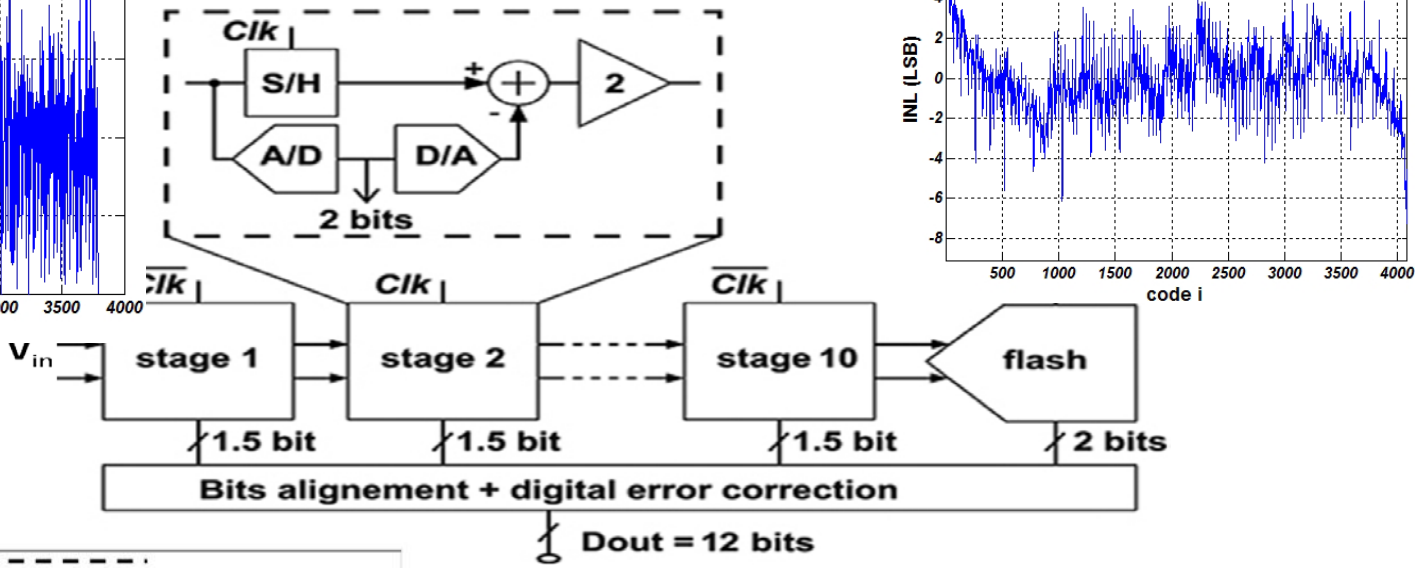
Fast Digitizer configuration:
Pipe line ADC

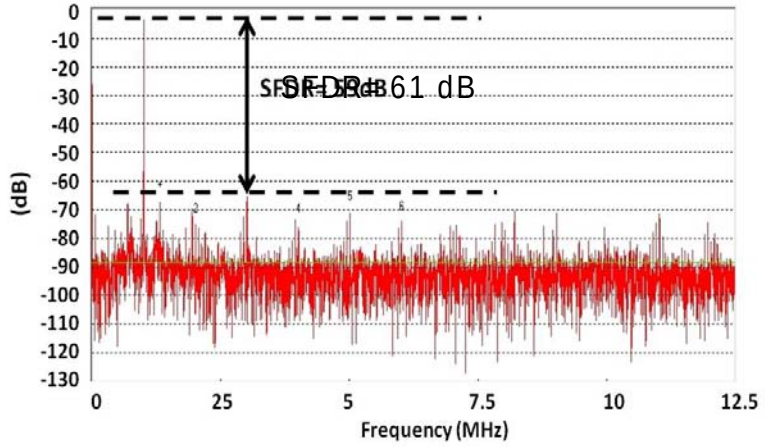
Assumption => To reduce the total power **by reducing the conversion time**



Already published results and **process limitations**







These results correspond to the Dispersions known for the 0.35µ.

Going beyond these results will lead to bad yield for the chip production

How can we improve these results?

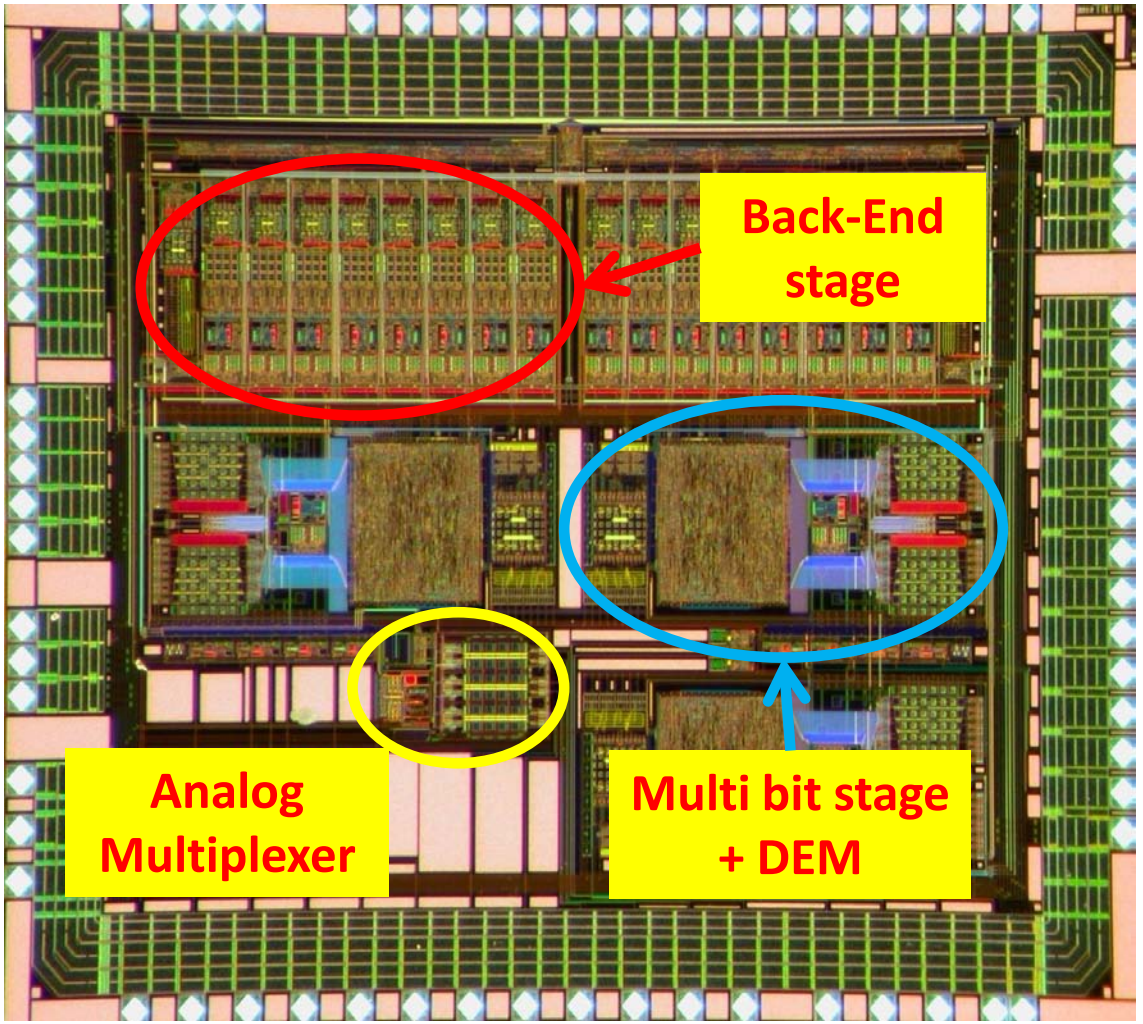
Since 2 years now, we are working on: Multi bits stages with DEM algorithm.

1. The first prototype in this configuration shows that the DEM is effective.
2. But designing a multiplier by 4 appears more difficult than expected;
   then the new results were not actually better according to the INL.

- Our last prototype was submitted in May and we just receive it (September15)

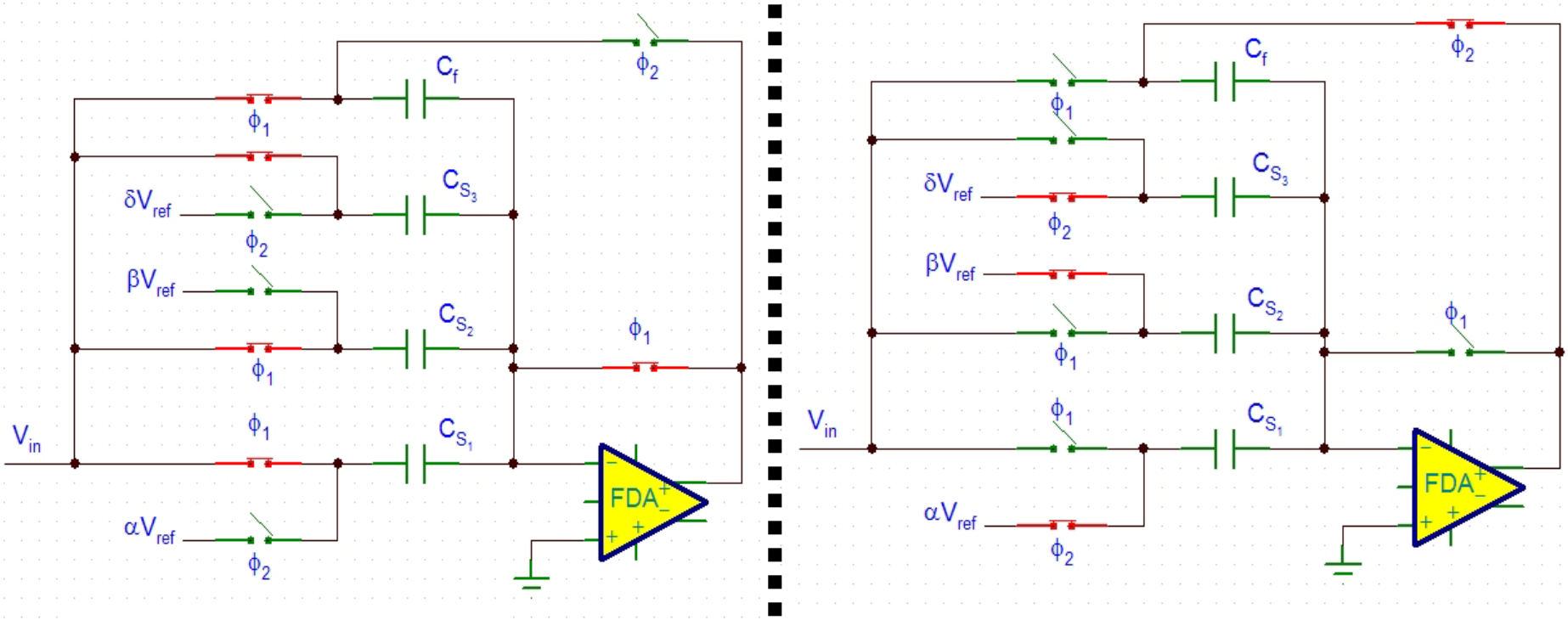
Our last prototype received Sept. 15th:

Pipeline ADC +Analog multiplexer +MDAC with buffer for analog testing



Multiplying and DAC 2.5 bits

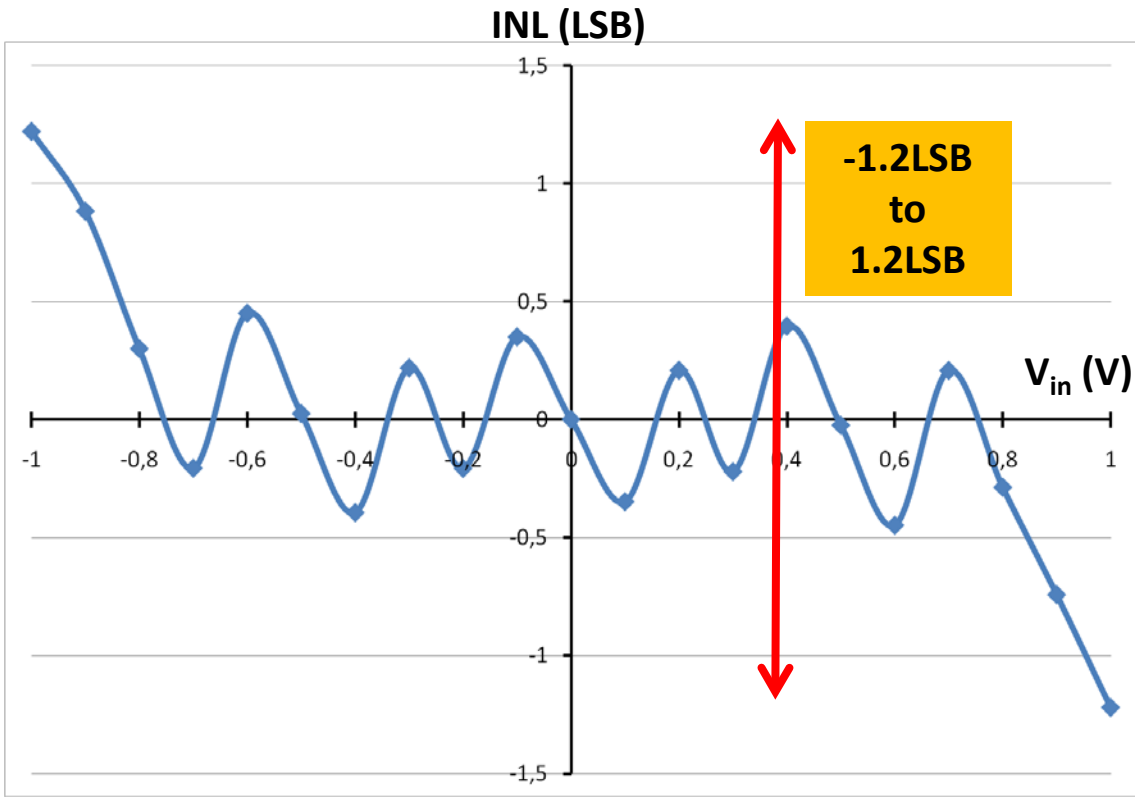
- **Architecture**



Sampling phase **Hold phase**

$V_s = 4 \times V_{in} - 3 \times \mu V_{ref}$, μ=[-1, 0, +1] depends on sub-ADC output

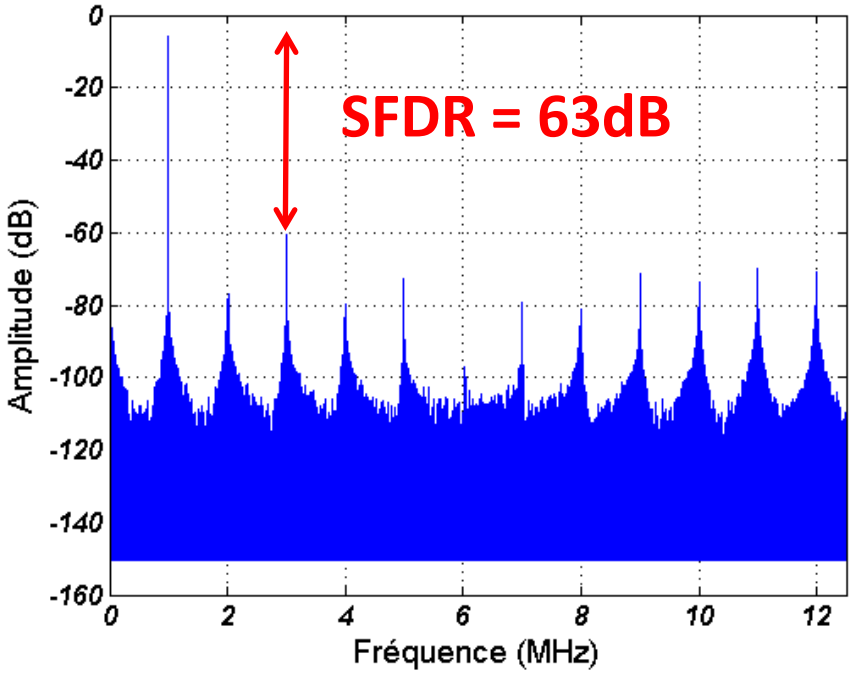
MDAC simulation results



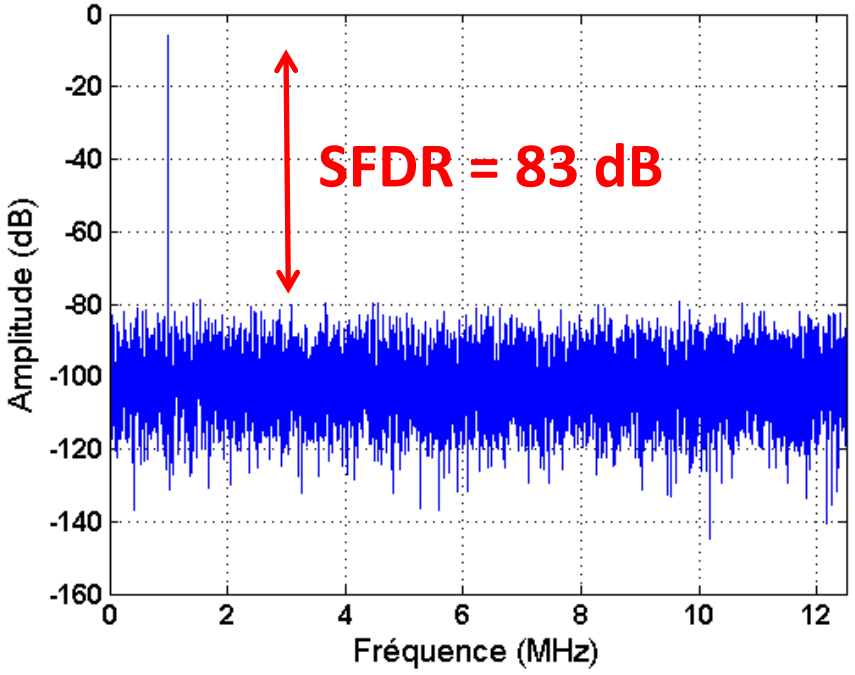
Multi-bit MDAC linearity (LSB@12bit)

Model of Dynamic Element Matching

Simulations results

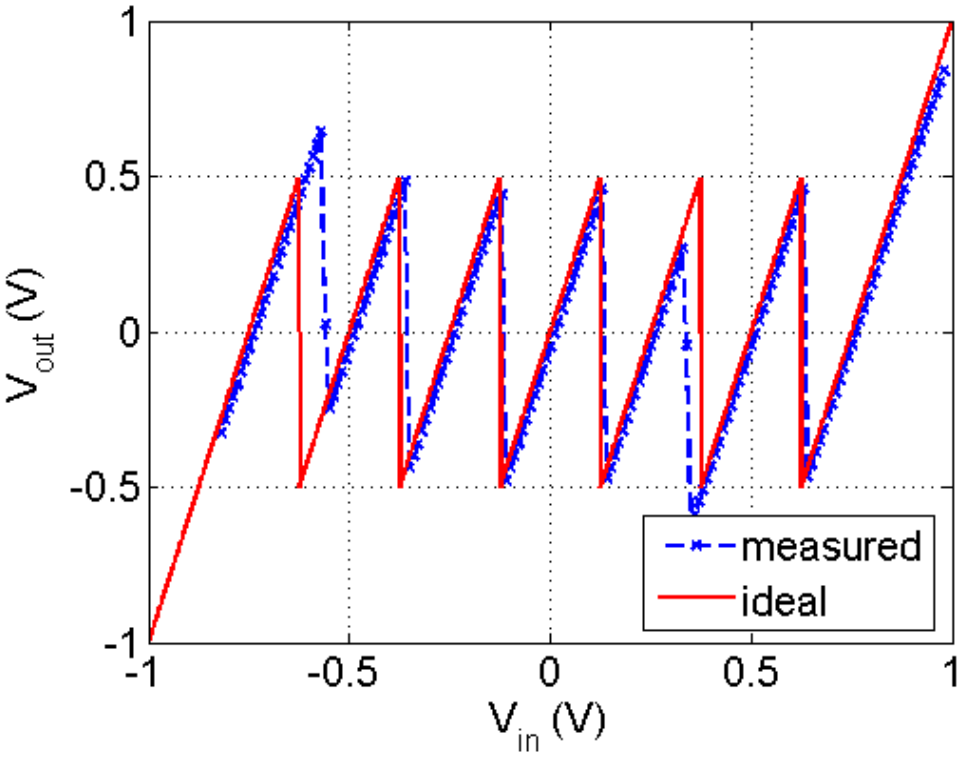


a) Output spectrum with without DEM



b) with DEM

2.5 bit MDAC Test results

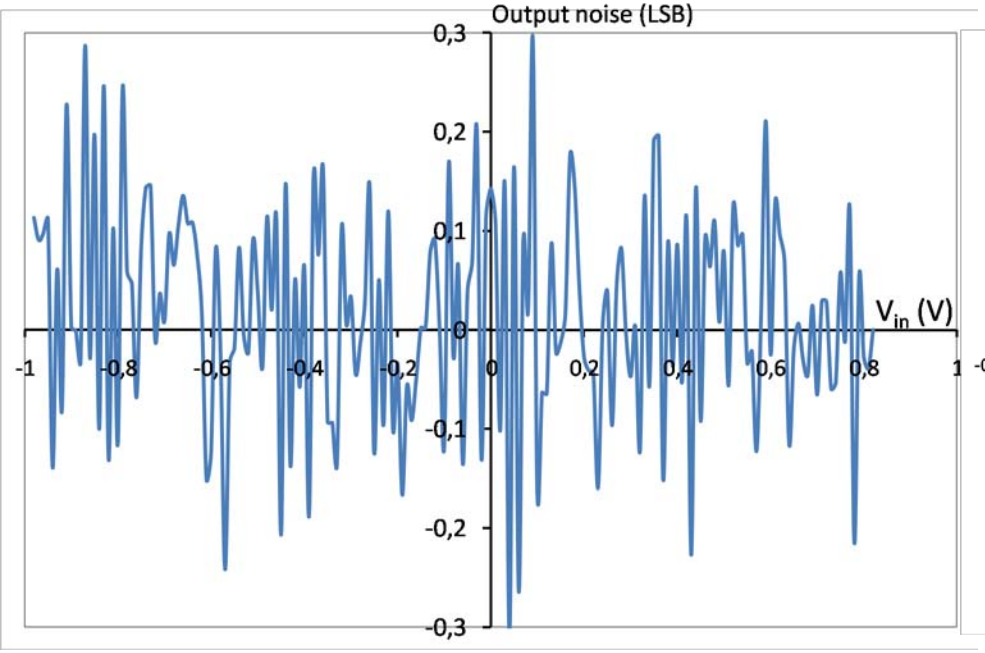


Residue transfer curve of the multi bit stage

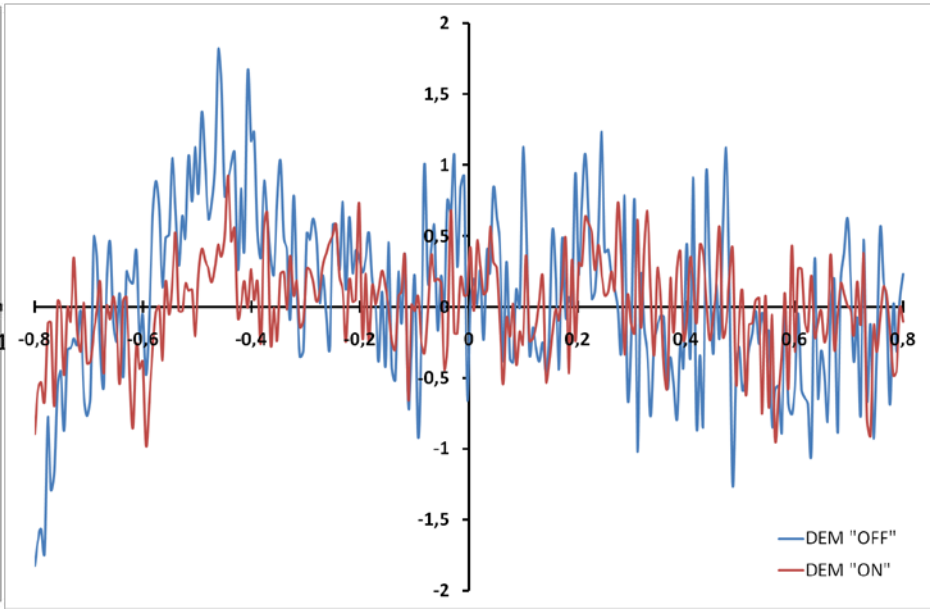
→ **Dynamic Comparator Offset about 60 mV**

→ **Good linearity in the multi-bit first stage**

2.5 bit MDAC Test results

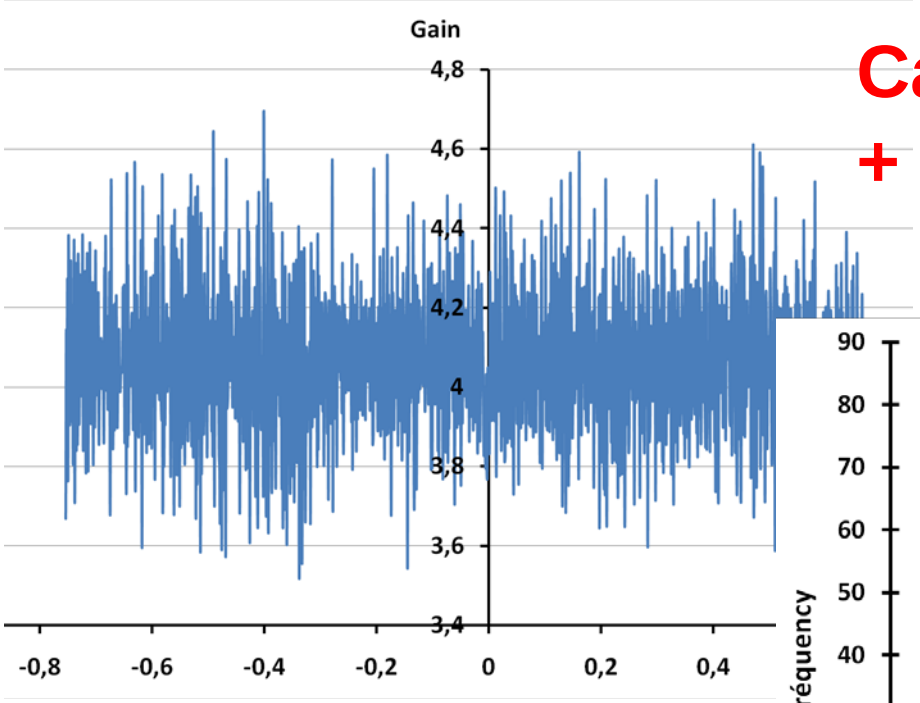


2.5 bit MDAC output noise



2.5 bit MDAC output linearity
The DEM improves the INL

A 2.5 bit MDAC with a DEM + integrated buffer Testing results

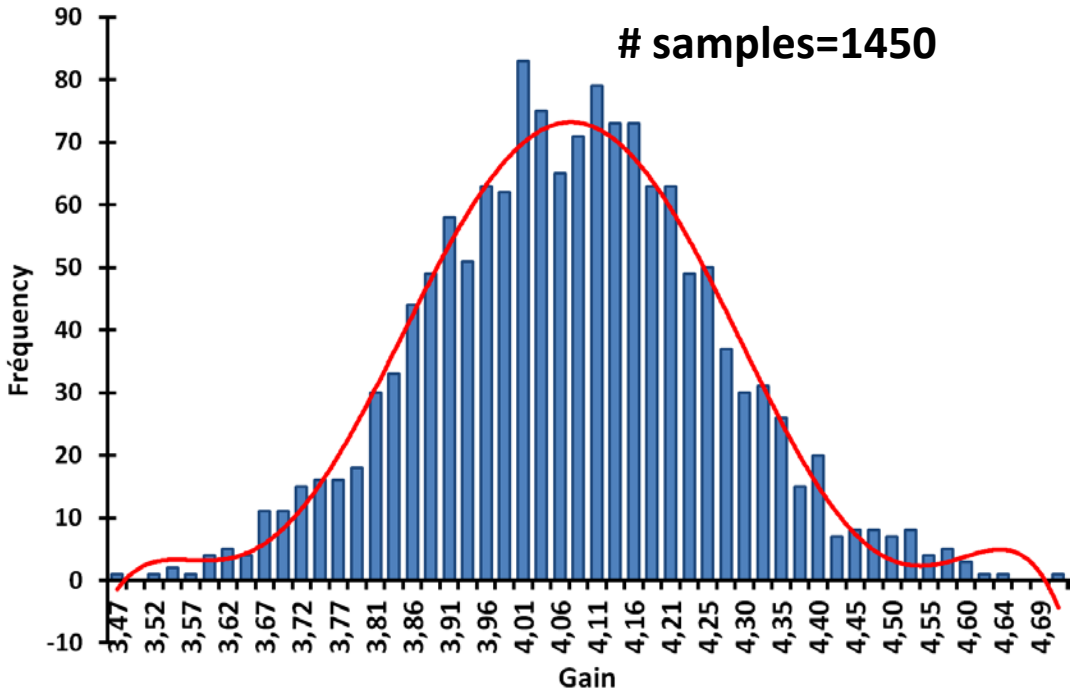


Capacitors matching + parasitics effects

μ = 4.06

σ = 0.19=>0.5%

 # samples=1450

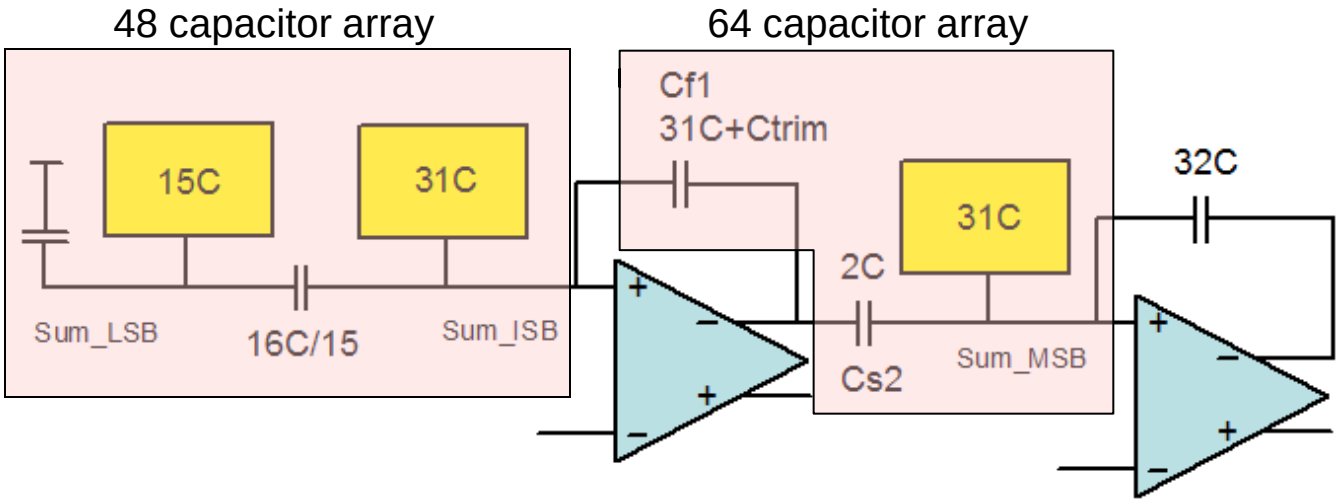


2.5 bit MDAC: expected average Gain is 4

FIRST CONCLUSIONS with this proto

- The DEM seems effective on MDAC
- The output linearity on MDAC is reasonable
- We need now to go through the test of full ADC
- The matching of the capacitors is still a challenge
- This challenge in the technology, exists for any other charge transfer circuit.

A 14 bit 5MS/s SCDAC (2009)



- Switched Capacitors architecture.
- Power pulsing
- DEM algorithm is included to improve the INL.
- Trimming for this 1st prototype : 0.1C step.
- Charge injector to be designed.

Layout : 14 bit DAC (2009)

CMOS 0.35µm

Vdd = 3.3 V

DEM => 0.2 mW @ 5MHz

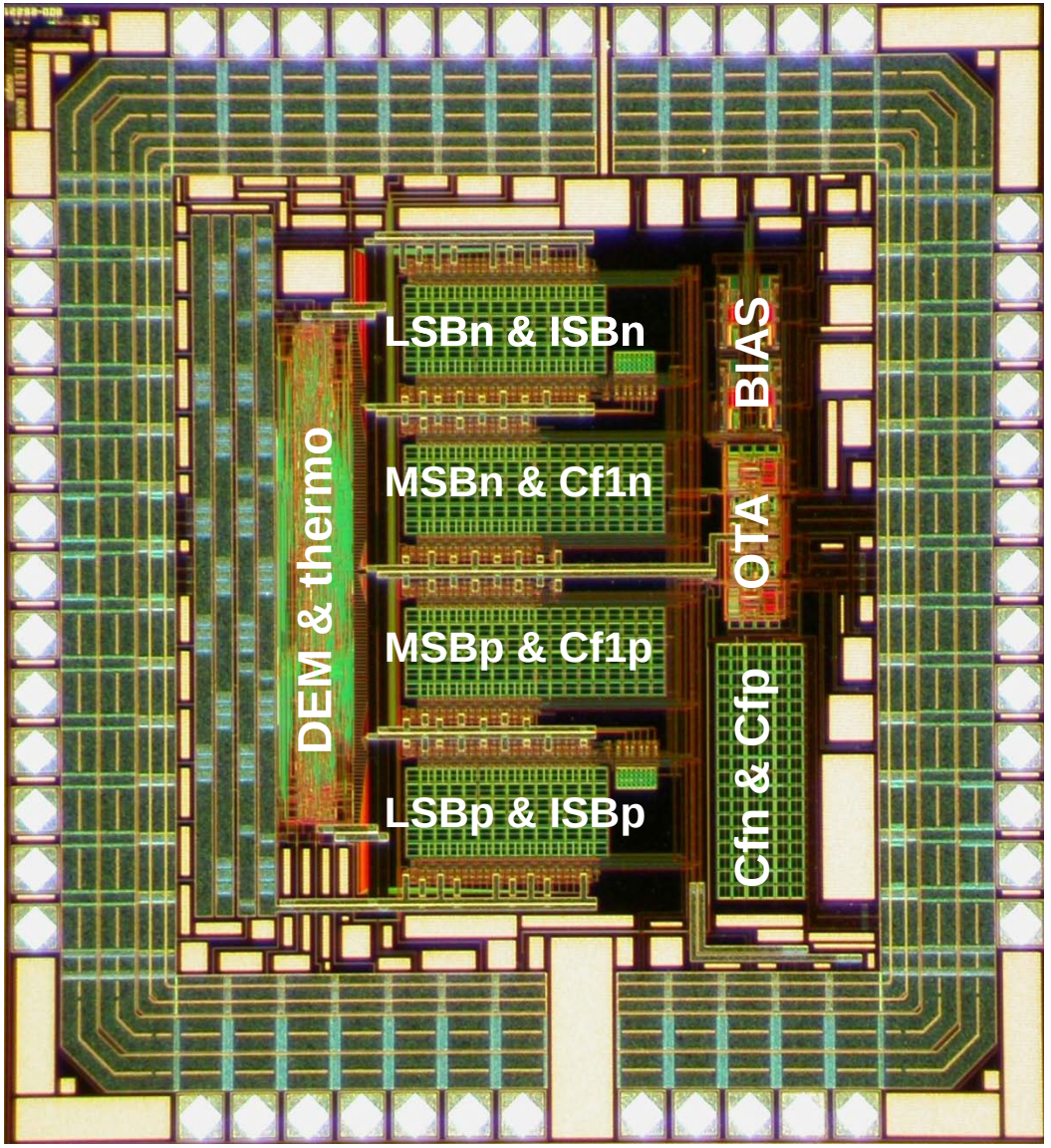
OTA => 2 x 2.2 mW

BIAS => 2.5 mW

DAC14 => 7.1 mW

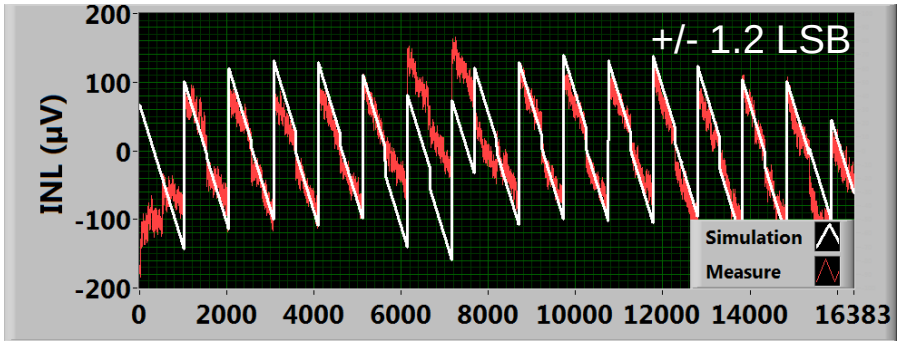
Idle mode : < 1µW

Active area : 1.3 x 1.1 mm^2

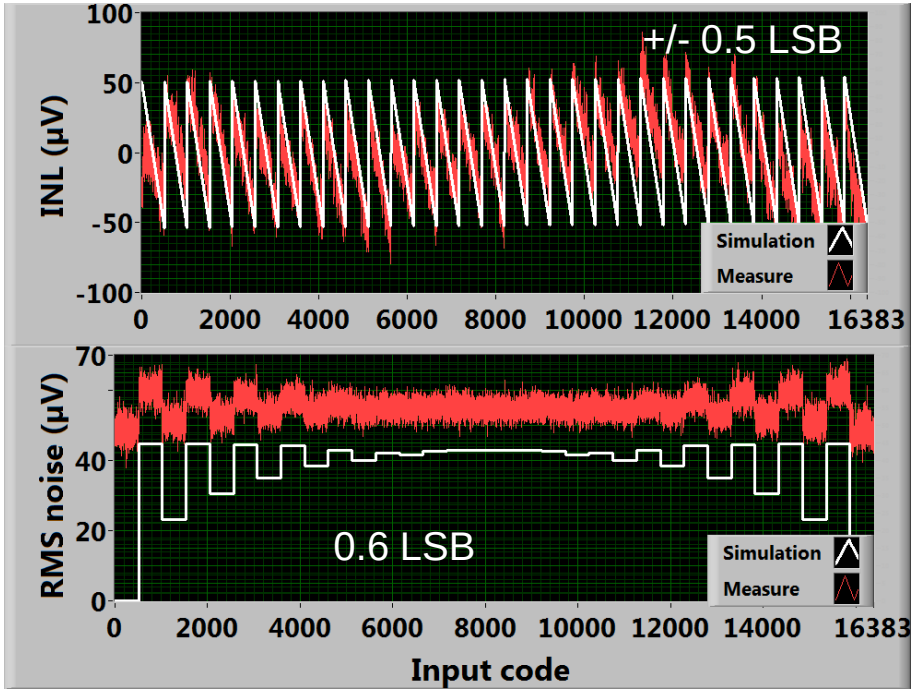


Simulation and test results : (2009) static parameters of the 14 bit DAC

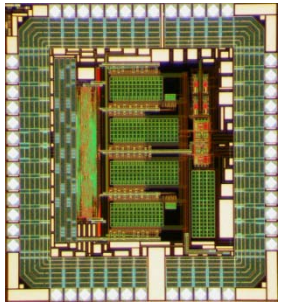
DEM OFF



DEM ON



- ME : from 0.25% to 0.4%
- DAC model : very good agreement / exp. Data.
- DEM : INL improved by a factor of 2.
  small effect on the noise.
  remaining INL => 0.1C trimming step.
- trimming value : same for 9 tested chips.
  found with HL simulation.



1.3 x 1.1 mm^2

Simulation and test results : (2009) main features of the 14 bit DAC

DAC main features	Test results	
	DEM off	DEM on
Area (mm^2)	1.4	
Power (mW)	7	
Frequency (MHz)	5	
INL (LSB / µV)	**1.2** / 150	**0.5** / 60
RMS noise (LSB / µV)	0.5 / 60	0.6 / 70
THD (dB)	-89	-96
SNR (dB)	82*	81*
ENOB	**13.2***	**13.2***

*** limited by the testing board noise**

A 14 bit 1 MS/s SAR ADC : (2010)

- Relies on an ***improved version of the 14 bit DAC***.
- Power pulsing.
- Can also be used as a **14 bit 15 MS/s DAC.**
- DEM algorithm is included to improve the INL.
- DEM efficiency for multi pixels' events: under evaluation.
  - Validated with an home made event generator (1024 pixels & 16 ADC).
  - To be validated soon using data from SiW calorimeter simulation.
- Prototype Chips expected in November.

Layout : 14 bit DAC & SAR ADC (2010)

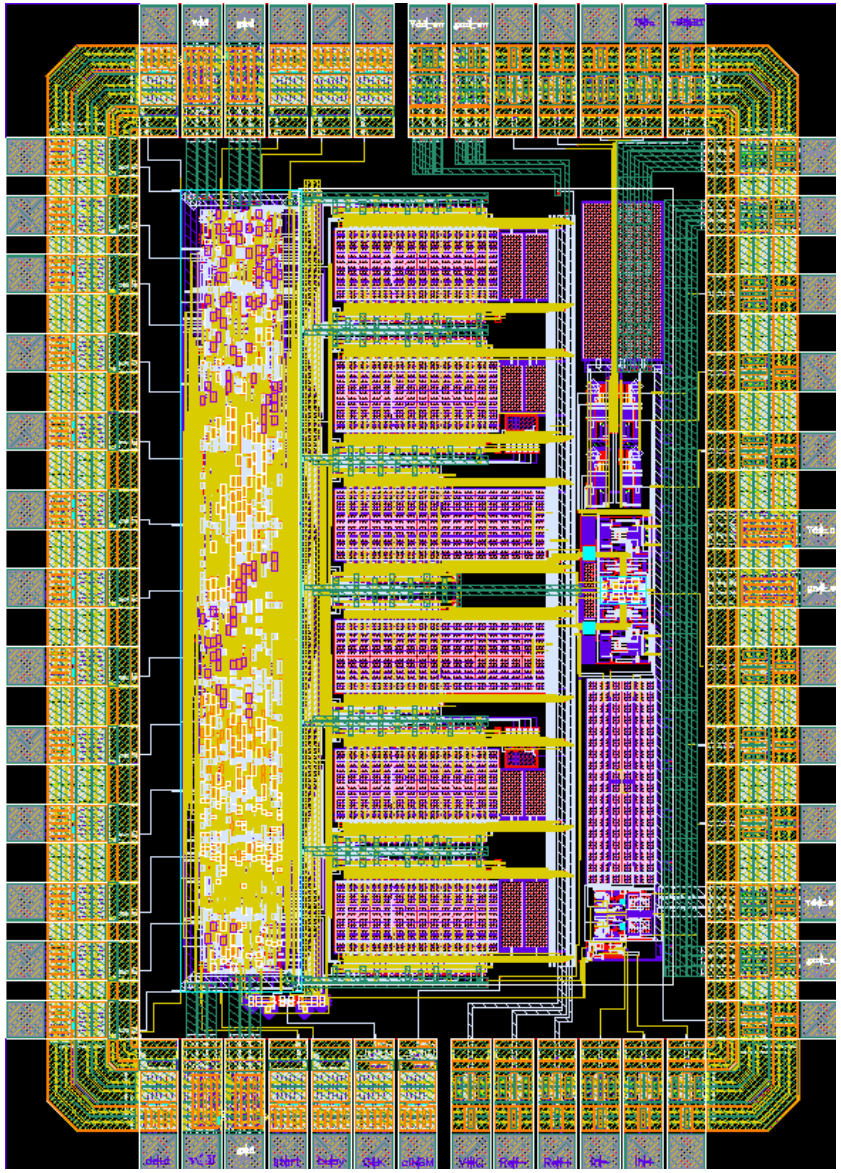
CMOS 0.35µm

Vdd = 3.3 V

Active area : 2.0 x 1.2 mm^2

Expected features with 14 bits:

- ADC Fs > 1 MS/s
- DAC Fs > 15 MS/s
- Power < 20mW; 8mW(DC)
- Idle mode : < 1µW



PROS AND CONS for SAR ADC

- Depends less on the matching;
- The reference voltages do not impact on the linearity.
- We have already good results from the DAC

- It is less power effective than the pipe line.

- RESULTS FOR THIS SAR => after November