

SDHCAL ASU board and HARDROC production test bench

Production issues towards the 1m³ SDHCAL
technological prototype

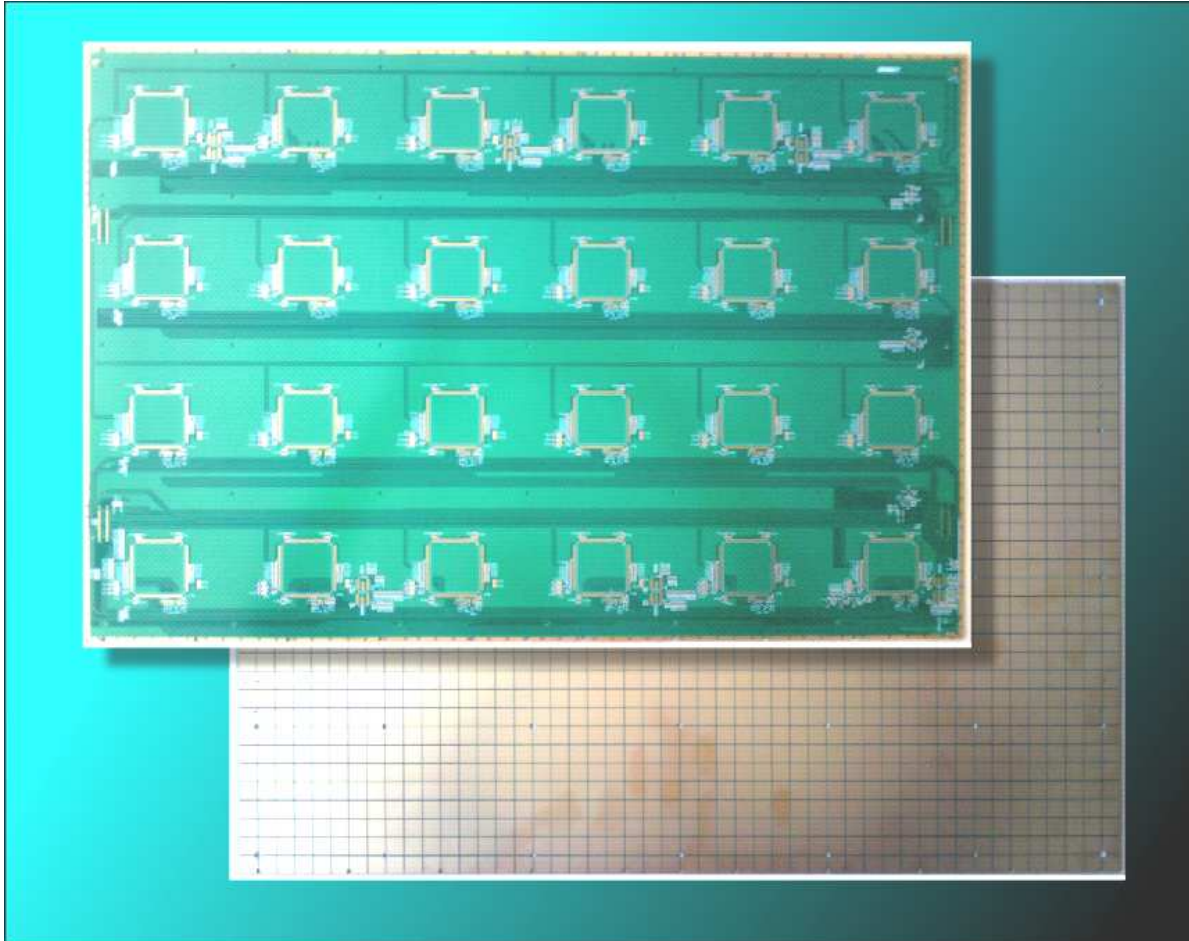
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in collaboration with the LAL Orsay

Presentation outline

- Active Sensor Unit electronics board
 - reminder
 - interconnections for the 1m³ technological prototype
 - version 3 of the ASU board
- HARDROC2 production test bench
 - brief presentation
 - preliminary results
- project status

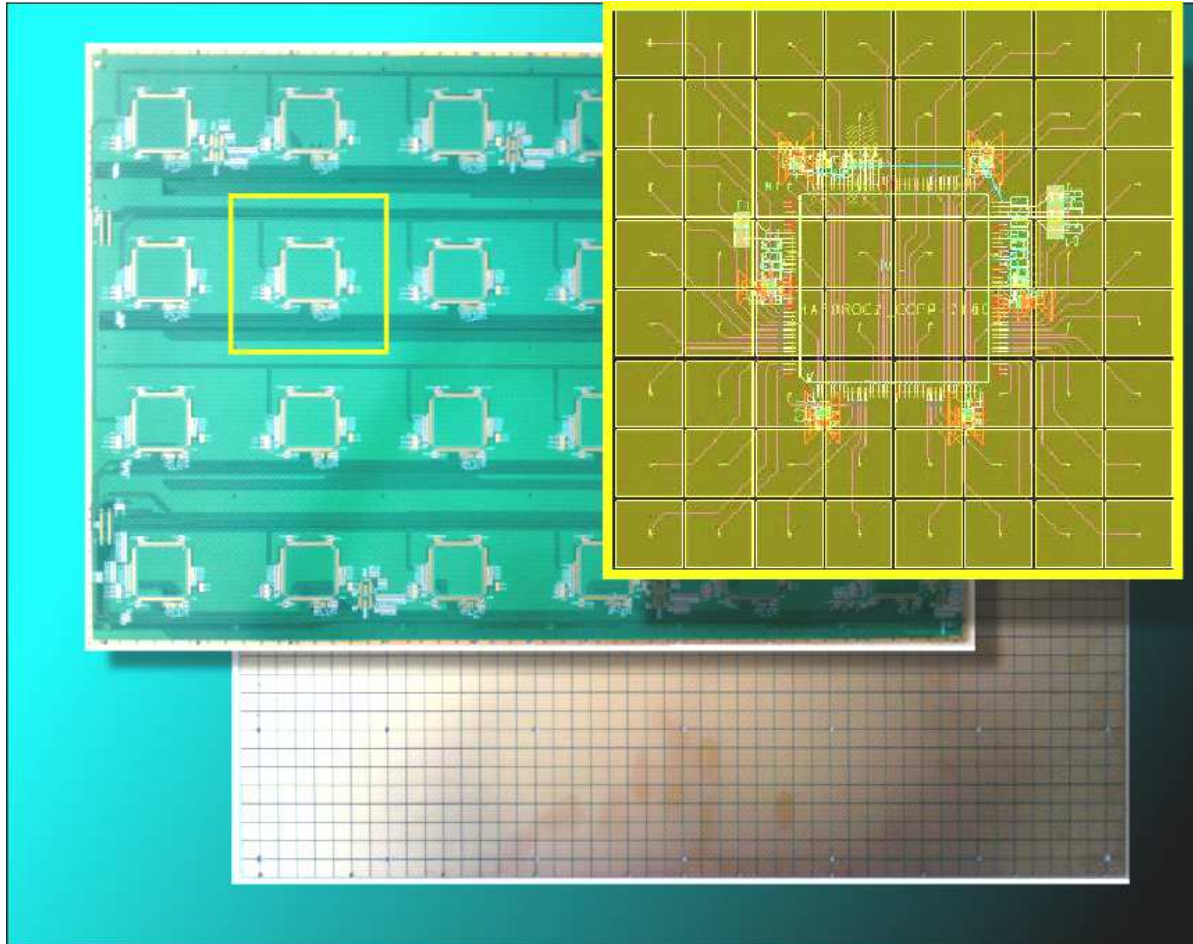
The ASU board: a reminder



Main characteristics:

- 8 layers w/ blind vias
- 24 HARDROC2b
- 64 pads/ASIC
- 1,2mm max thickness
(1,4 w/ components)
- 1/6th of square meter
- testability

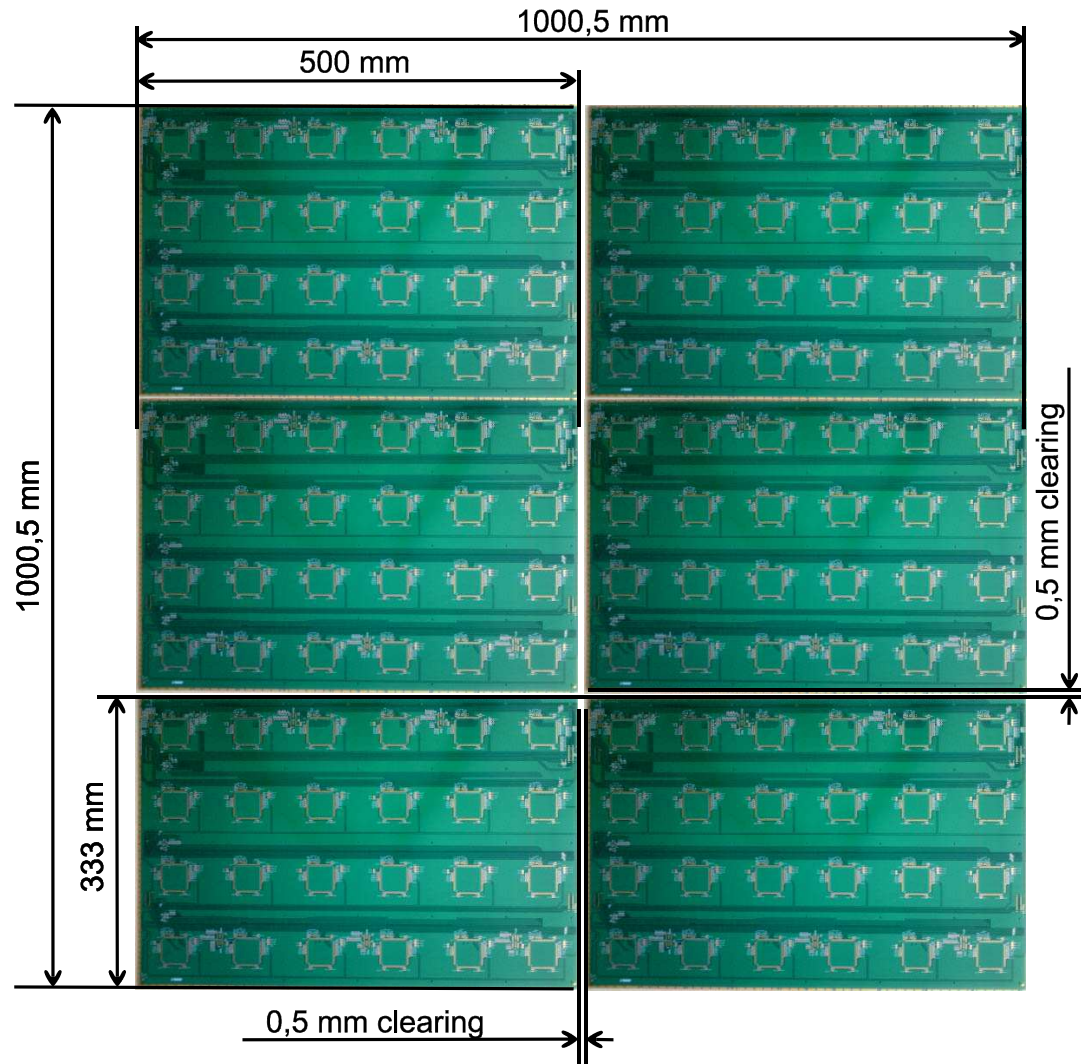
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The square meter PCB



- single GND plane:
 - soldered copper braid on board's outlines
- signals cross two ASUs board in the same slab
- leftmost ASU board in each slab connected to a DIF
- use of interconnection boards:
 - ASU-ASU
 - DIF-ASU
- testability issue:
 - only one type of ASU board

The ASU board: design issues

DIF-ASU

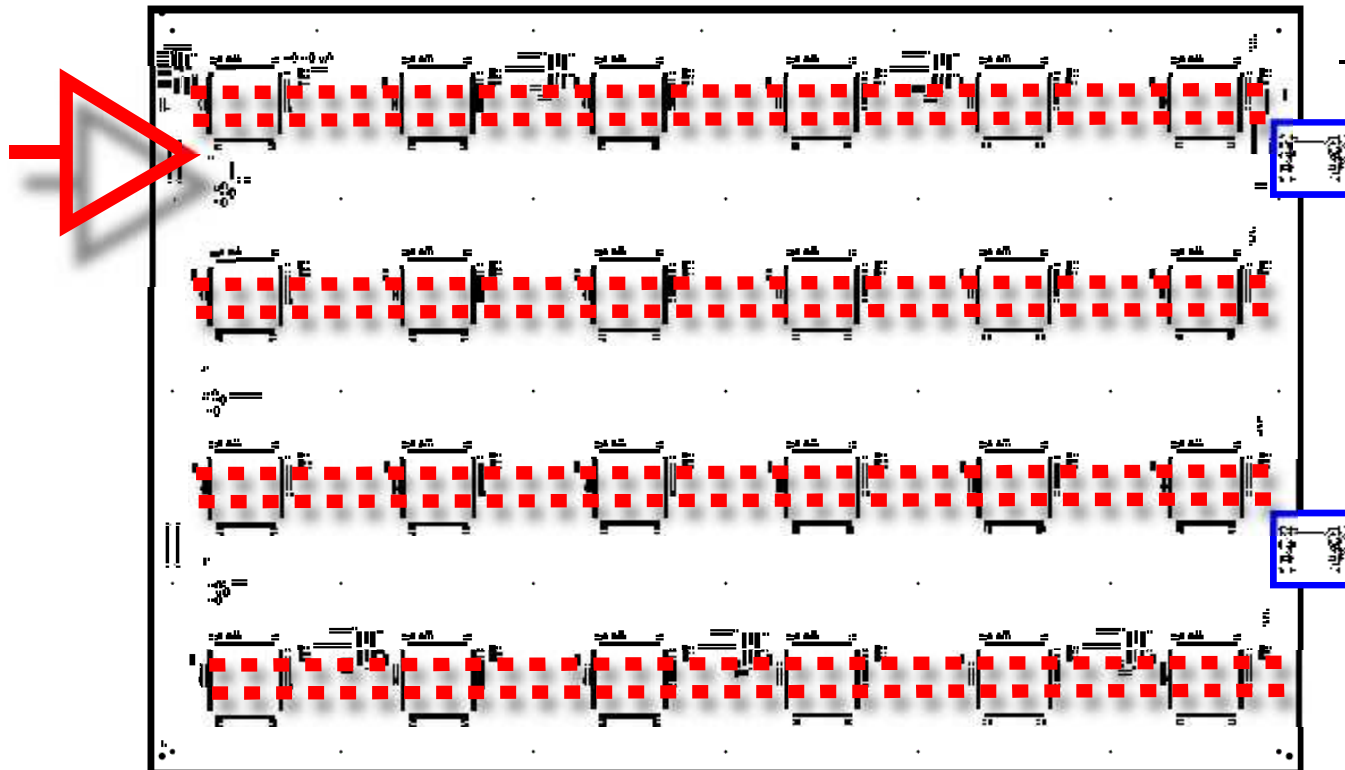
- flex-rigid design
- active board (LVDS and slowctrl lines buffering)



The ASU board: design issues

DIF-ASU

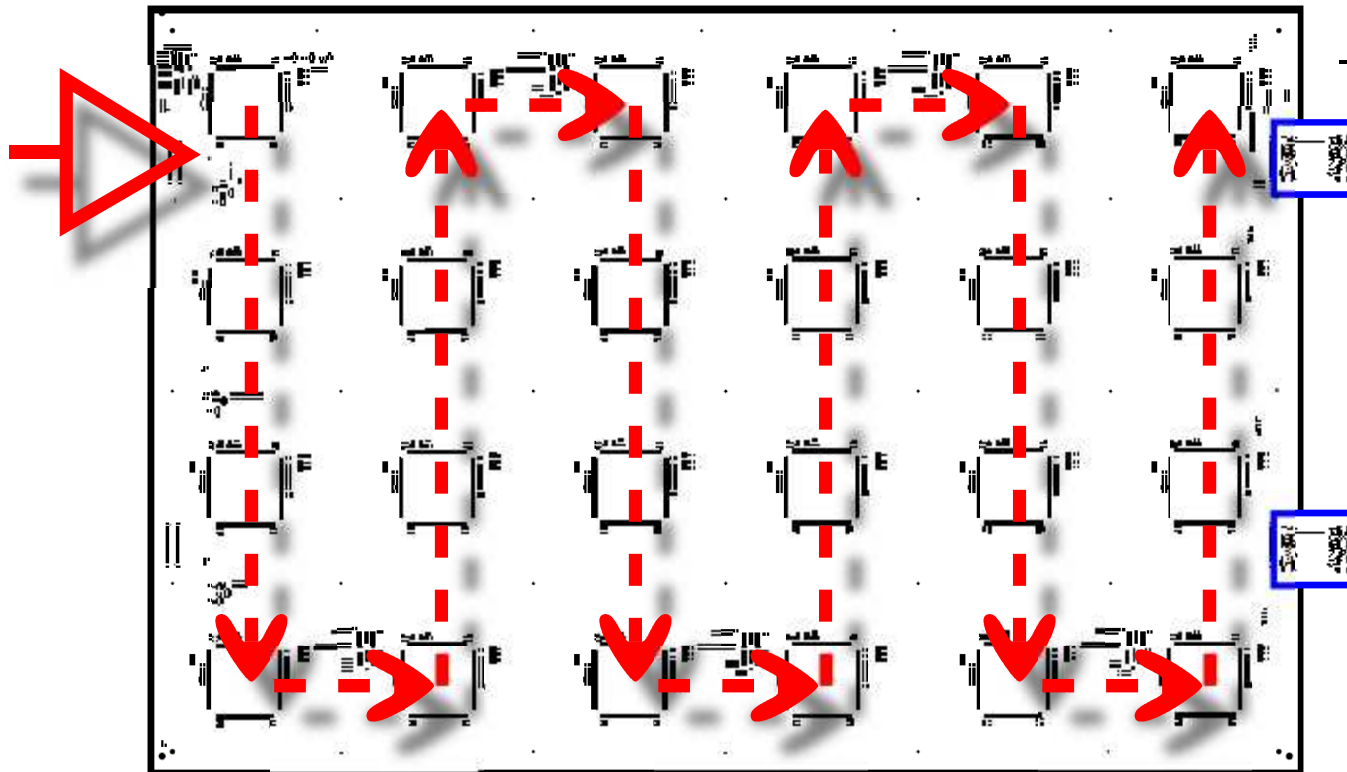
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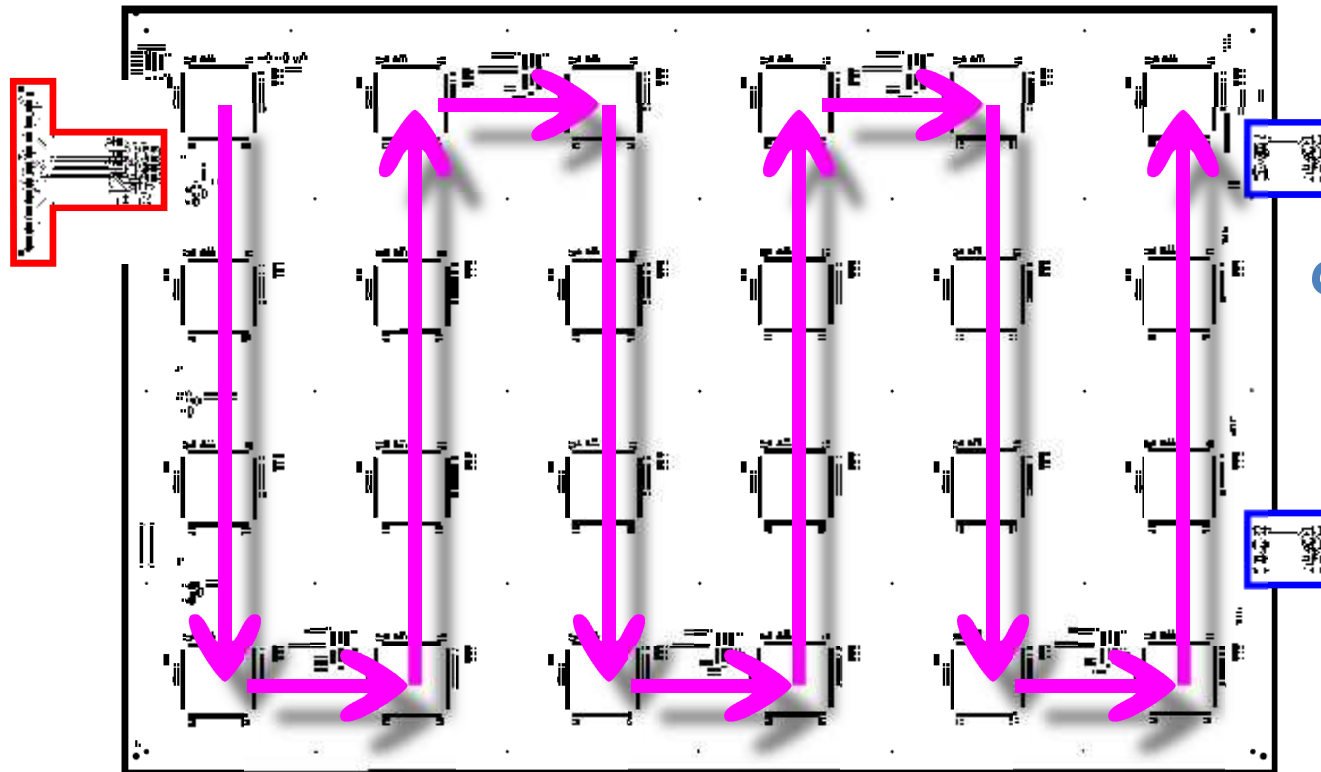
The ASU board: design issues

DIF-ASU

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The ASU board: design issues



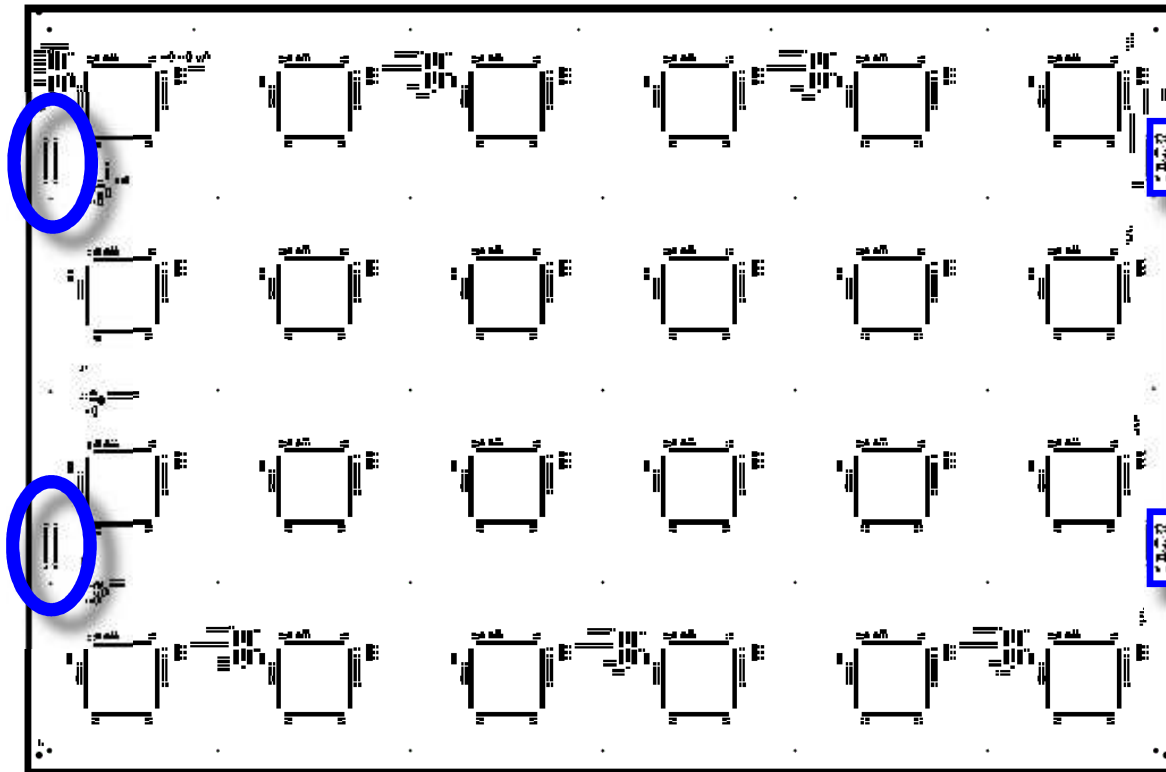
DIF-ASU

- flex-rigid design
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digital (SR) signals

- serial chaining of all HARDROCs

The ASU board: design issues



DIF-ASU

- flex-rigid design
- active board (LVDS and slowctrl lines buffering)

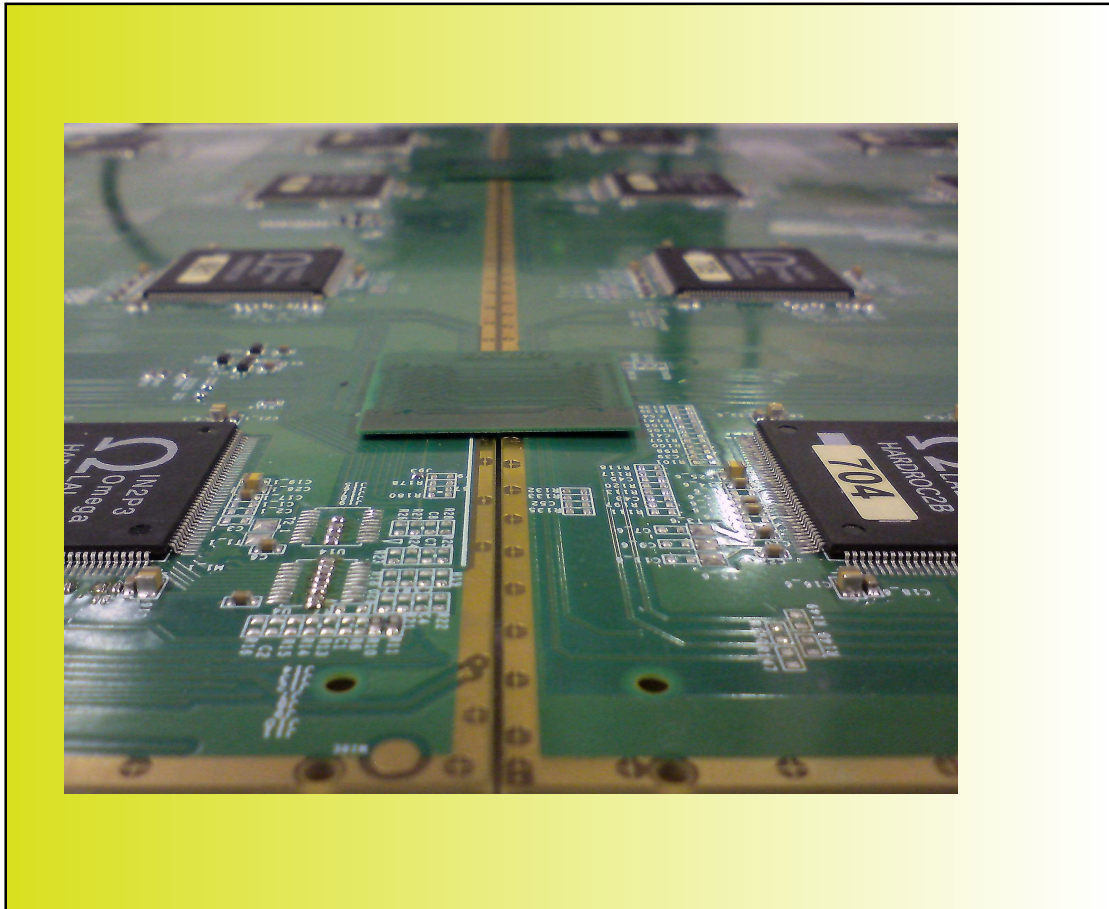
digital (SR) signals

- serial chaining of all HARDROCs

ASU-ASU

- board-to-board interconnect
- same connectors as in DIF-ASU

Interconnection issues: KYOCERA board-to-board connector

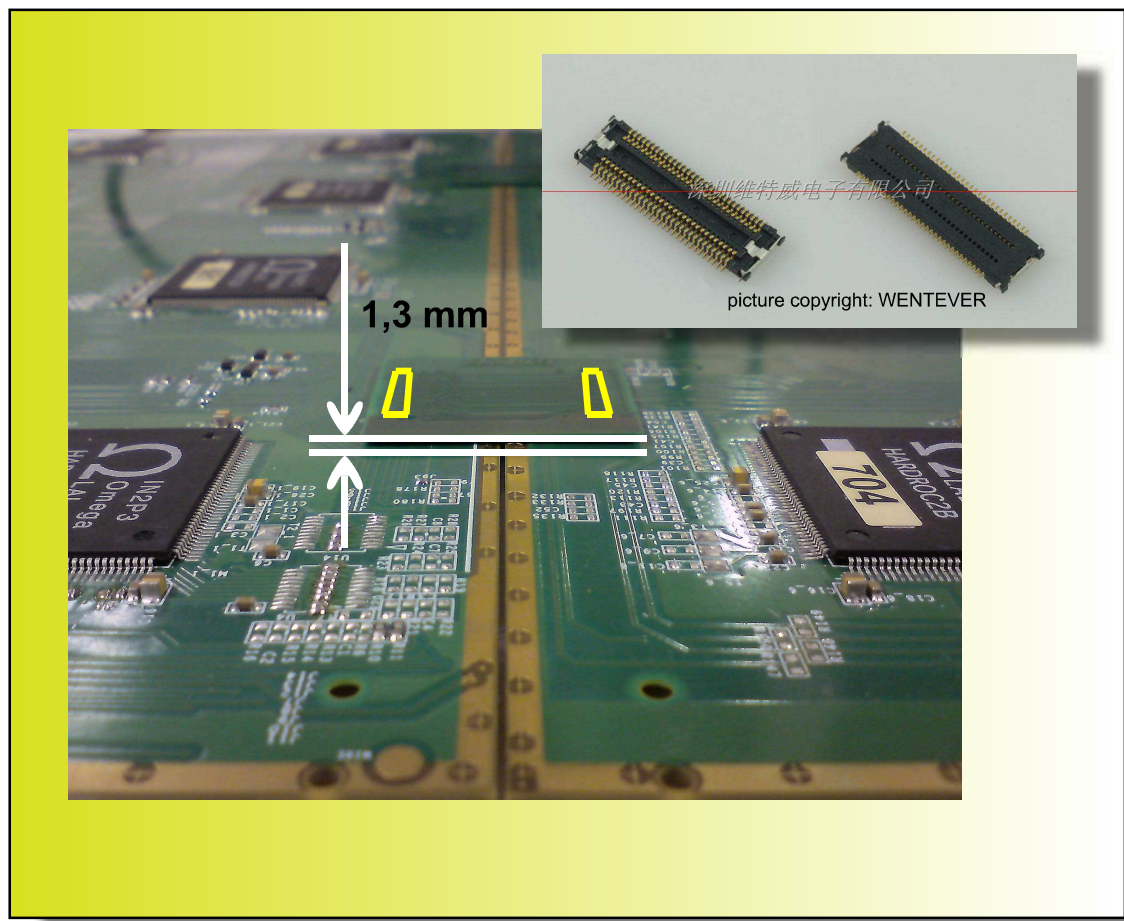


KYOCERA 5801

(ASU-ASU shown)

- same used in ECAL
- 80 pins
- 0,4 mm pitch
- 0,8 mm stacking height
- 1,3 mm thickness
when assembled
- allows the continuity of
the GND soldering

Interconnection issues: KYOCERA board-to-board connector

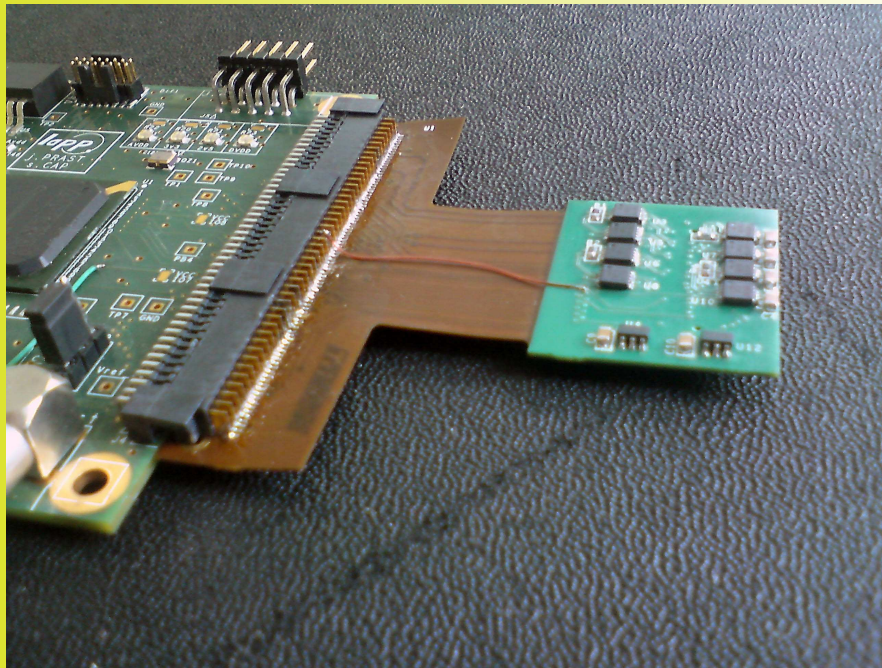


KYOCERA 5801 (ASU-ASU shown)

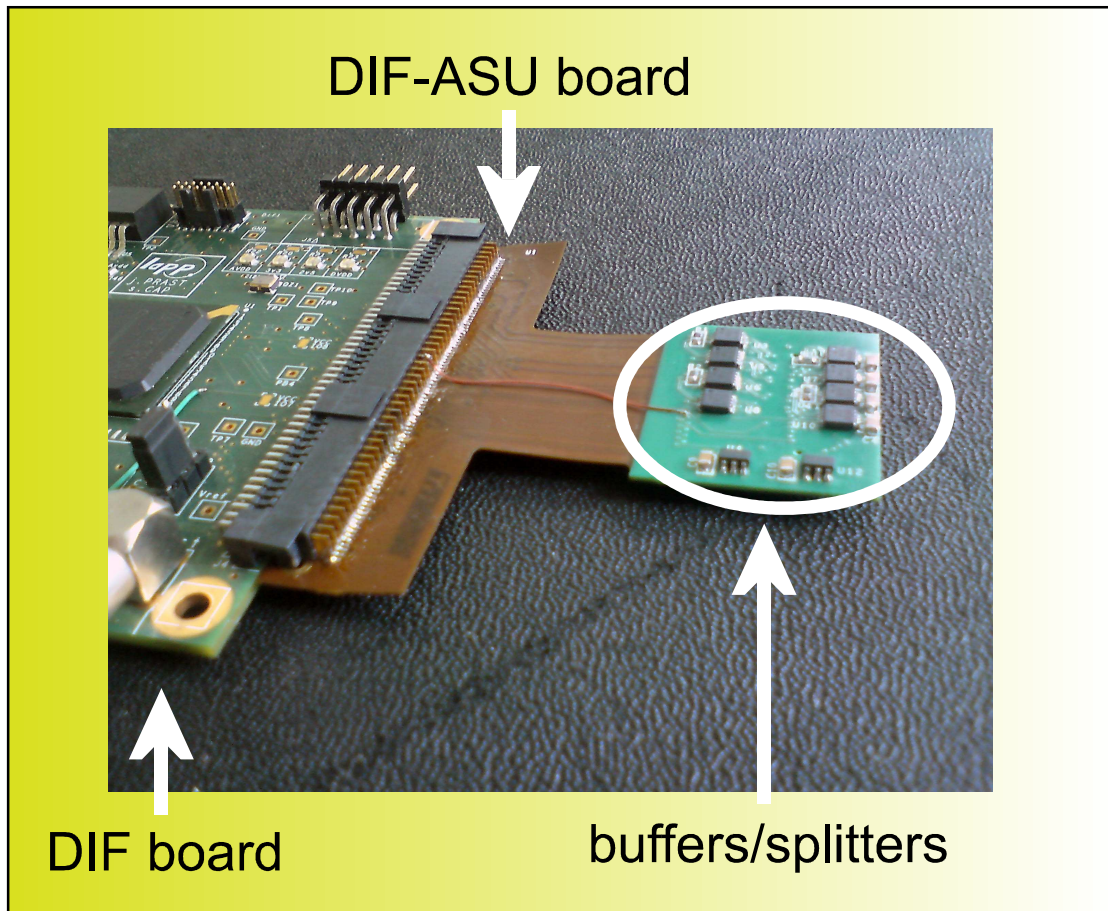
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Interconnection issues: DIF-ASU board

reliability problem in
first prototype

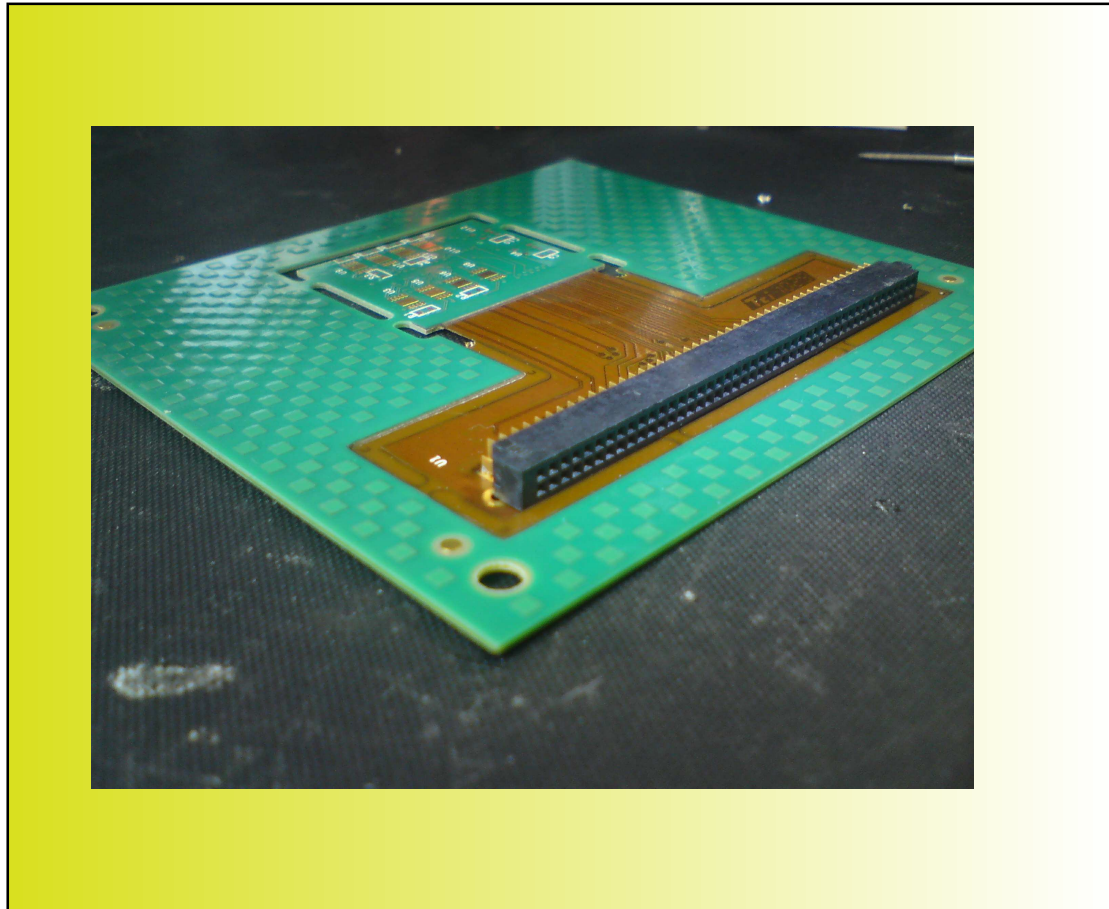


Interconnection issues: DIF-ASU board



reliability problem in first prototype
 investigation traced back the problem to the use of the SAMTEC connector on the flex part of the board

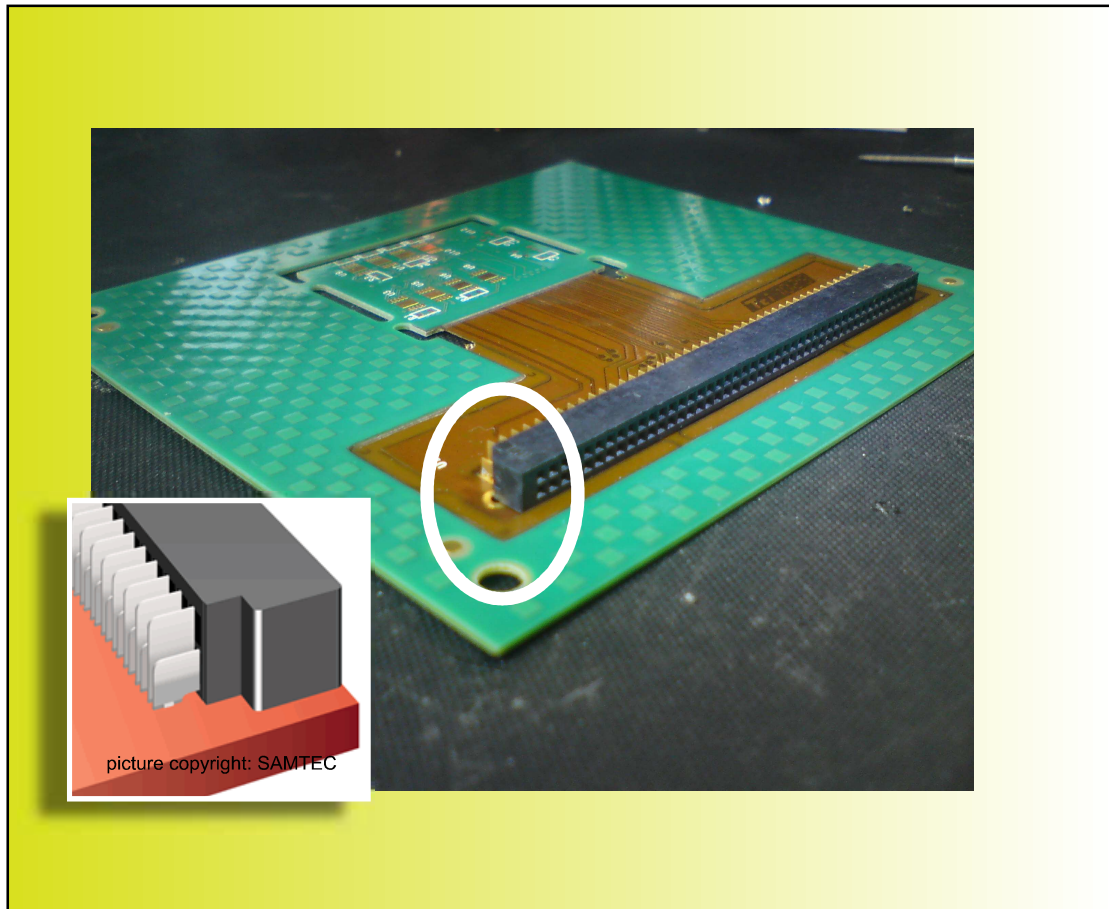
Interconnection issues: SAMTEC (DIF) connector



SAMTEC SFMH (DIF-ASU shown)

- 90 pins
- 0,64 mm pitch
- reliability issues when mounted on kapton

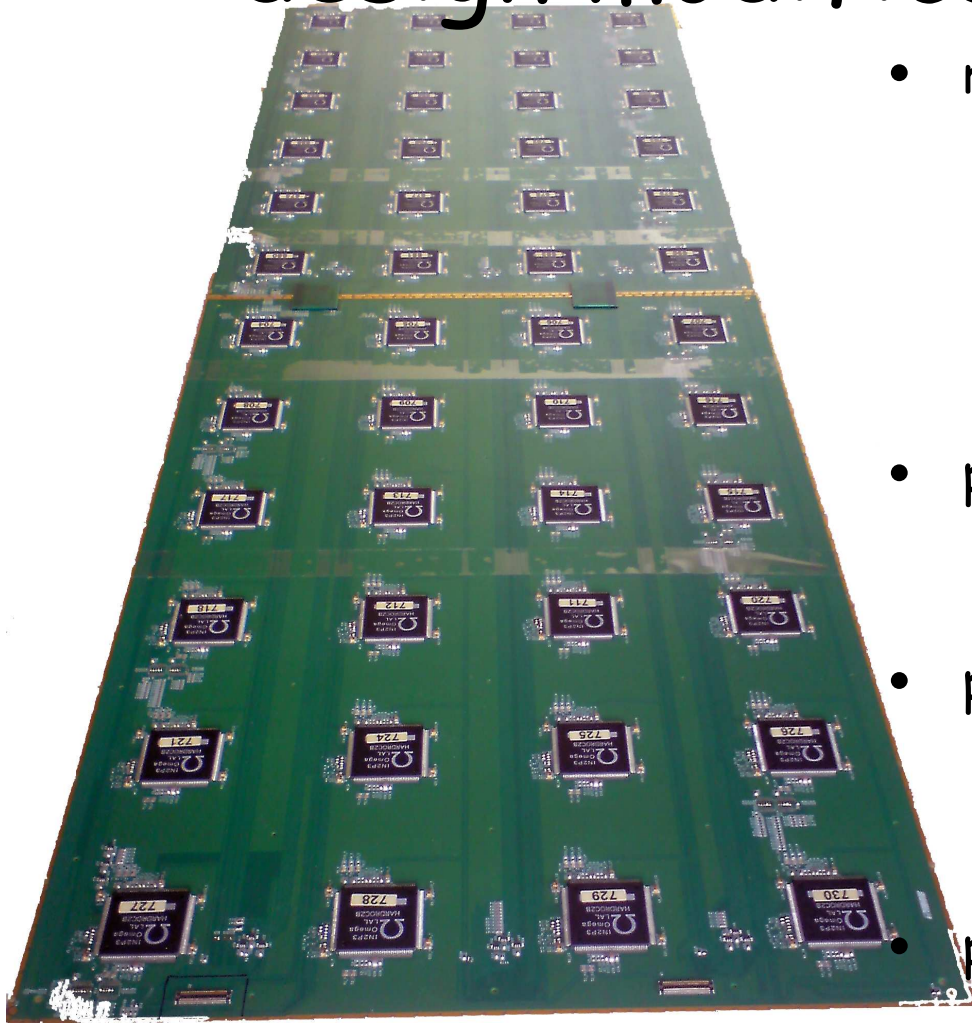
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SAMTEC SFMH (DIF-ASU shown)

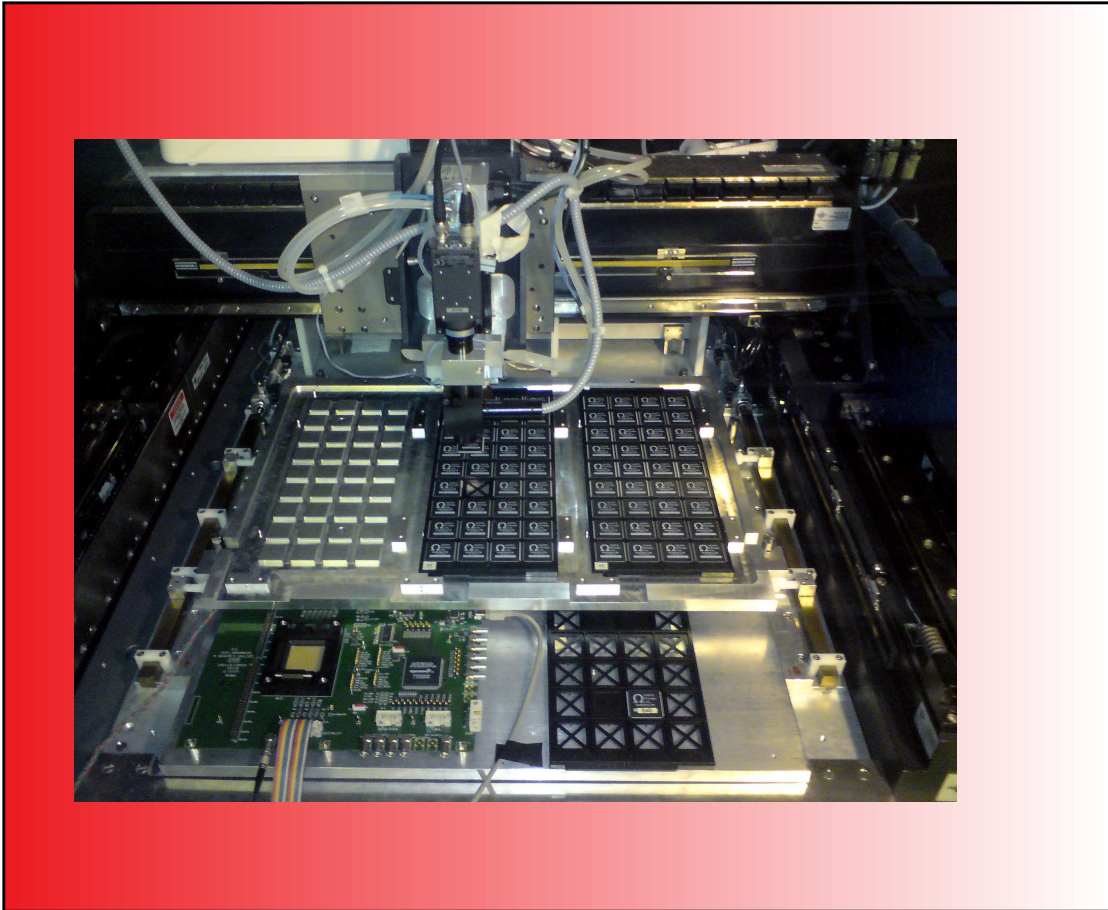
- 90 pins
- 0,64 mm pitch
- reliability issues when mounted on kapton

ASU board version 3: design modifications wrt V2



- reliability driven:
 - interconnection boards for signals crossings
 - use of KYOCERA connectors
 - copper layers optimization for better board planarity
- production driven:
 - holes opening along the outline:
 - ease the GND soldering step
- power consumption driven:
 - LVDS buffers with pwr down:
 - buffers are switched ON only during power pulsing
- project status:
 - ASU V3 mature for production

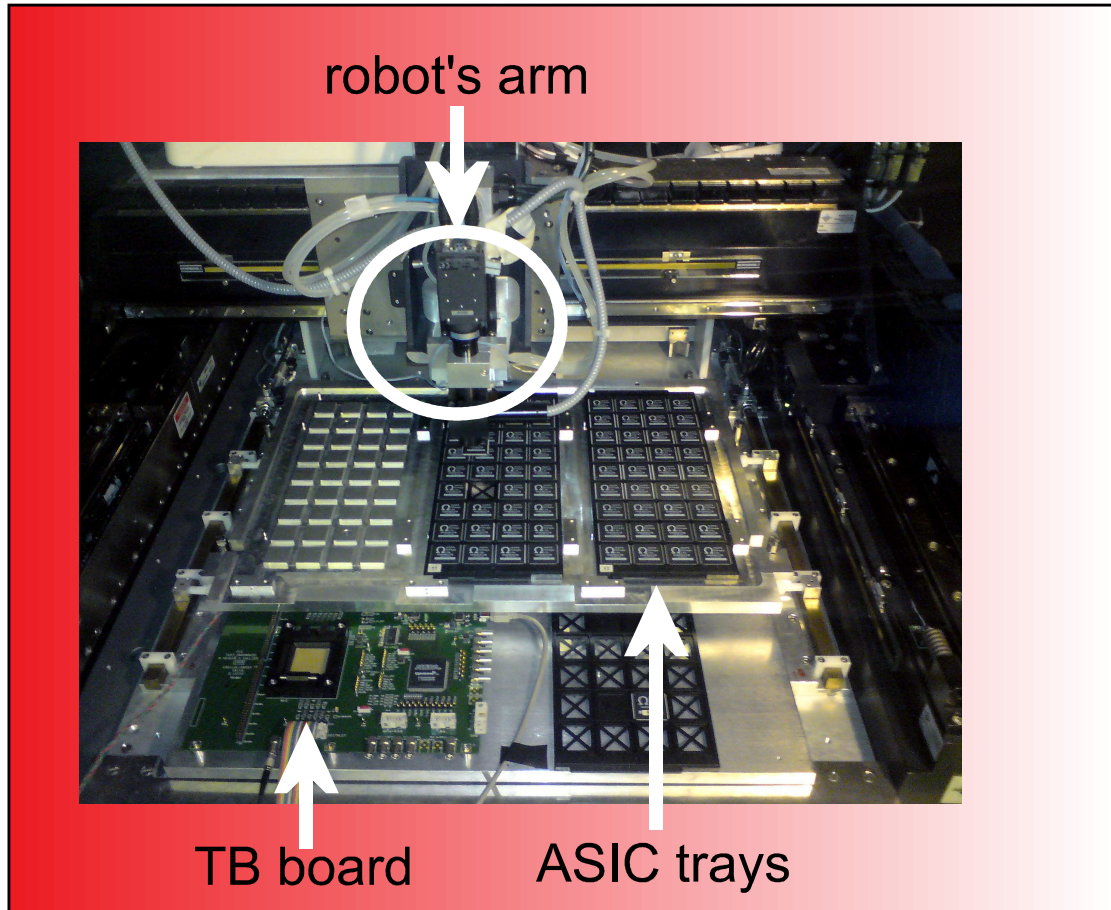
HARDROC2 production test bench



gantry robot fully operative

- 4 axes pick and place operation

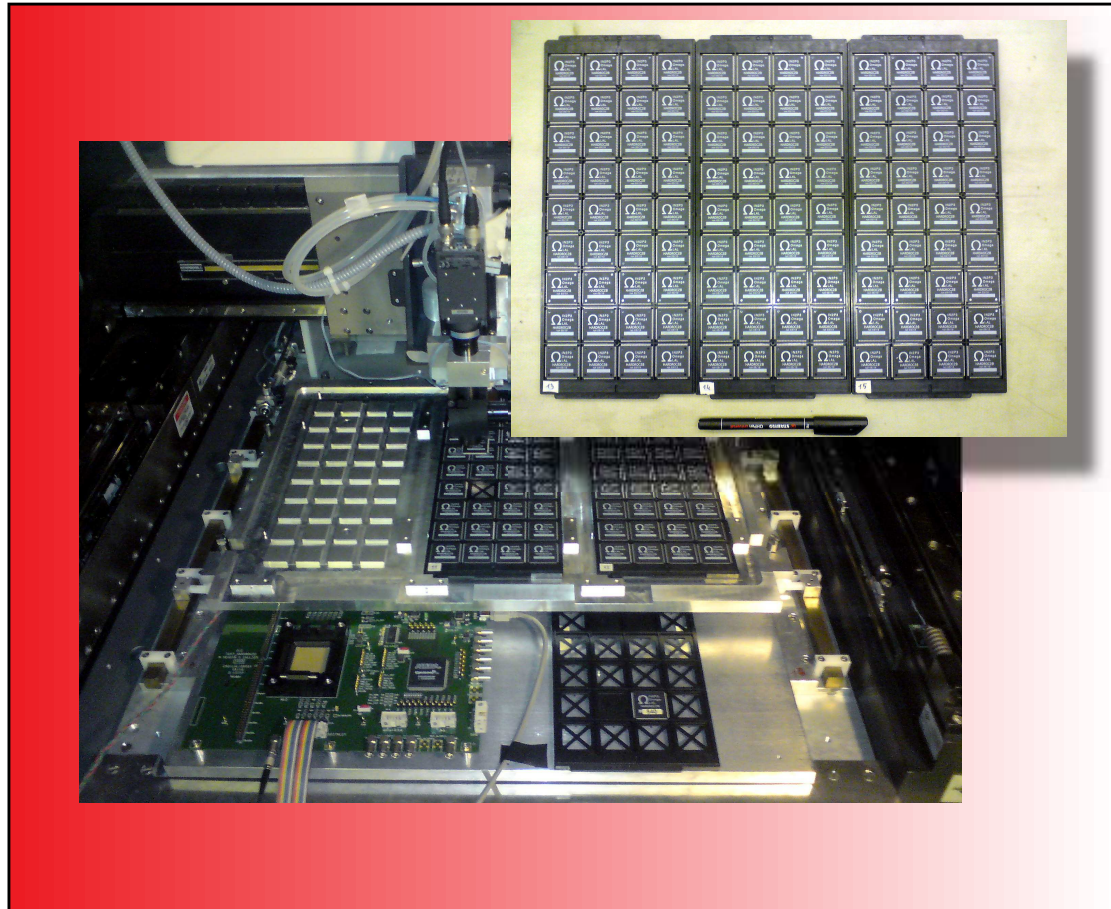
HARDROC2 production test bench



gantry robot fully operative

- 4 axes pick and place operation
- alu base design

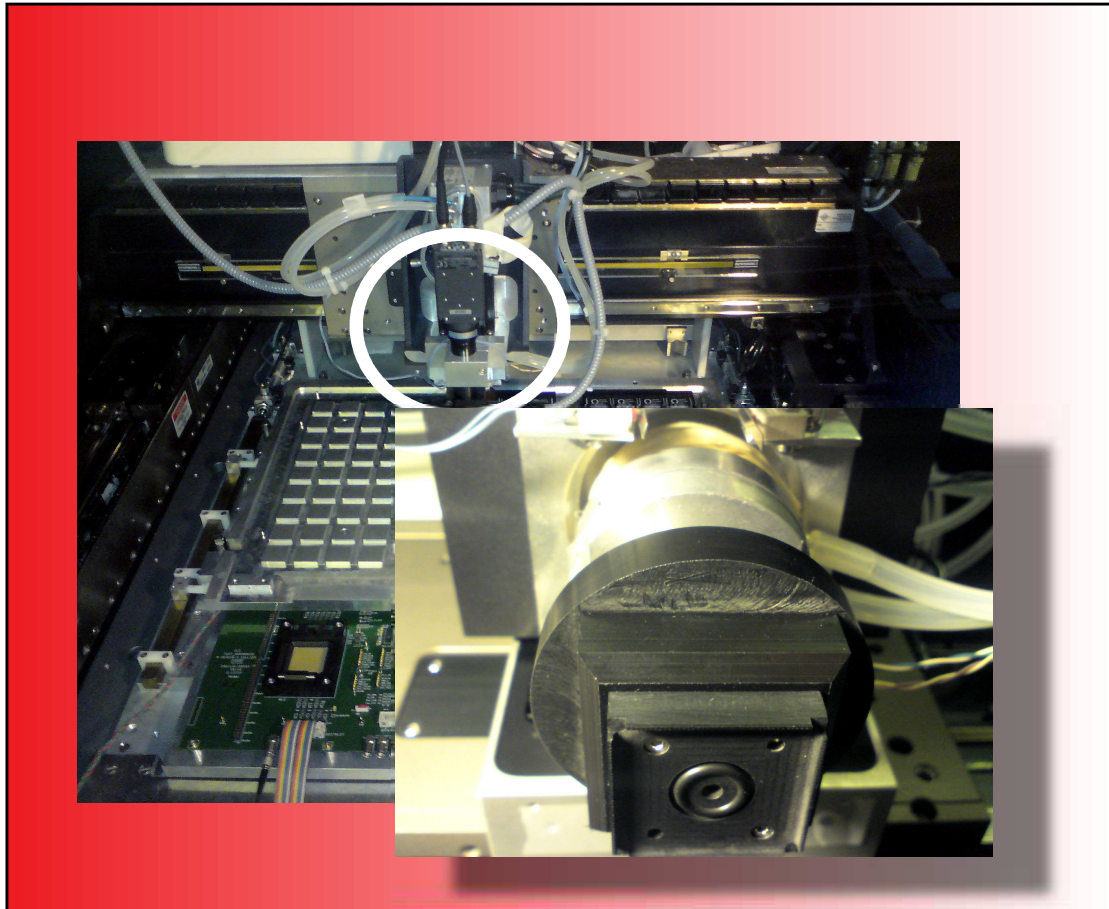
HARDROC2 production test bench



gantry robot fully operative

- 4 axes pick and place operation
- alu base design
- 3 trays/batch
 - less than 10m/HR
 - 108 HRs in ~ 17 hours
 - 540 HRs / week

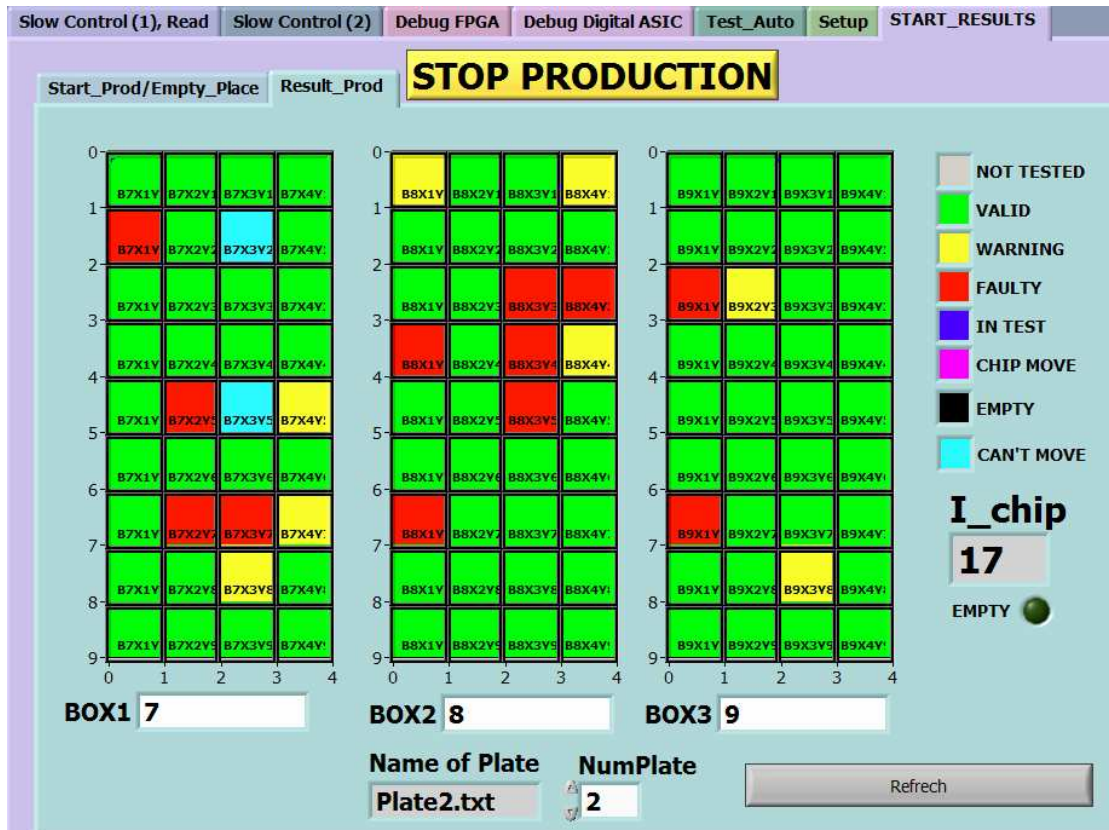
HARDROC2 production test bench



gantry robot fully operative

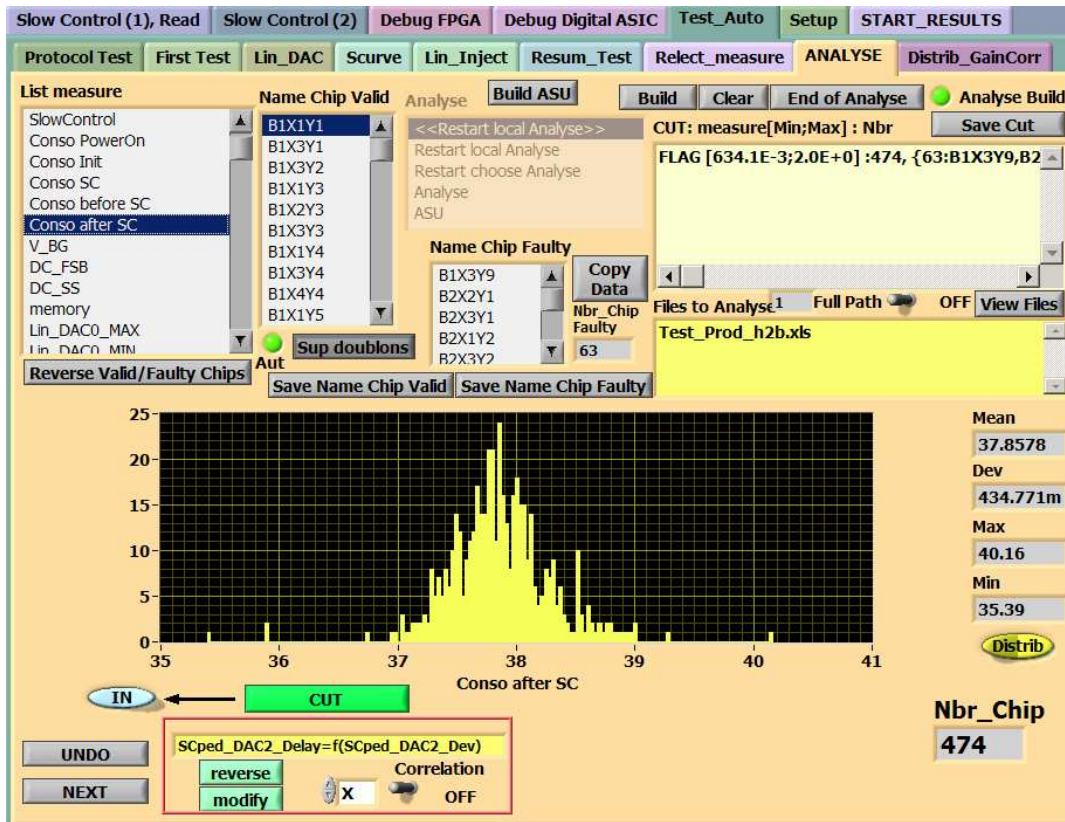
- 4 axes pick and place operation
- alu base design
- 3 trays/batch
 - less than 10m/HR
 - 108 HRs in ~ 17 hours
 - 540 HRs / week
- socket pressure pad
 - adapted for use with the robot
 - O-ring added for vacuum pump operation

HARDROC2 production test bench



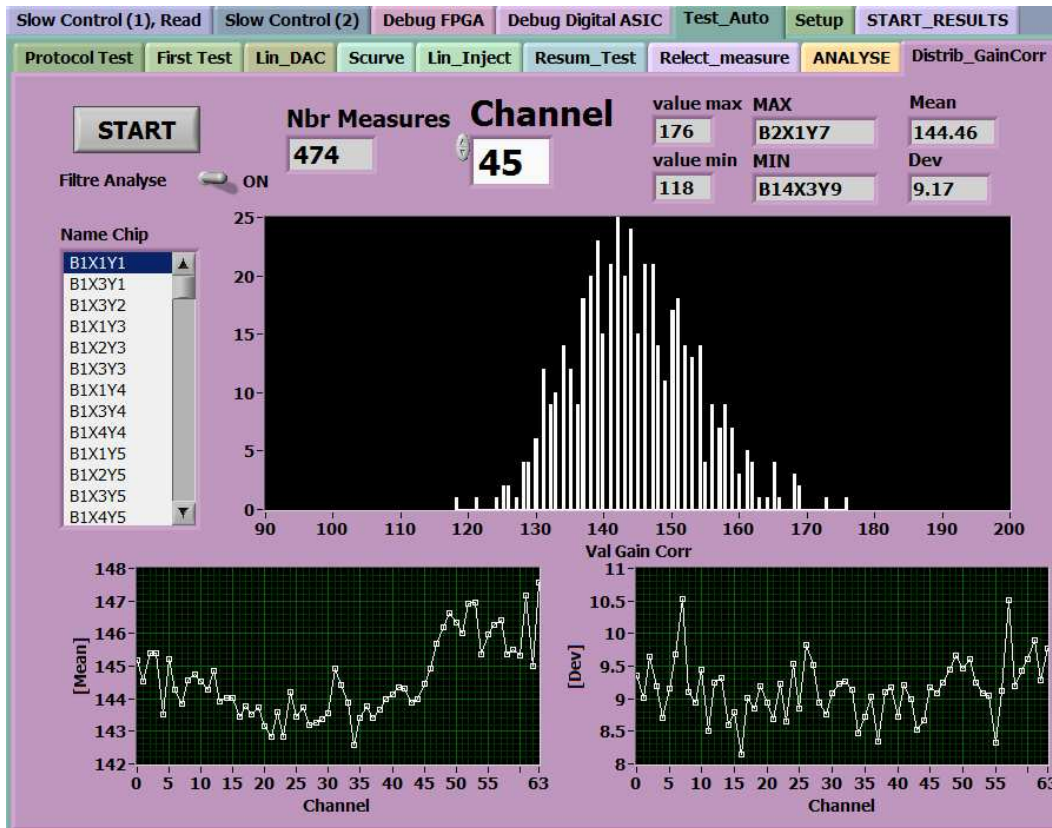
LABVIEW based s/w
– fully automated (batch)

HARDROC2 production test bench



- LABVIEW based s/w
- fully automated (batch)
 - status display + measurements windows
 - statistical analysis available for the full production

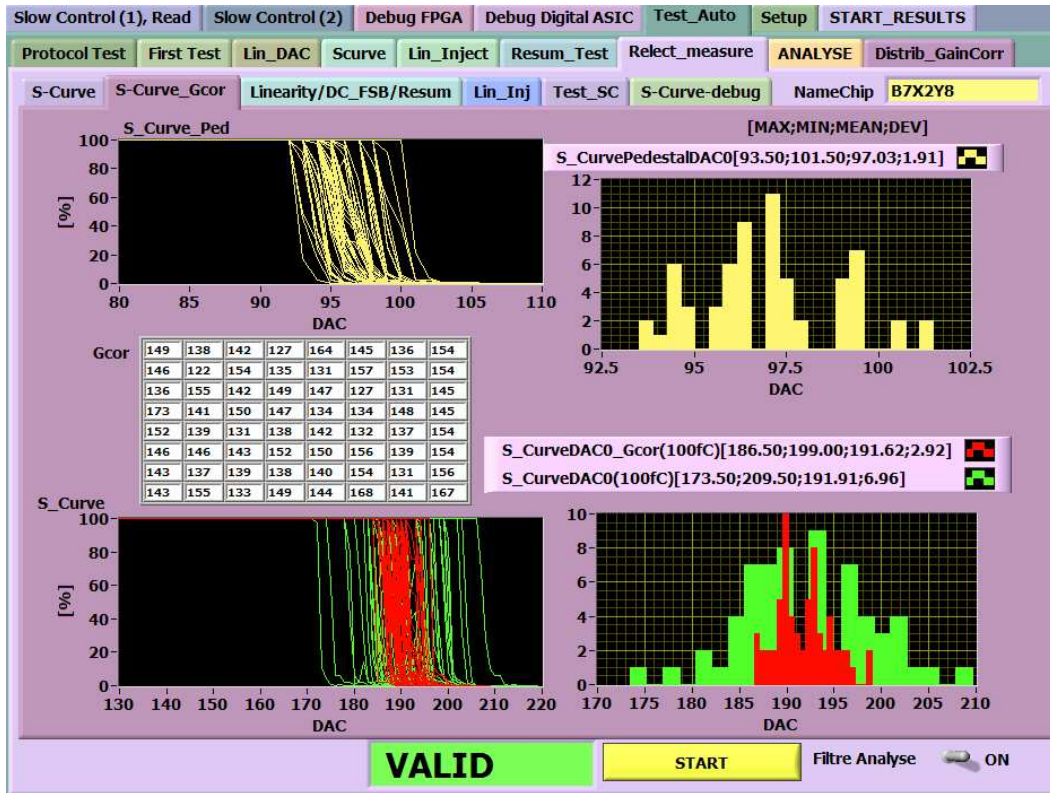
HARDROC2 production test bench



LABVIEW based s/w

- fully automated (batch)
- status display + measurements windows
- statistical analysis available for the full production
- TB features:
 - HR gain correction

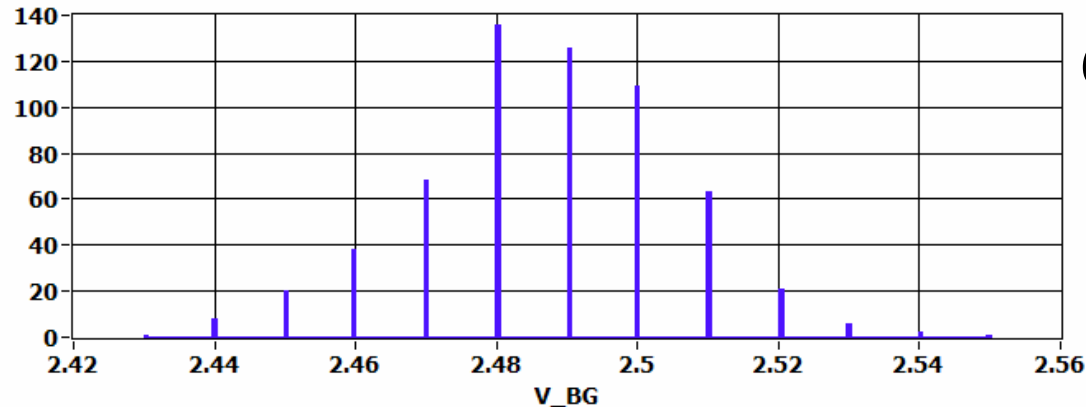
HARDROC2 production test bench



LABVIEW based s/w

- fully automated (batch)
- status display + measurements windows
- statistical analysis available for the full production
- TB features:
 - HR gain correction
 - trigger efficiency
 - S-curves
 - DAC linearity
 - SC load
 - HR internal memory

HARDROC2 production test bench: preliminary results



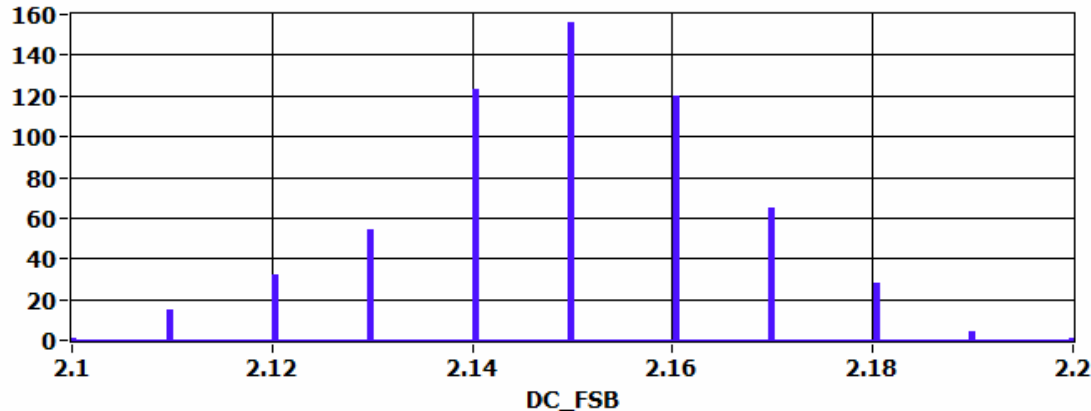
676 HARDROCs tested

- < 10% total production
- 77 faulty chips ("raw" figure)

- bandgap voltage

Num:600 Chips
Mean:2.487 V
Dev:18.23 mV
Max:2.55 V
Min:2.43 V

HARDROC2 production test bench: preliminary results

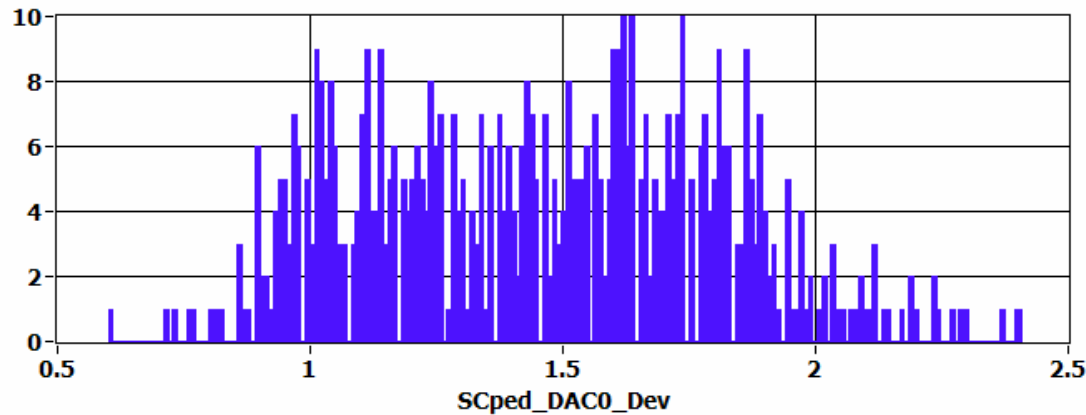


676 HARDROCs tested

- < 10% total production
- 77 faulty chips ("raw" figure)
- bandgap voltage
- **FSB0 baseline**

Num:600 Chips
Mean:2.149 V
Dev:16.41 mV
Max:2.2 V
Min:2.1 V

HARDROC2 production test bench: preliminary results

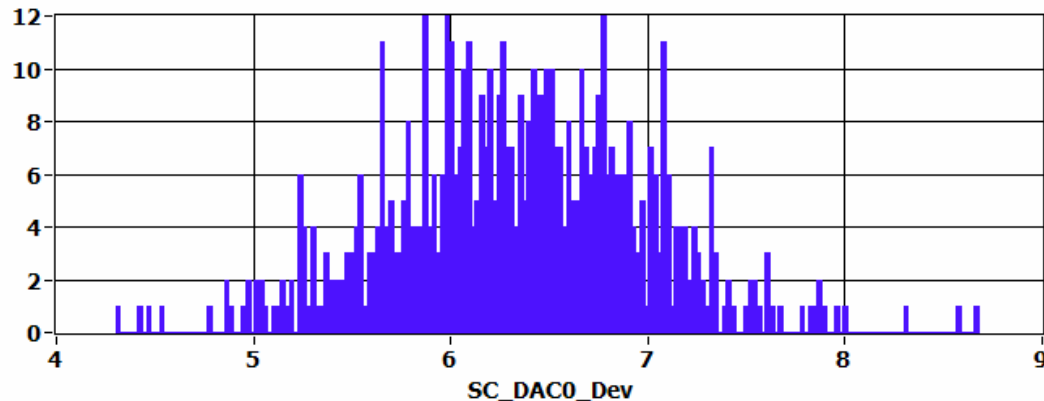


Num:600 Chips
Mean:1.46 V
Dev:0.35 V
Max:2.41 V
Min:0.6 V

676 HARDROCs tested

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- bandgap voltage
- FSBO baseline
- **Dev [S-Curve Pedestal DAC0] : 64 Ch**

HARDROC2 production test bench: preliminary results

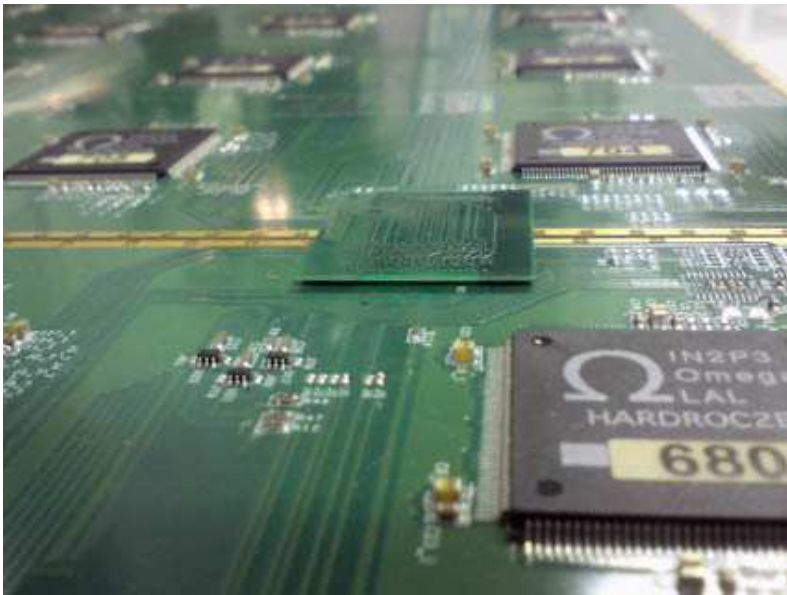


Num:600 Chips
Mean:6.34 dac
Dev:0.65 dac
Max:8.67 dac
Min:4.3 dac

676 HARDROCs tested

- < 10% total production
- 77 faulty chips ("raw" figure)
- bandgap voltage
- FSBO baseline
- Dev [S-Curve Pedestal DAC0] : 64 Ch
- **Dev [S-Curve 100fC DAC0] : 64 Ch**

Conclusions



- 1 complete V3 slab under test
- boards (and interconnects) for 1m² available on week 42
 - prototypes intended for design validation (electrical + mechanical)
- reliability problem on DIF-ASU:
 - design modified and sent to fab
 - prototypes available by week 42
- good level of confidence with fabs
 - TECH-CI (PCB fabrication)
 - KEP-ES (component assembly)
 - CCTP almost ready
- HARDROC2 production test bench
 - software and gantry robot fully functional
 - more than 600 chips already tested