AHCAL Electronics.

integration status and open issues

Mathias Reinecke
CALICE main meeting
Univ. HASSAN II, Casablanca, Morocco
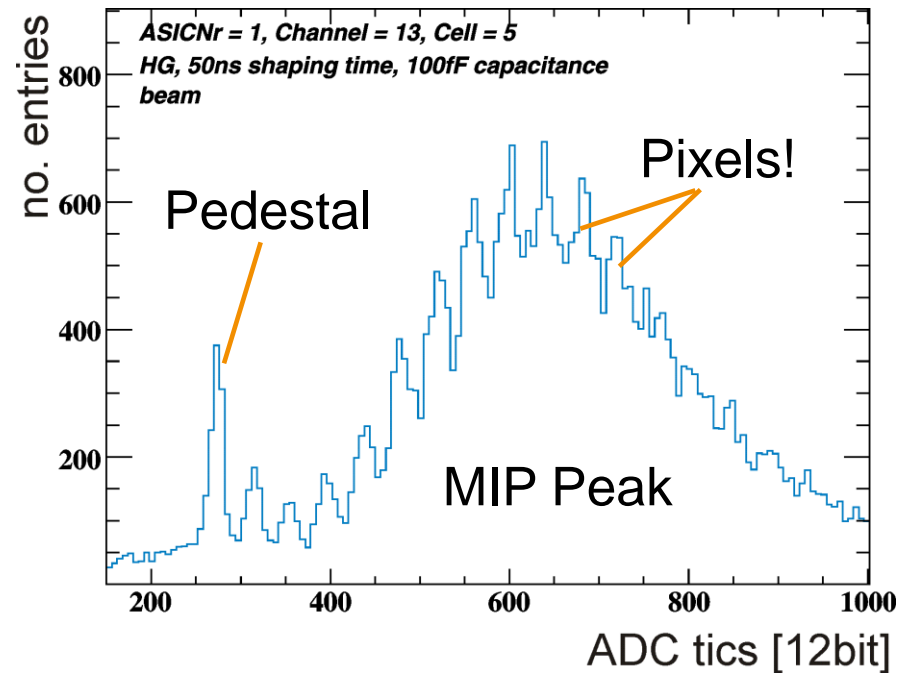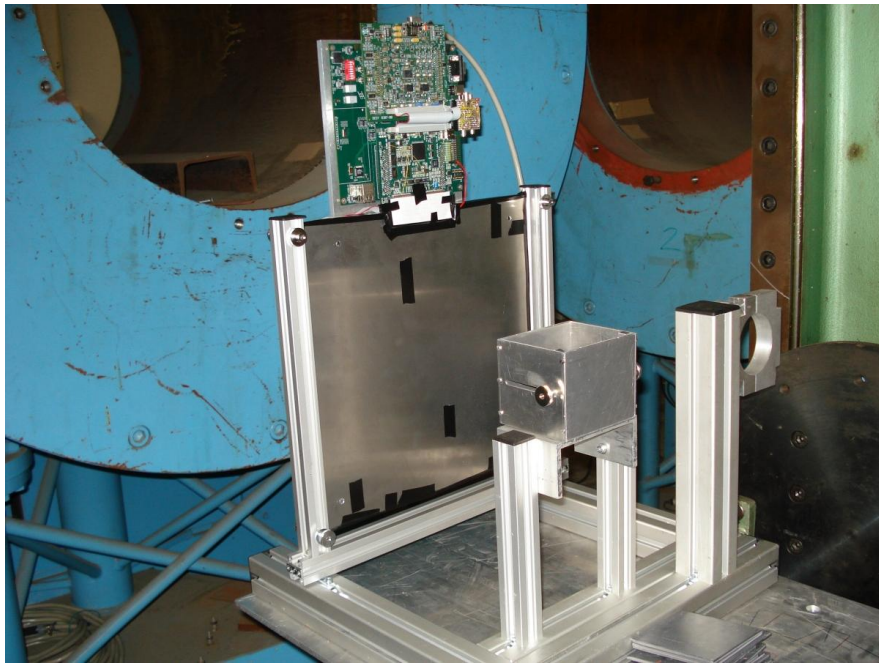Sept. 23rd, 2010

Outline

> ## Status Electronics / Hamburg Activities

- Testbeam Setup (HBU_II)
- Laboratory Setup (HBU_I)

> ## Next Generation (Full Layer EUDET Module)

- Status Redesigns Boards (DESY)
- Tiles
- LED Systems for Calibration

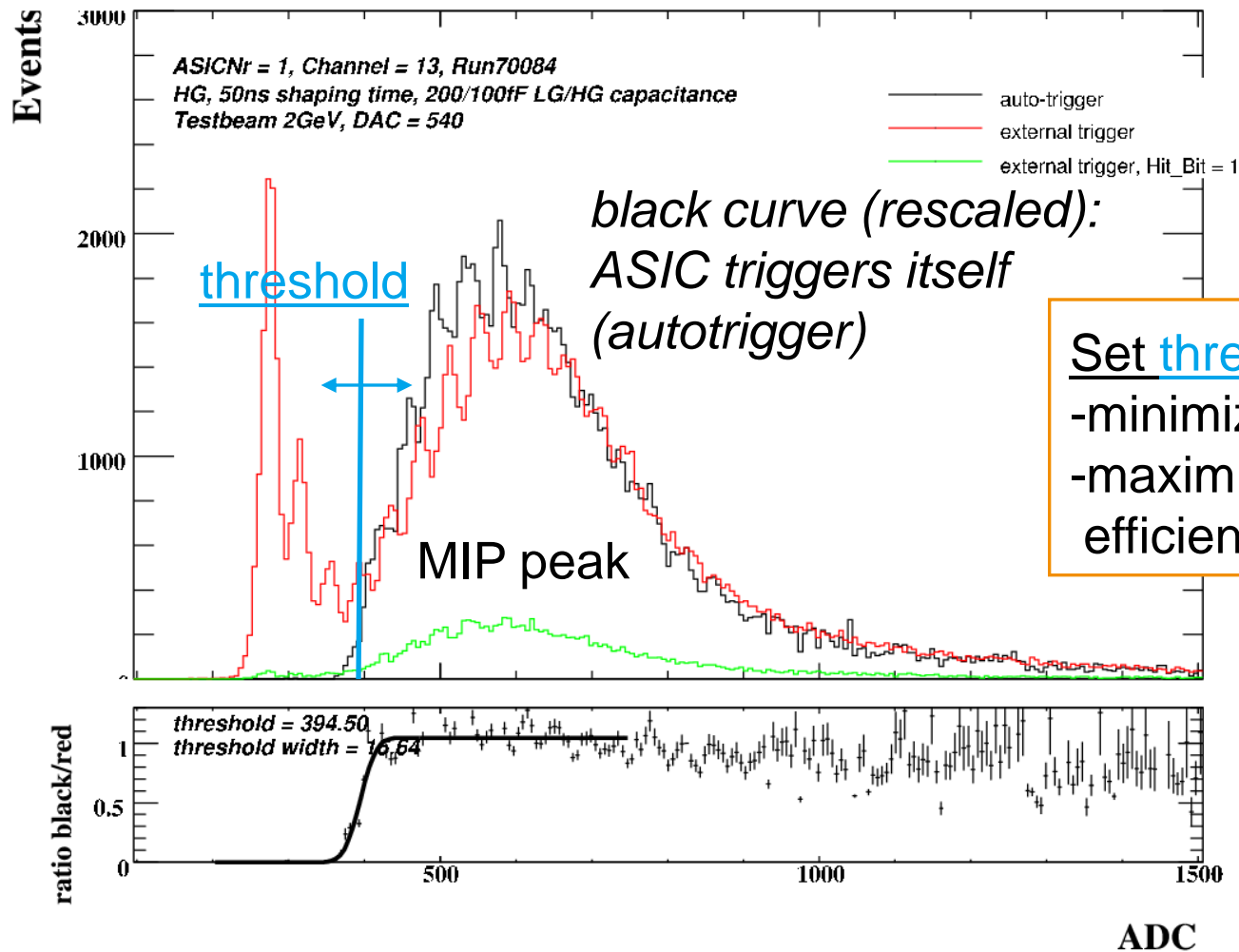> ## Status DAQ / Discussion about CALICE DAQ

> ## Conclusion

DESY Testbeam Setup – HBU_II
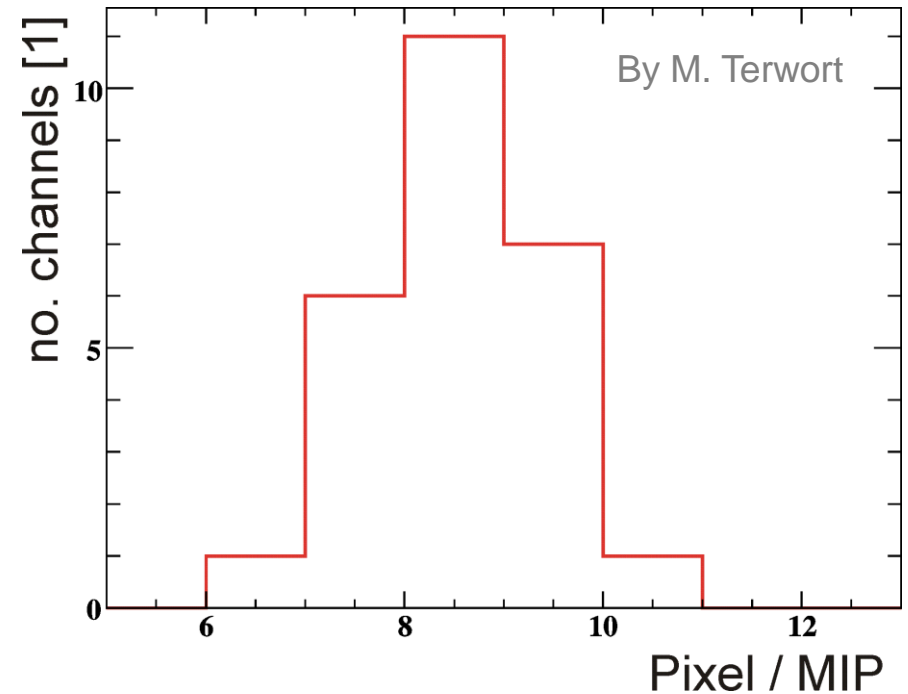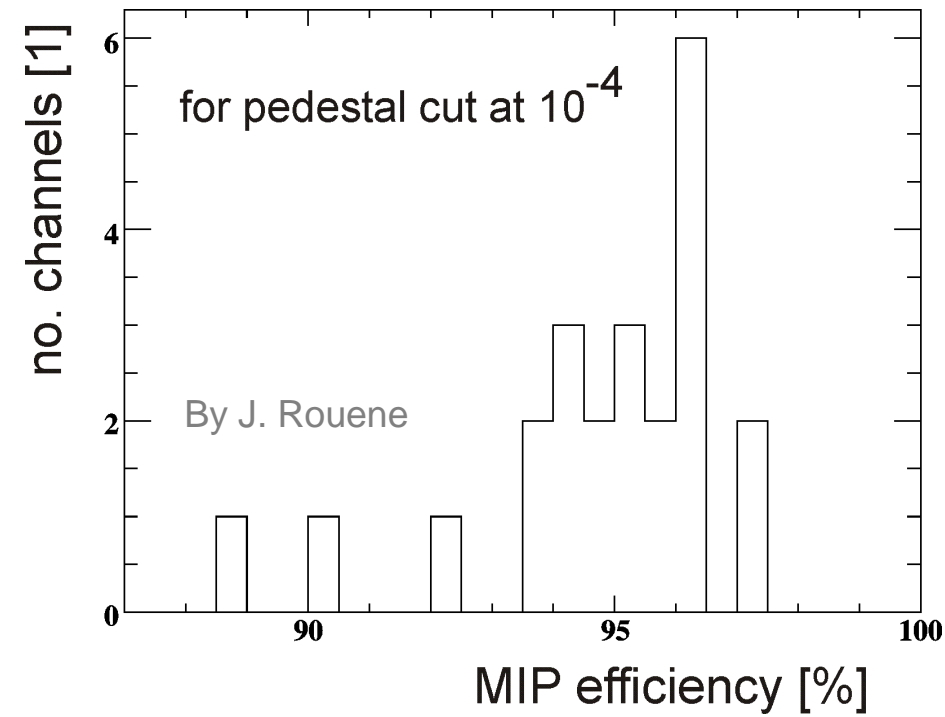

> DESY 6GeV electron Testbeam operation: Setup optimization, Channel-wise calibration with MIPs: **Mark Terwort**

> Integrated LED System, uniformity studies / optimiz.: **U. Wuppertal**

DESY Testbeam - Autotrigger

black curve (rescaled):
ASIC triggers itself
(autotrigger)

threshold

MIP peak

Set threshold to:
-minimize noise hits (10^-4)
-maximize MIP detection
 efficiency

Results by
Jeremy Rouene

Testbeam – multi-channel studies

for pedestal cut at 10^{-4}

By J. Rouene

MIP efficiency [%]

By M. Terwort

Pixel / MIP

A **MIP efficiency of ~95%** can be achieved for a threshold-pedestal cut at 10^(-4) for most channels (autotrigger mode).

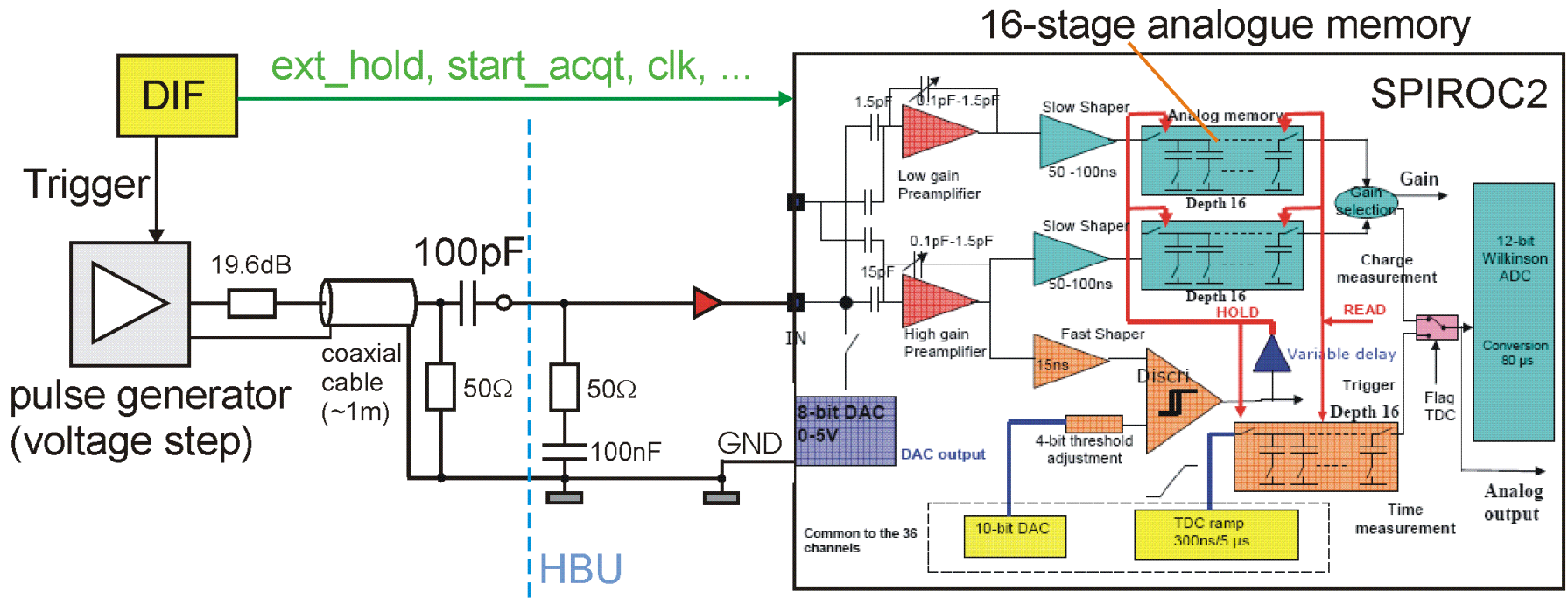Preliminary tests show a lightyield of **~8.5pixels / MIP**

DESY

Summary SPIROC2 and HBU measurements

> Autotrigger Mode of SPIROC2 under test (channelwise)

> Threshold is adjusted to optimize MIP efficiency

> Multi-channel analysis in testbeam

  - has to incorporate tile and SiPM variations

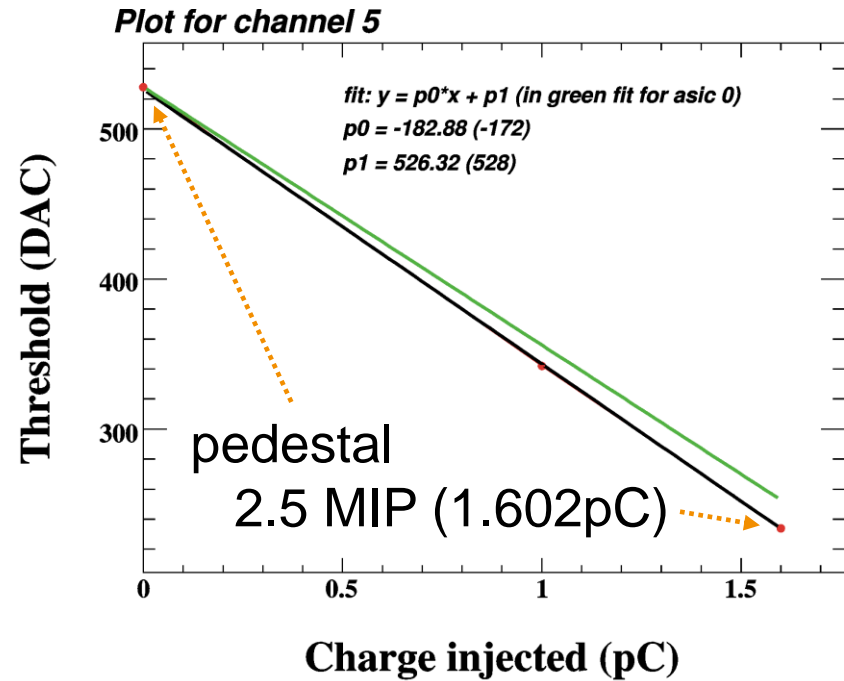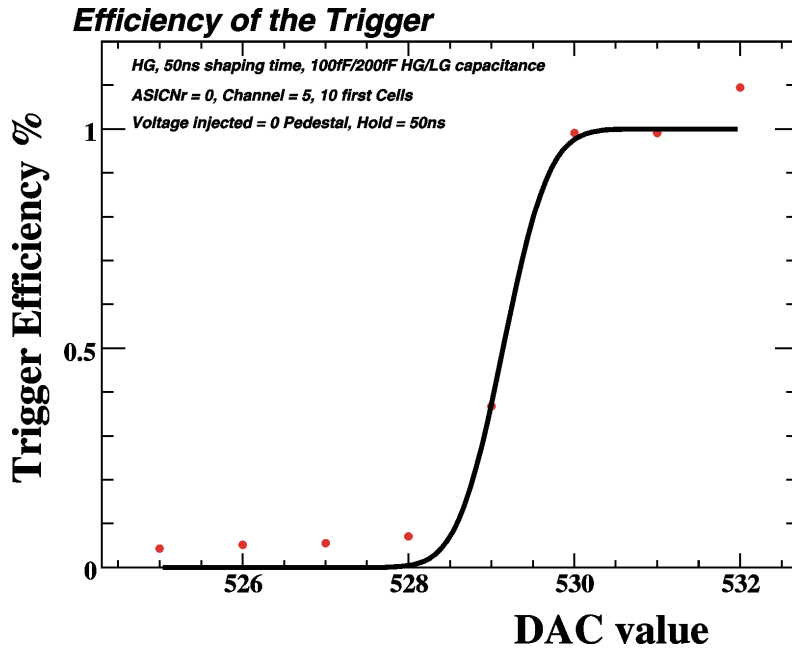> Multi-channel Autotrigger and Timing (TDC) studies to be done

Advantage of charge injection: Amount of charge well defined.

Autotrigger Threshold Adjustment

Efficiency of the Trigger

HG, 50ns shaping time, 100fF/200fF HG/LG capacitance
ASICNr = 0, Channel = 5, 10 first Cells
Voltage injected = 0 Pedestal, Hold = 50ns

Trigger Efficiency %

DAC value

Plot for channel 5

fit: y = p0*x + p1 (in green fit for asic 0)
p0 = -182.88 (-172)
p1 = 526.32 (528)

Threshold (DAC)

pedestal
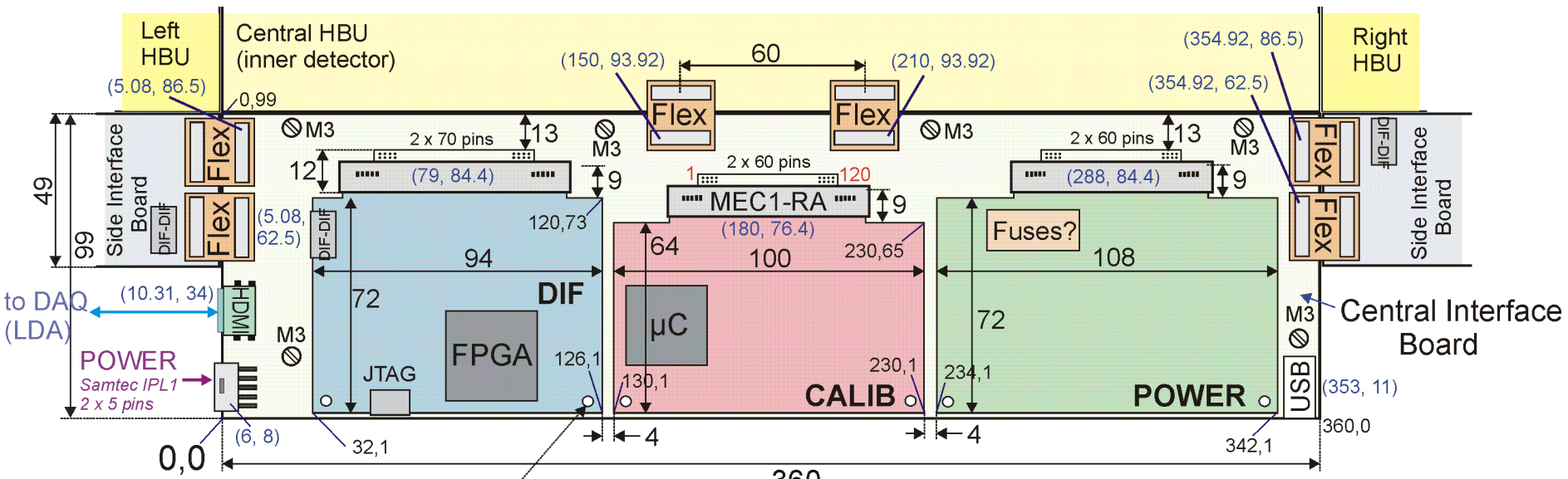2.5 MIP (1.602pC)

Charge injected (pC)

analyze threshold position (DAC setting) for different injected charges ('S-curves')

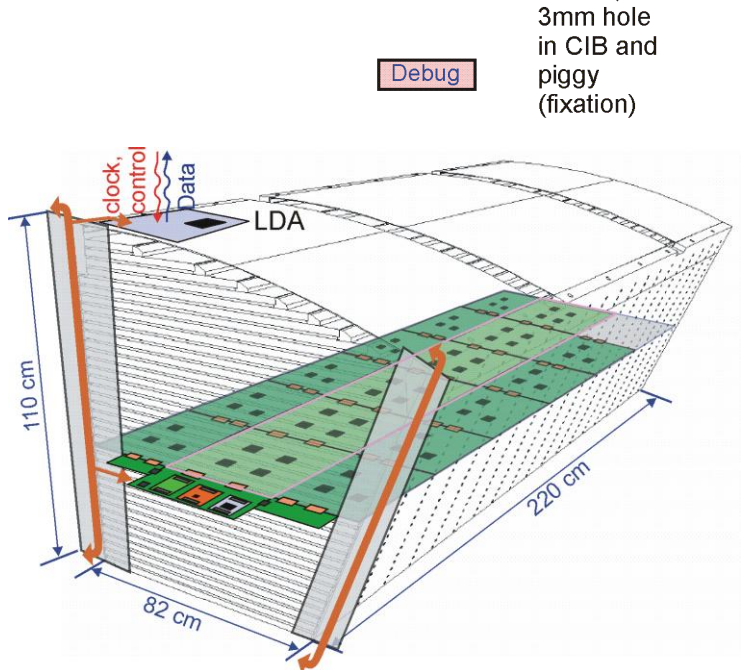**=>**

~172 DACtics / pC (ASIC1)
~182 DACtics / pC (ASIC2)

More results on SPIROC2 tests in "electronics/DAQ" session.

Results by
Jeremy Rouene

DESY

Designs to be done:
CIB, SIB, DIF, CALIB2, POWER2, HBU2, (Flexleads)

Reflector Foils

SPIROC2 in cutout

Flexlead on 0.8mm connector

UV LED

Robust Interface Connector

Electronics height: 17mm max

DIF, CALIB and POWER mezzanine cards

~7.5 max

1.6

18

4.2

2.6

4.1

0.5

~6

~75

in mm, not in scale

100

Tile with SiPM

HBU, 0.9mm thick (Printed Circuit Board)

Cooling Pipe

Cassette Bottom Plate (Steel)

Central Interface Board
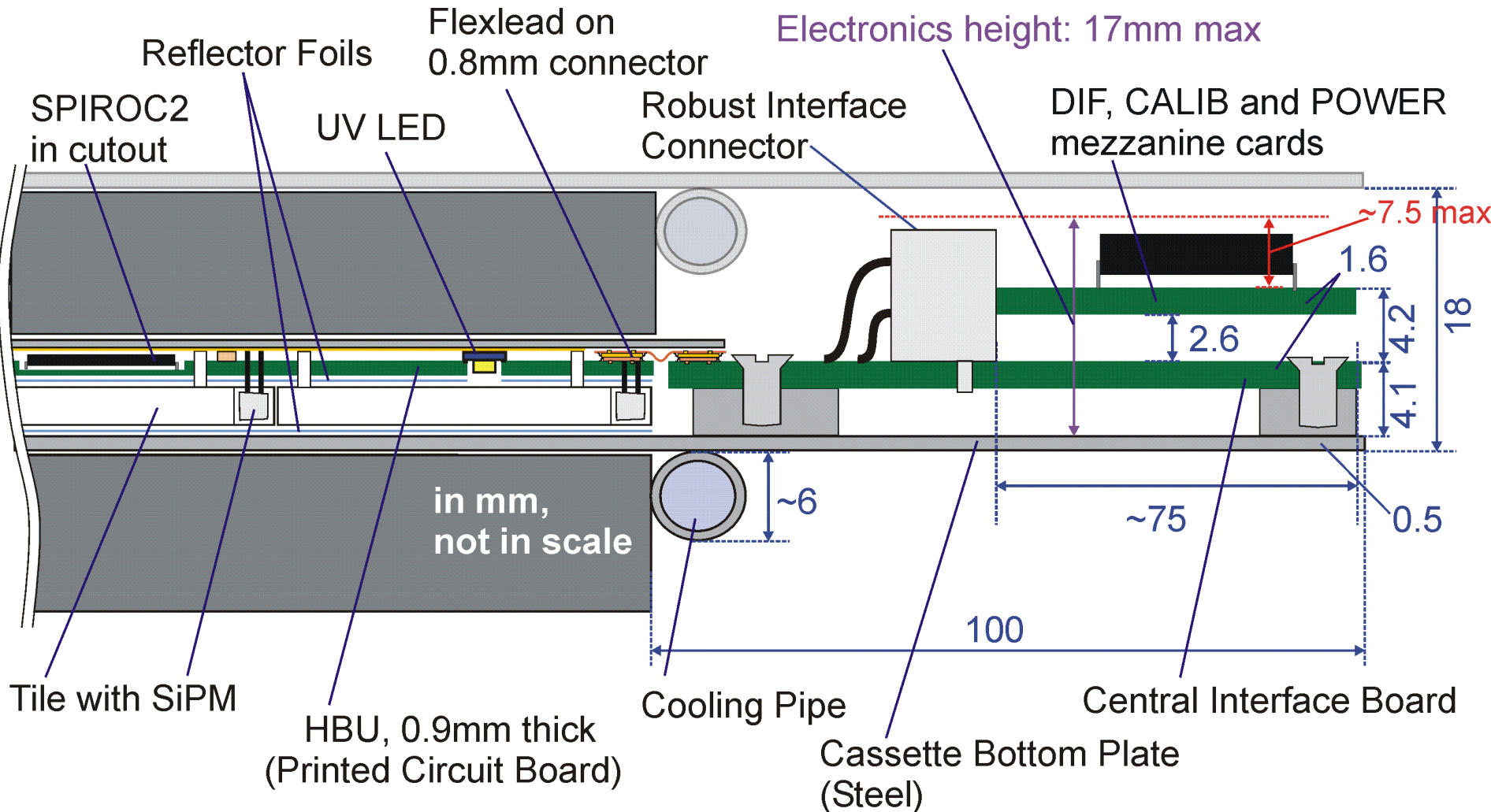
Compliant with Steel and Tungsten options.

Status Redesigns

|	DIF	CALIB2	POWER2	HBU2	CIB	SIB	Flexleads
concept dev., circuit design	X (green)	X (green)	X (green)	X (green)	X (green)	X (red)	X (green)
schematic entry	NIU X (yellow)	X (green)	X (green)	X (green)	X (green)	X (red)	X (green)
Layout	NIU X (red)	X (green)	X (green)	X (yellow)	X (green)	X (red)	X (green)
Production	NIU X (red)	X (green)	X (yellow)	X (red)	X (yellow)	X (red)	X (green)

X (green) done

X (yellow) in preparation

X (red) not started yet

> Most critical part: HBU2 (depends still on results from ASIC tests, tile size definition). **HBU2 can carry SPIROC2, 2a or 2b.**

> SIB is not needed for layer module => delayed.

> all modules needed for EUDET layer-module.

> DIF design taken over by NIU – thank you!!

DESY Redesigns:
M. Zeribi, H. Wentzlaff,
M. Reinecke

CALIB2 module (realized)
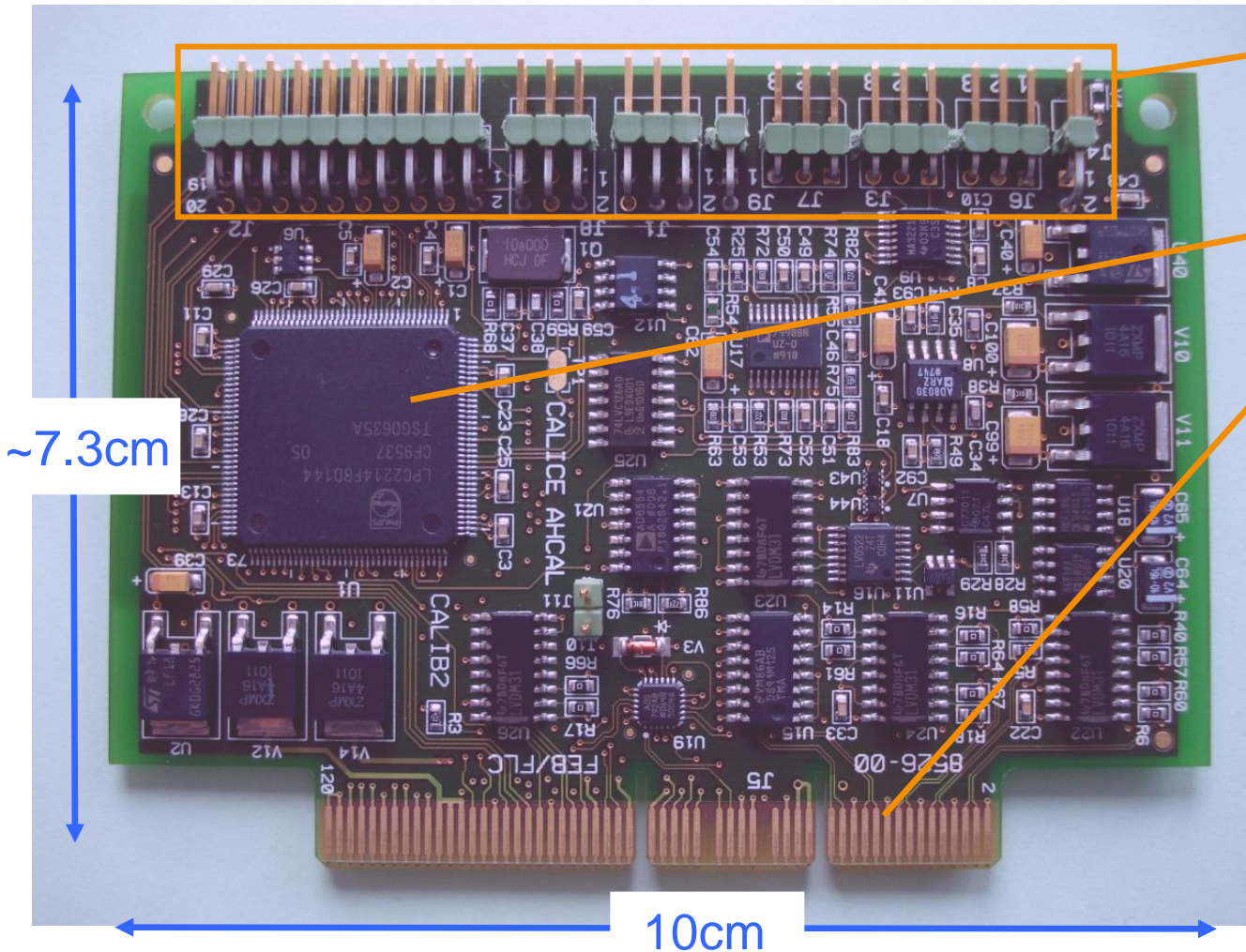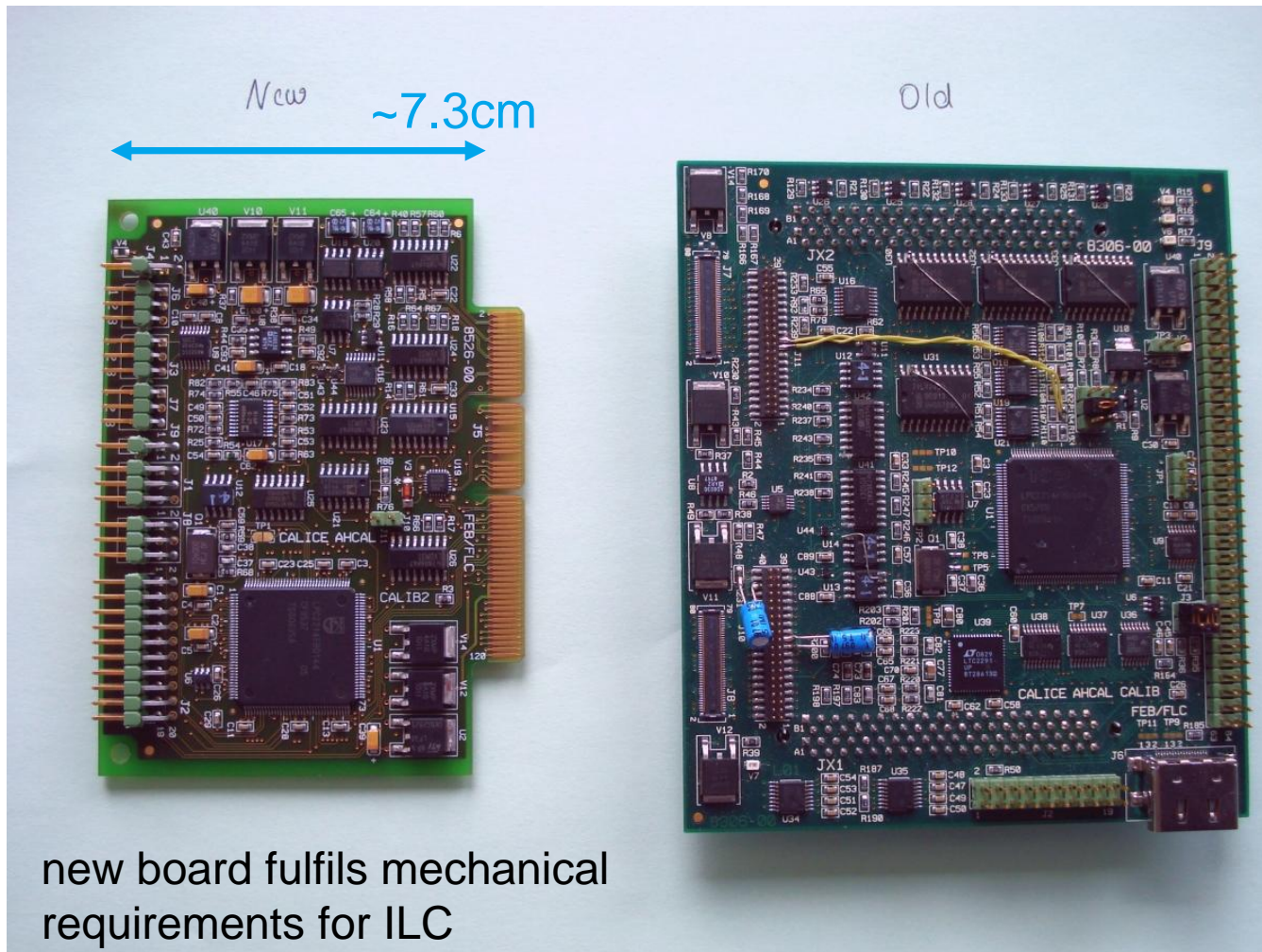

JTAG- and test-connectors

ARM7 µController

Connector to CIB

~7.3cm

10cm

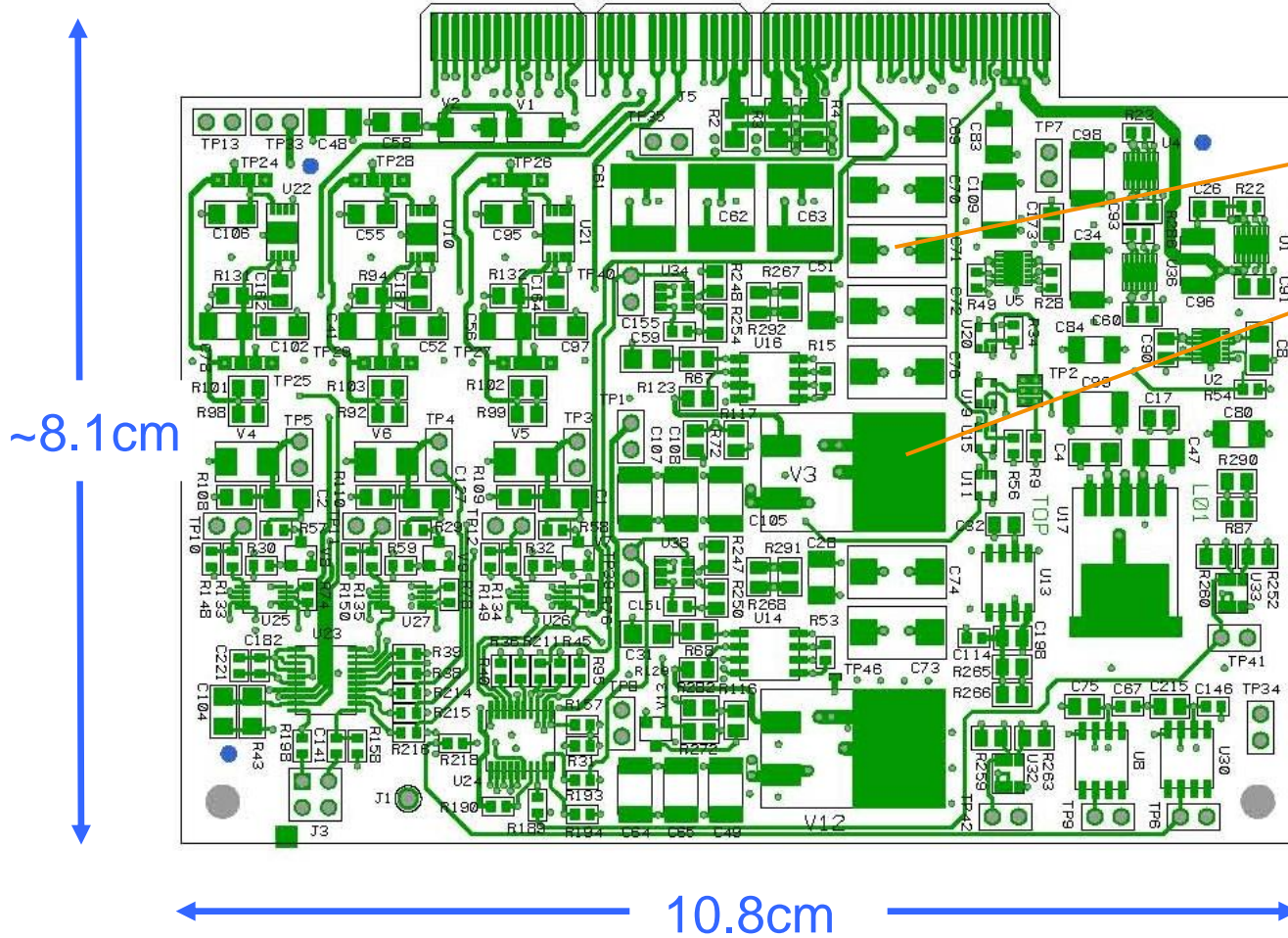**Board survived smoke test, µController is running with old code already.**

CALIB2 module (left) vs CALIB1 module (right)

new board fulfils mechanical
requirements for ILC
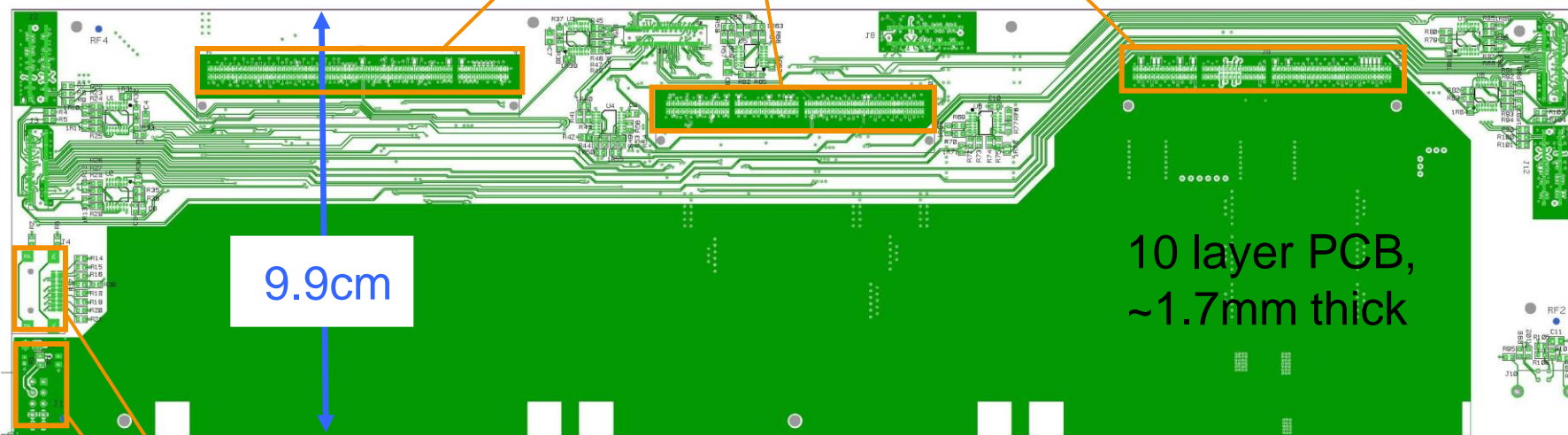(height, x,y-dimensions)

POWER2 Module (in production)

~8.1cm

10.8cm

BIG capacitors and
BIG regulators

for ILC power-pulsing

CIB Module (in production)

connectors for
DIF2 CALIB2 POWER2

9.9cm
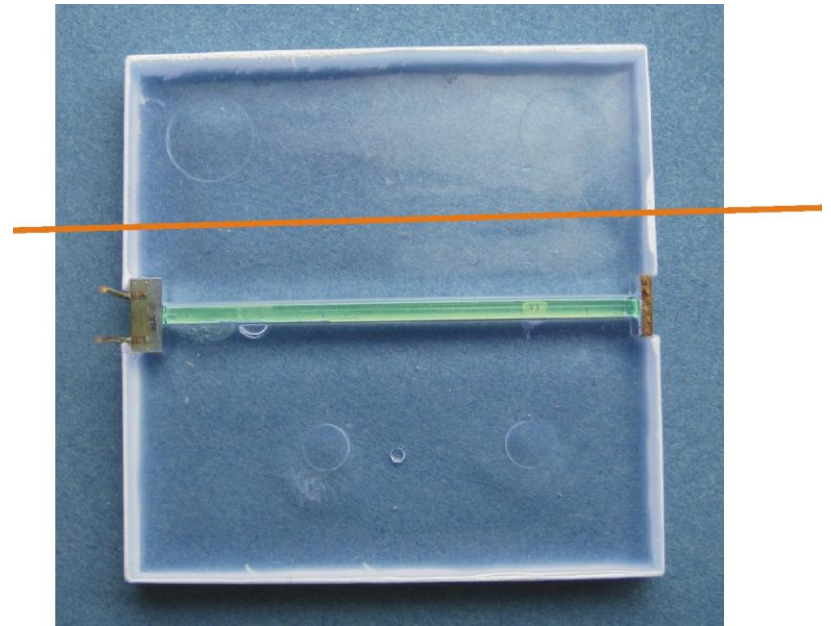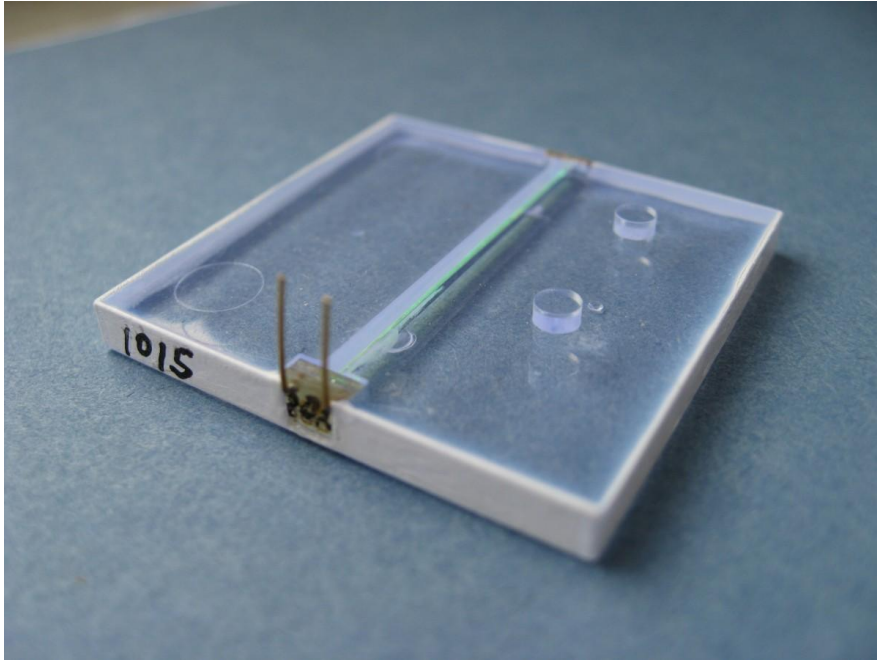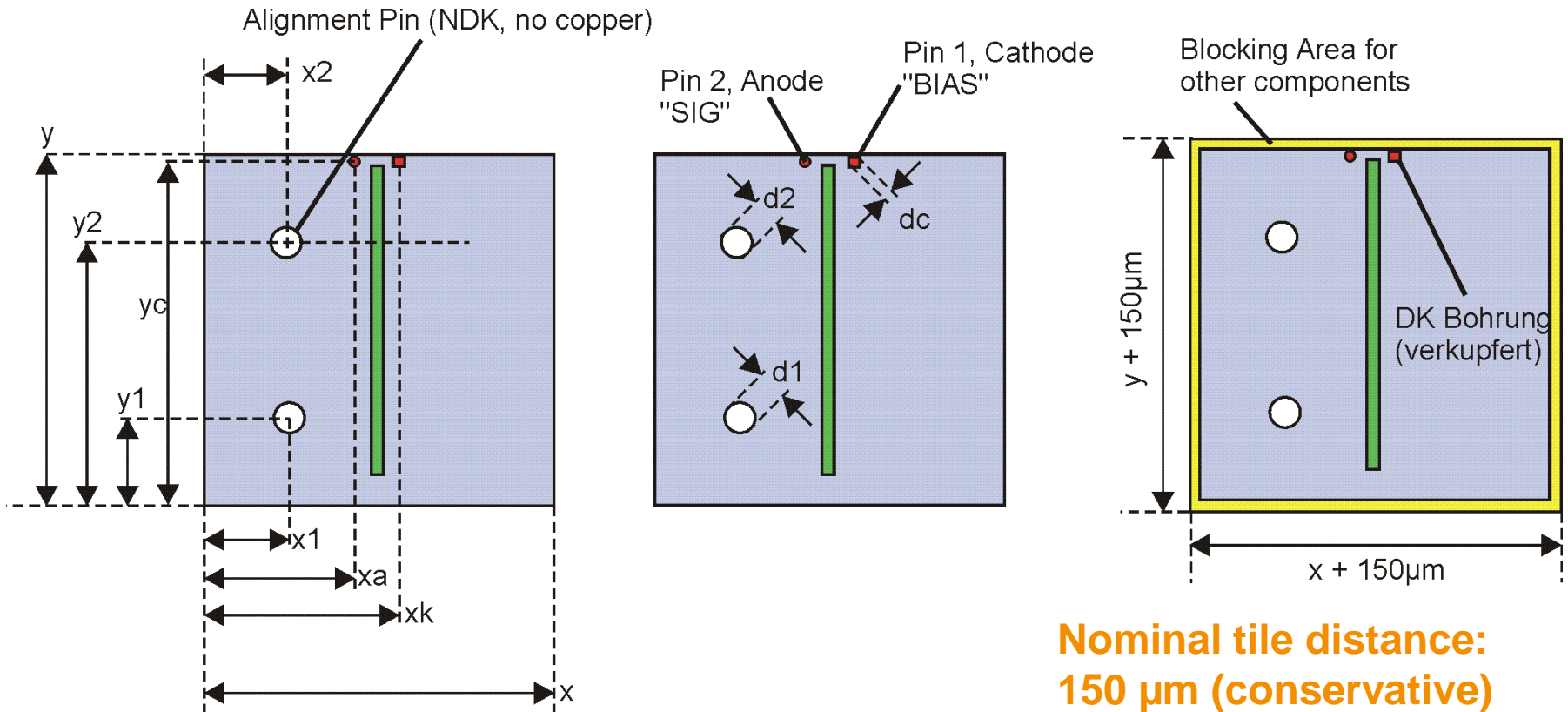
10 layer PCB,
~1.7mm thick

36.19cm

HDMI (DAQ – to LDA)
Power Input

The first 50 have arrived from ITEP in Hamburg – Thank You!!!

EUDET Tiles - Dimensions

Nominal tile distance:
150 µm (conservative)
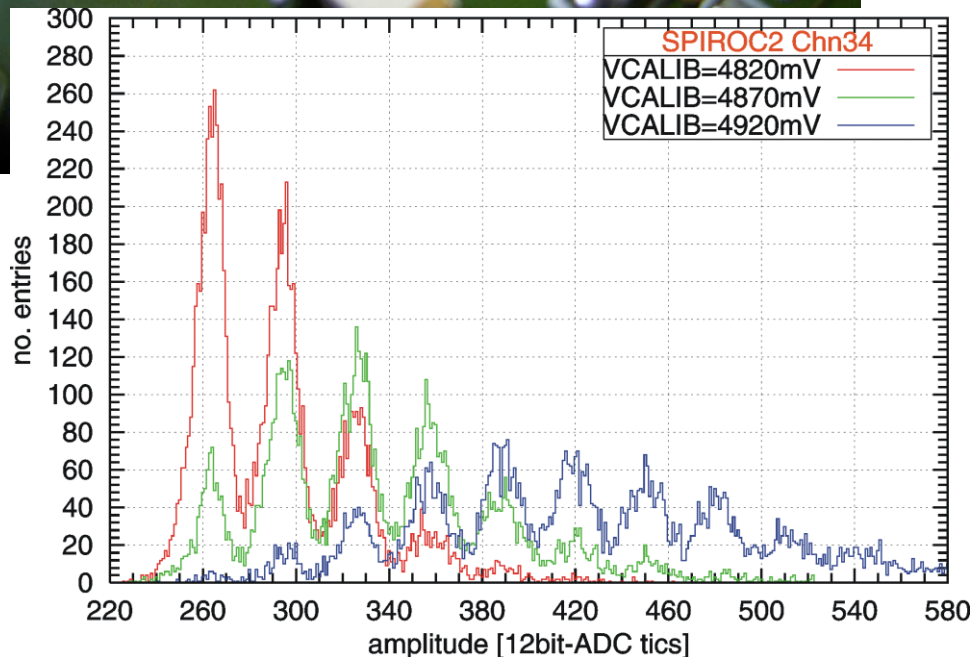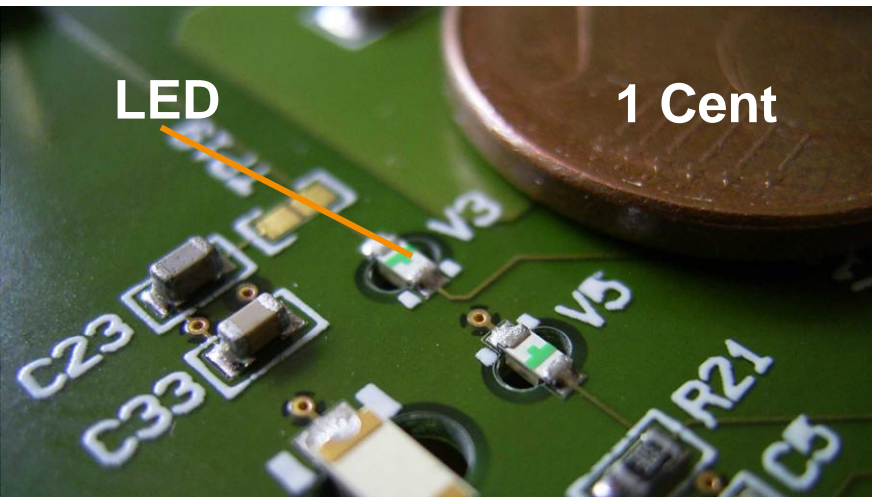**100 µm (tight)**
(tile size reduced to 30.0mm)

> Tile Dimensions still under discussion => HBU2 design delayed!

> Tile alignment testboard in design-phase (ITEP-DESY coordination)

Integration of ASCR Prague LED system into DESY setup

TCALIB (CALIB to QRLD6x)

**HBU (DESY)**

QRLD6x board (ASCR Prague)

Fiber
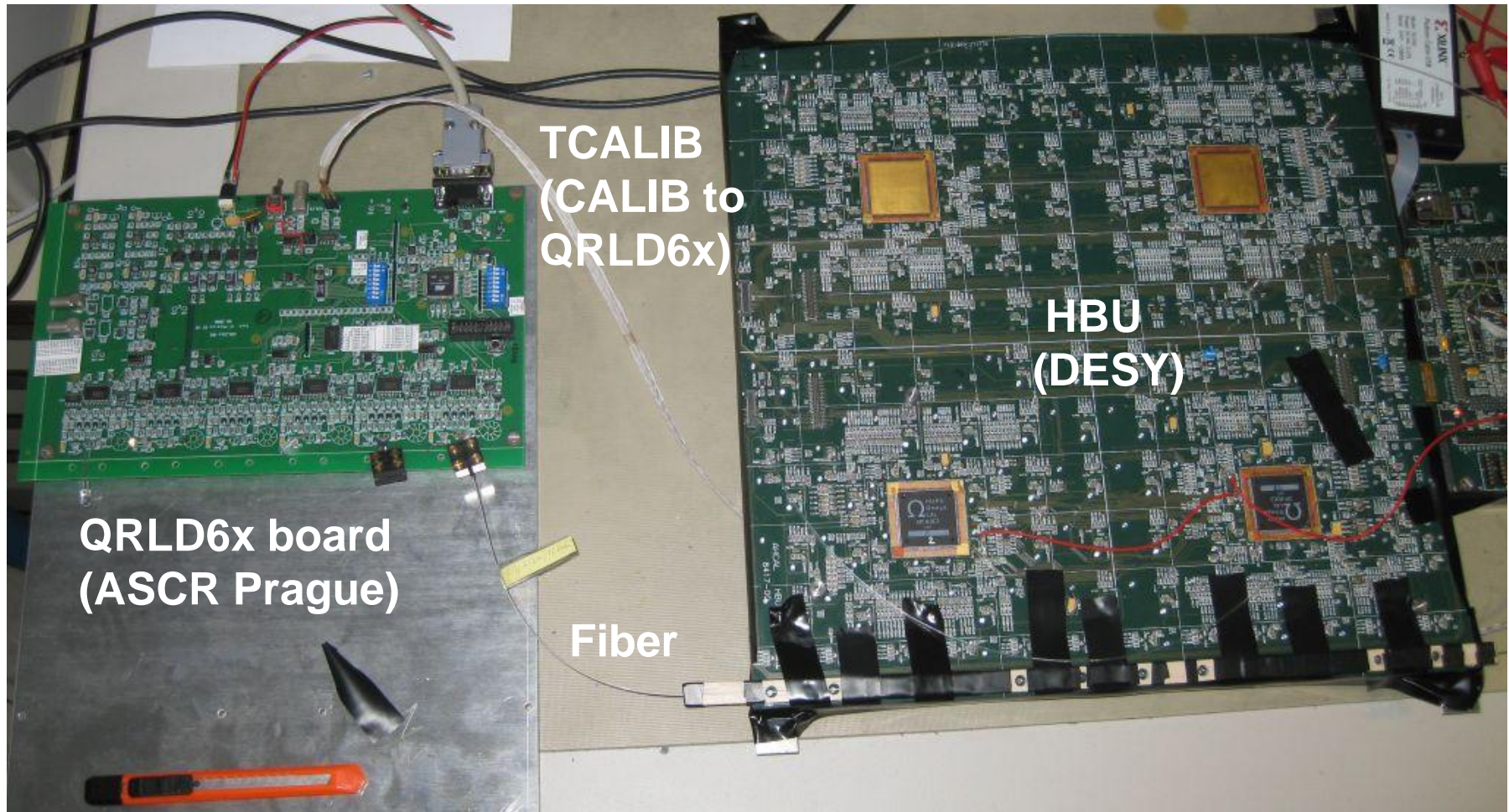
See talk from our Prague colleagues!

LED Calibration Systems II – DESY + Uni Wuppertal

LED   1 Cent

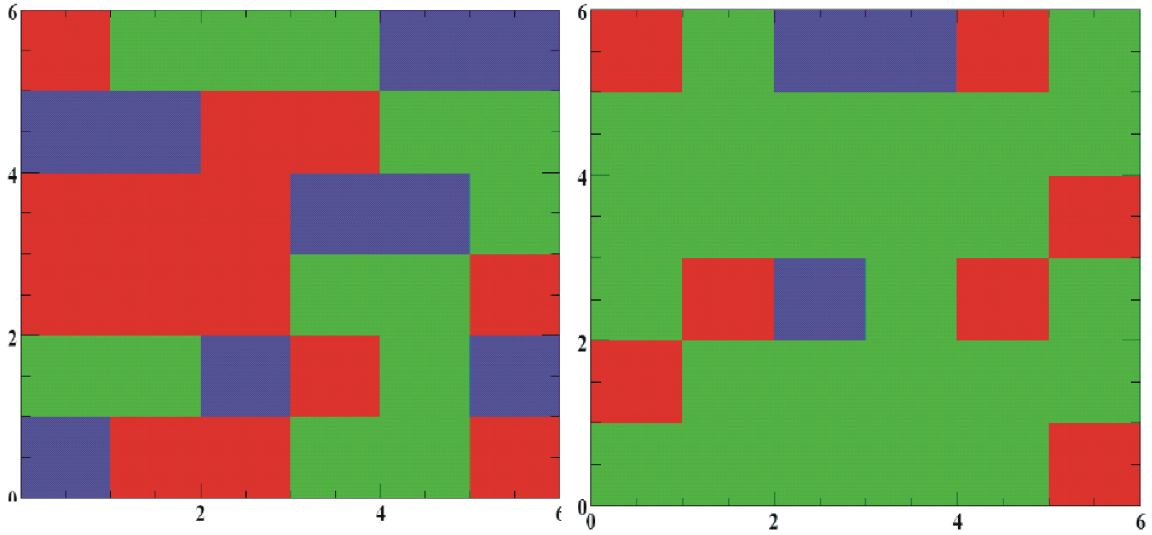SPIROC2 Chn34
VCALIB=4820mV
VCALIB=4870mV
VCALIB=4920mV

> LED uniformity under investigation

> Wuppertal recommended new LED driving circuit and new LED type with lower spread in output.

> HBU2 will contain solder parameter field in order to adjust LED power per channel.

> to be optimized: LED light output spread, dynamic range (saturation)
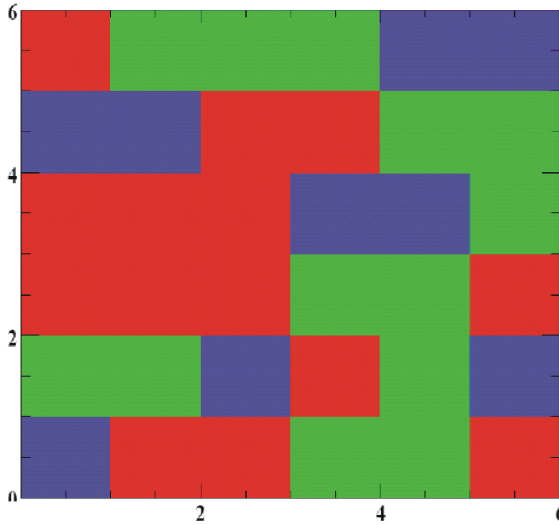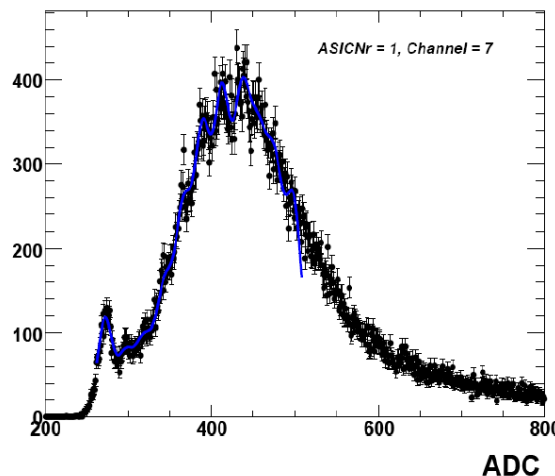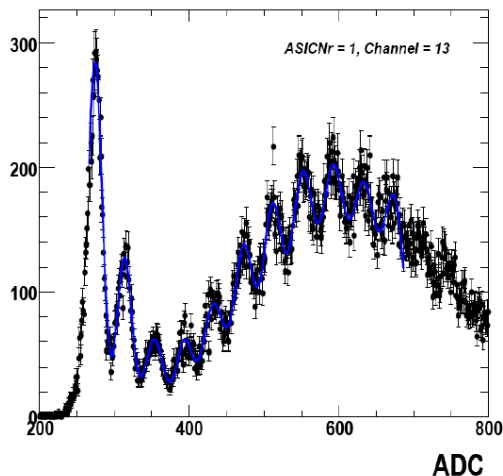
SPIROC2_2

SPIROC2_1

HBU-wide charact. of SiPM single-pixel spectra

green: good single-pixel spectrum
red: SiPM does not show single-pixels
blue: LED or SIPM dead
(to be analyzed …..)

ASICNr = 1, Channel = 13

ASICNr = 1, Channel = 7

Development of:
Automatic fit and
gain extraction routines
(here: for testbeam MIP
  signals)

Results by
Julian Sauer

AHCAL DAQ – currently still Labview and USB

> CALICE DAQ integration still not scheduled

 - hardware missing (e.g C&C to LDA, not all LDA outputs work)

 - DAQ operation/firmware: LLR did great progress, but parallel development @DESY does not make sense.

> DIF firmware structure/block definition within DIF task force

 - first step for CALICE DAQ integration

 - AHCAL DAQ runs with specified command set.

> AHCAL layer module cannot really run with USB DAQ – data taking will be very slow (~1Hz).

Conclusions and Outlook

> 2 prototype setups running in parallel in Hamburg:

  - testbeam: channel-wise calibration with MIPs

  - lab-setup: SPIROC2 tests

> redesigns are ongoing, but are delayed by ongoing system tests and optimization of tile tolerances.

> CALICE DAQ integration strongly delayed due to situation in UK.

> LED calibration system development ongoing with 2 options.

> Eagerly awaiting SPIROC 2a/2b.