FPCCD Vertex Detector R&D status and plan

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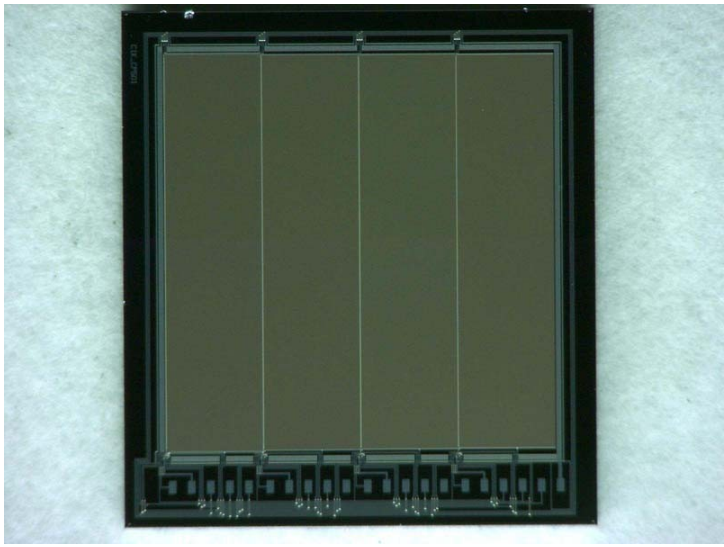
@ILDWS

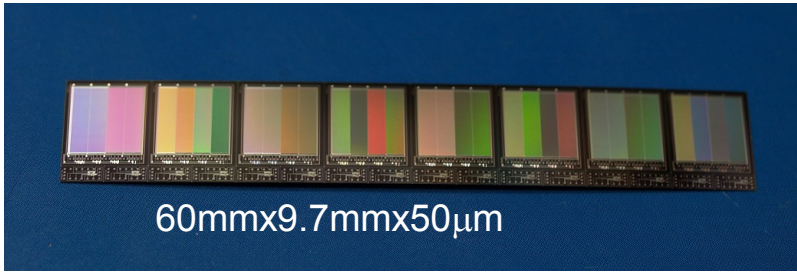
R&D issues

- Sensor R&D
- Frontend ASIC
- System integration
  - Carbon foam core sandwich ladder
  - 2-phase CO2 cooling system
  - Overall mechanical design
- Software development
- MOKKA model

Sensor R&D

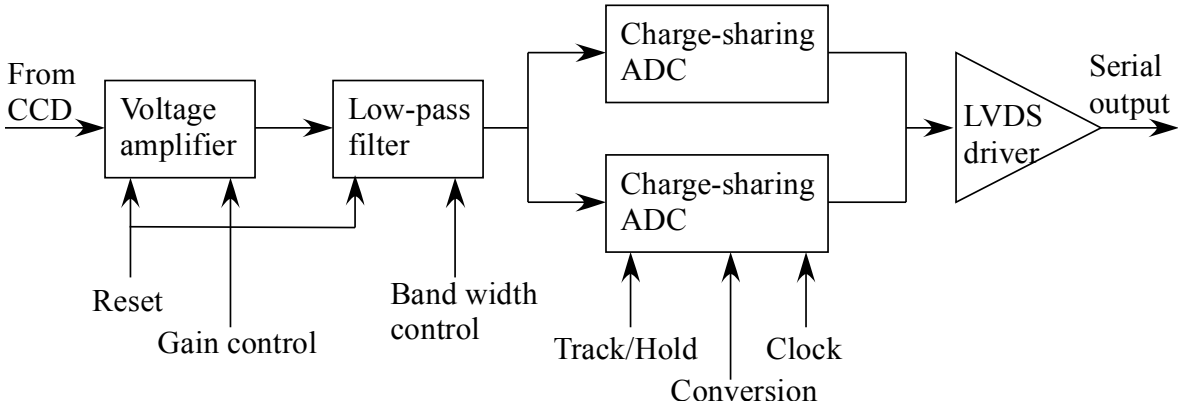
- Prototype FPCCD sensors have been developed
  - Pixel size: 6μm
  - Chip size: 6mmx6mm
  - Fully depleted epitaxial layer of t=15μm
  - To be tested soon
- Wafer thinning
  - Thinning down to 50μm is not a problem
  - Thinned samples have been made, and the dark current has been measured
- Plan towards DBD
  - Radiation hardness test
  - Measurement of spatial resolution, etc.
  - Larger prototype (1cmx6cm) if possible





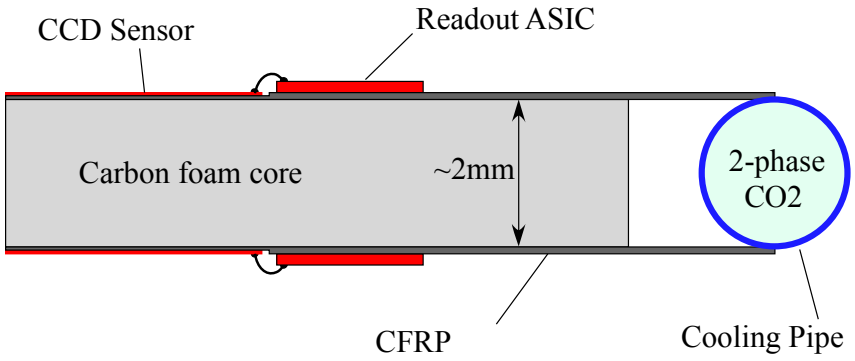
Frontend ASIC

- Our goal
  - Speed: 10M pixels/s
  - Power consumption: <10 mW/ch
  - Noise performance: <30 electrons
- Present status
  - Two types of prototypes have been made
  - We need more improvement on the speed and power consumption
- Before DBD, we will make another prototype ASIC, but it would be necessary to continue R&D after DBD to achieve the goal



System integration

- Ladder design
  - Carbon foam core sandwiched by CFRP sheets, Kapton FPC, and Si wafers
  - Cooling by 2-phase CO2 at both ends of the ladder
- CO2 cooling
  - R&D for 2-phase CO2 cooling system has been started collaborating with LC-TPC, Belle-II VTX, and KEK cryogenic groups
  - We have constructed a “blow system” of the CO2 cooling, and verified cooling between -40 and +15 degrees
  - We wish to construct a “circulating system”
- Plan towards DBD
  - Construct a dummy ladder (with heat source and CO2-cooling, but no FPCCD/ASIC) and a cryostat, and establish the thermal design
  - We cannot say how much maturity we can reach for these R&D issues because of resource shortage

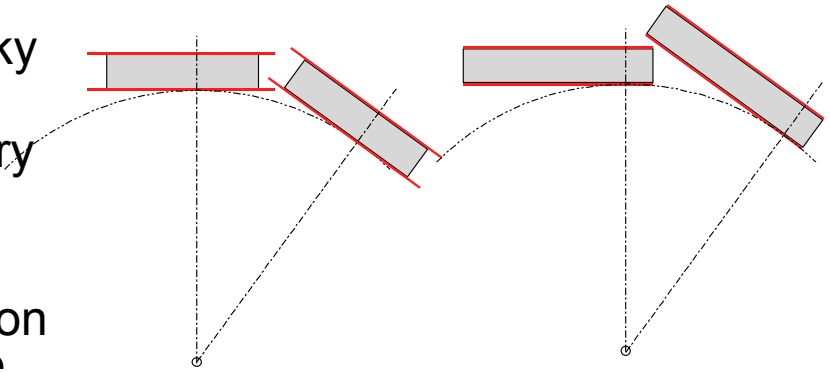


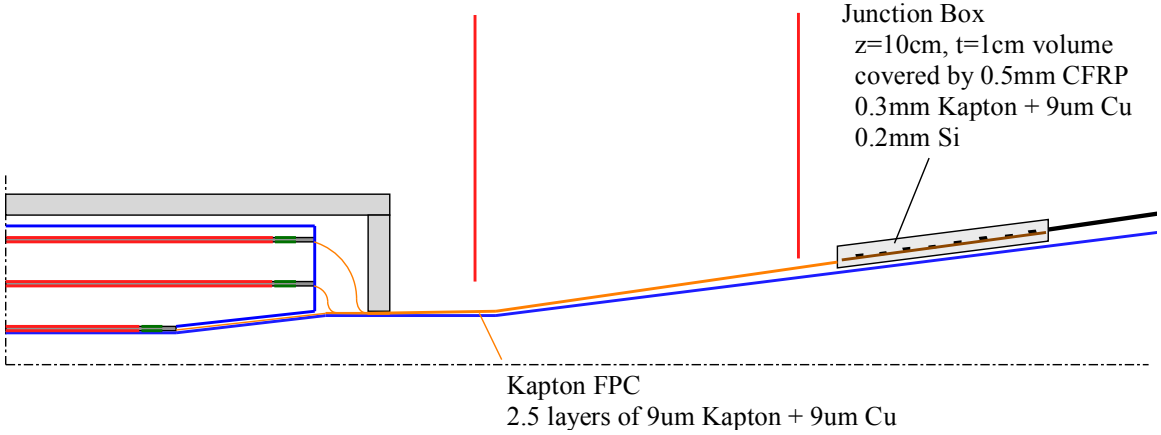
Software development

- Because the FPCCD VTX accumulates hits of one train, the hit density is very high for inner layers
- Special track-reconstruction software is necessary if background hits are overlaid
- Software tools as a part of MarlinReco package developed so far
  - FPCCD digitizer
  - Overlay processor
  - FPCCD clustering
- Plan by DBD
  - Study of flavor tagging and charge ID performance
  - Development of FPCCD track finder

MOKKA model

- Ladder layout
  - Present MOKKA model assumes a tricky overlapping
  - It has smaller <R> but R&D is necessary to achieve it
- Overall mechanical design
  - Design should be similar to CMOS option inside the cryostat, but some difference outside it
  - For MOKKA model, combination of conservative (larger X_0) parts is one possible option





	FPCCD	CMOS
Ladder	C foam	SiC foam
Cooling tube	SUS	?
Connector at cryostat	No	Yes
Kapton cables around BP	Yes	No
Junction box	Yes	No