An ILD vertex detector with CMOS sensors - status report

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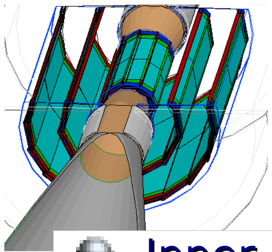
Orsay 2011 May 23

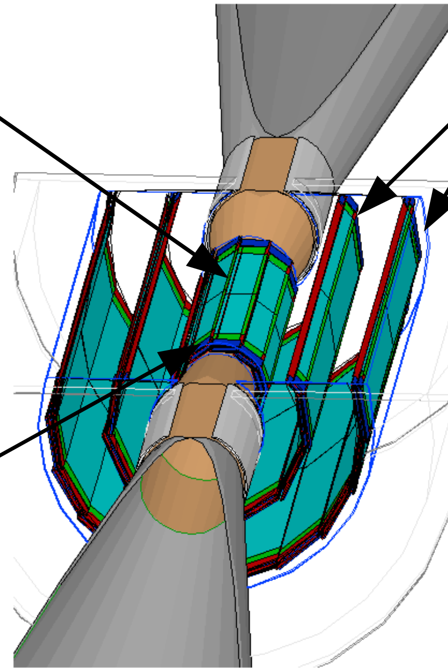
- Detector specifications
- CMOS sensor architecture
- Perspective toward the DBD
- Beyond the DBD
- Summary
- Back-up slides



The CMOS sensor-based VXD

Inner layer – internal side

- ✗ Optimized for resolution
- ✗ 16 x 16 µm²
- ✗ Q encoding: binary
- ✗ $t_{Integration}$ ~40 µs
- ✗ Sensitive area ~ 2 cm²



Outer layer

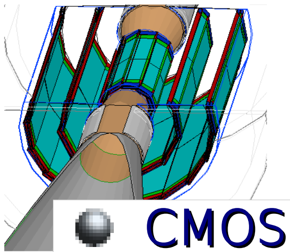
- ✗ Optimized for low power
- ✗ 35 x 35 µm²
- ✗ Q encoding: 4-bits
- ✗ $t_{Integration}$ ~100 µs
- ✗ Sensitive area ~ 4 cm²

Inner layer – external side

- ✗ Optimized for r.o. speed
- ✗ 16 x 64 µm²
- ✗ Q encoding: binary
- ✗ $t_{Integration}$ ~10 µs
- ✗ Sensitive area ~ 2 cm²

layer	radius (mm)	length (mm)	# ladders	# sensors*	#.10^6 pixels	t_{int} (µs)	$\sigma_{s.p.}$ (µm)
1	16/18	125	14	168	66 + 16	40 / 10	< 3 / ~5
2	37/39	250	26	312	2x112	100	< 4
3	58/60	250	40	480	2x173	100	< 4
total			80	960	652		

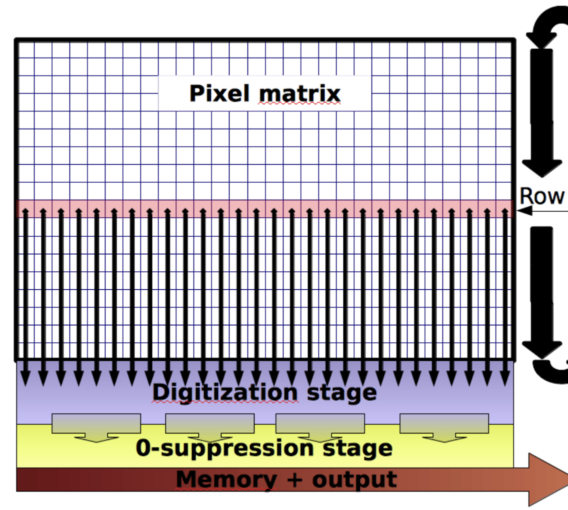
* Numbers corresponding to current CMOS technology (0.35 µm) prototypes



Architecture concepts

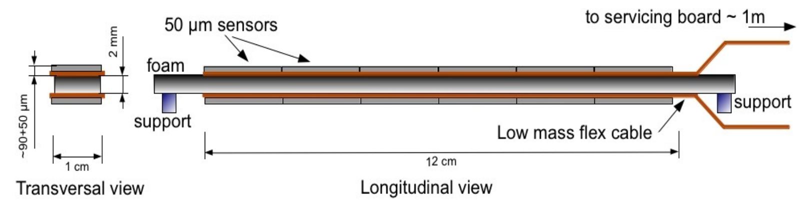
CMOS sensors: high granularity & low power

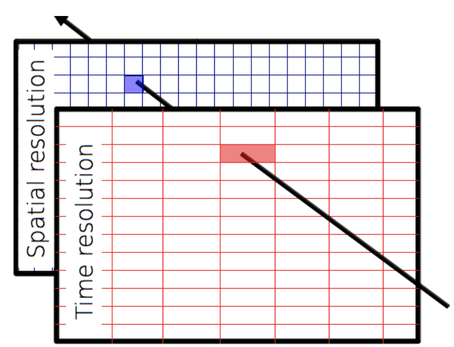
- In-pixel: pre-amplification pedestal suppression
- periphery: digitization + zero-suppression
- Readout strategy = rolling-shutter (column //)
  - ➔ single row active at a time → save power
  - ➔ $t_{integration} = t_{read\text{-}out}$
- Active only during train (2 to 4 ms)
  - ➔ Power pulsing with duty cycle 1/100 to 1/50
- Collaboration: IPHC, IRFU

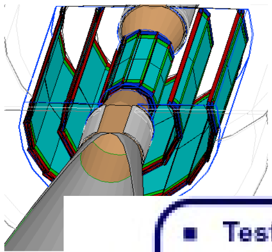


Ladders:

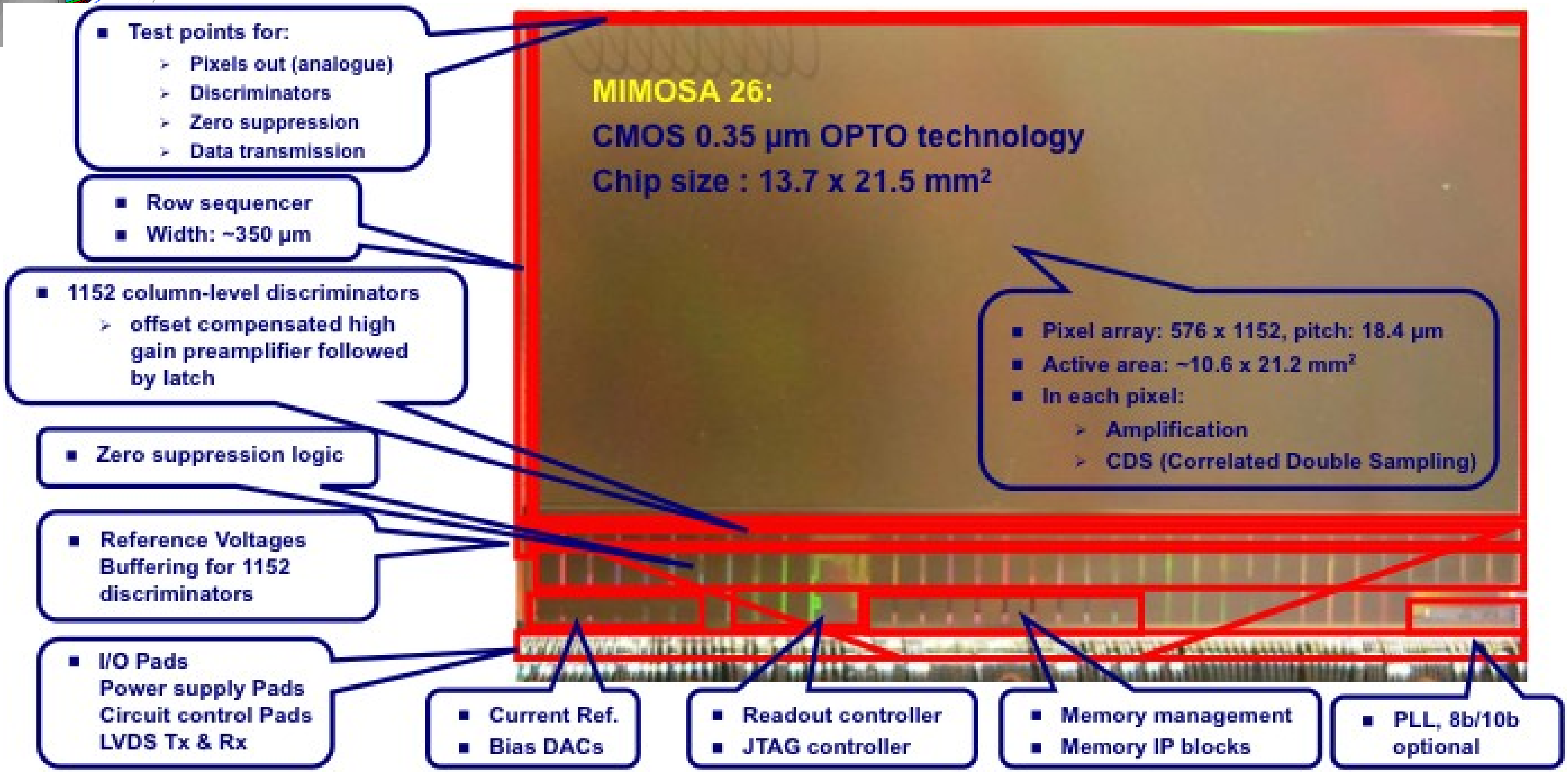
- Sandwich: sensor+cable / stiffener / cable+sensor
  - ➔ Increased stiffness → low mass spacer (foam)
  - ➔ Allows to combine sensors with different spec.
- Air cooling assumed
- PLUME collaboration:
  - ➔ DESY, IPHC, Uni. Bristol, Uni. Oxford



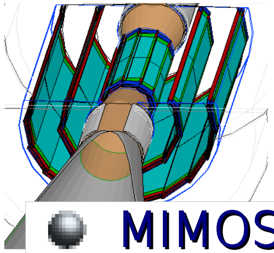




CMOS sensor prototypes



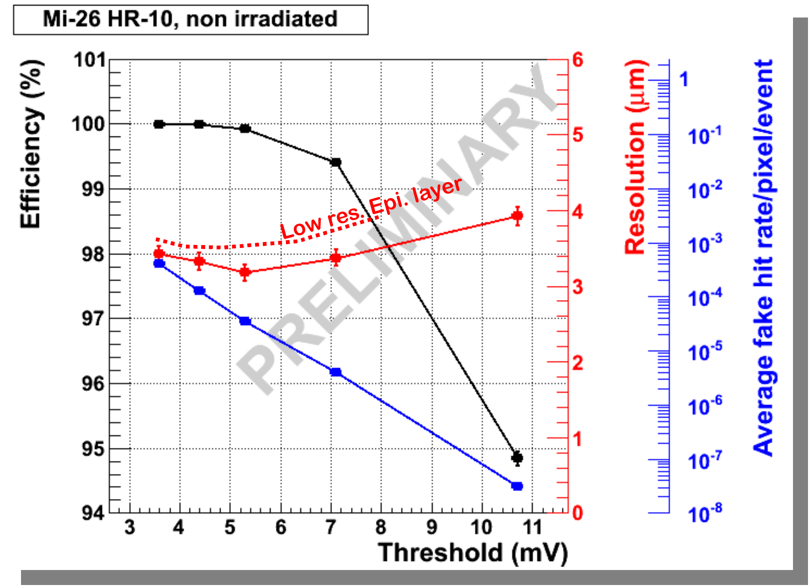
- ✗ EUDET Final Telescope chip
- ✗ Fabricated in 2009 & 2010 with standard (few Ω.cm) & high resistivity (400 Ω.cm)
- ✗ Yield 75% for "perfect" sensors, 90% for usable
- ✗ Thinned down to 50 µm



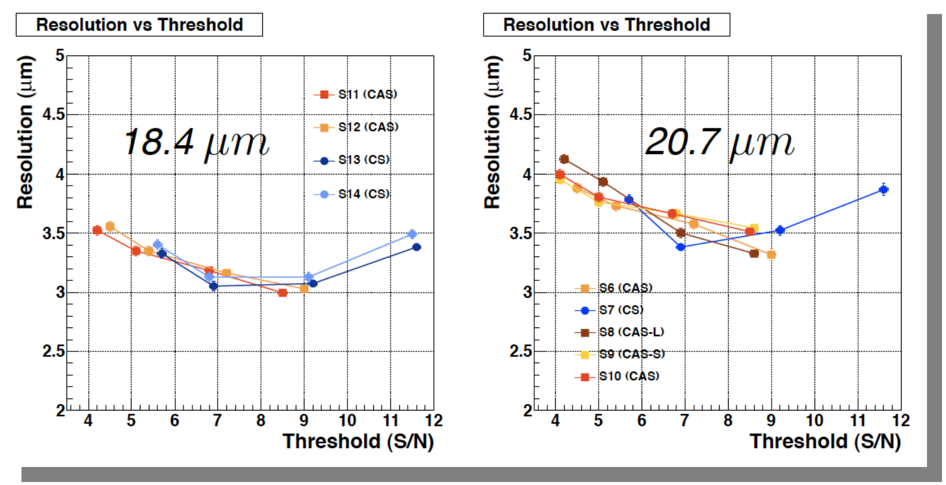
CMOS sensor prototypes

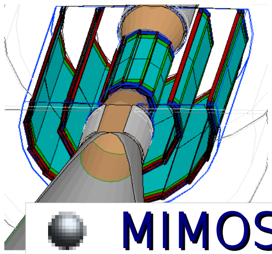
MIMOSA 26

- ✗ Readout time (pixel clock 80 MHz) ~ 100 µs
  - ➔ > 10^6 part/cm²/s
- ✗ Power dissipated ~250 mW/cm²



MIMOSA 22 High Resistivity (400 Ω.cm), fab 2010





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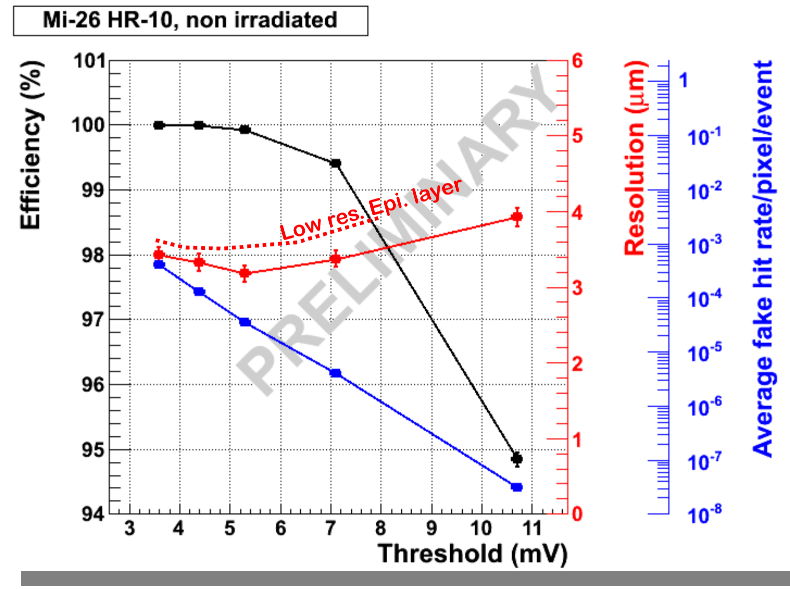

Spatial resolution ($\sigma_{s.p.}$)

- ✗ Depends on: pitch, epi. layer, SNR, q-encoding
- ✗ Extrapolation from previous measurements

Pitch (µm)	20.7	18.4	16
Nb of bits	1	1	1
Epi. layer	high R.	high R.	high R.
$\sigma_{s.p.}$ (µm)	measured 3.5	measured 3.1	extrapolated 2.7

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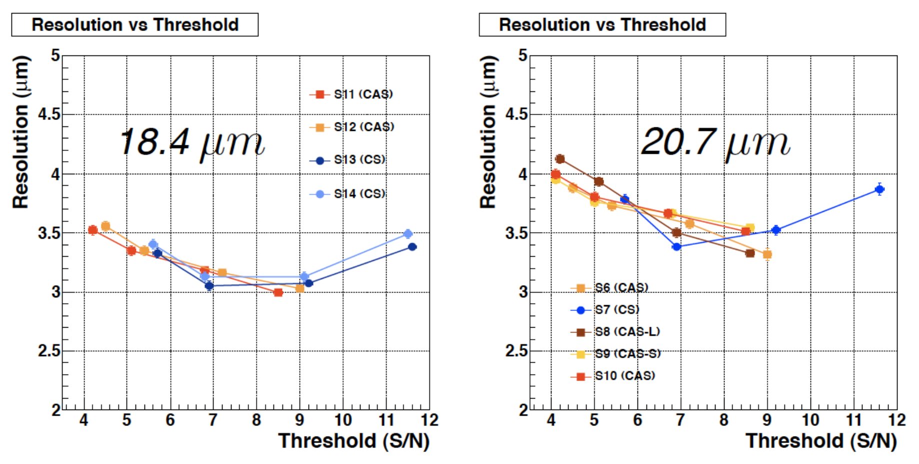
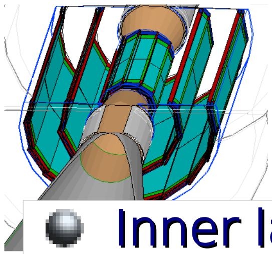


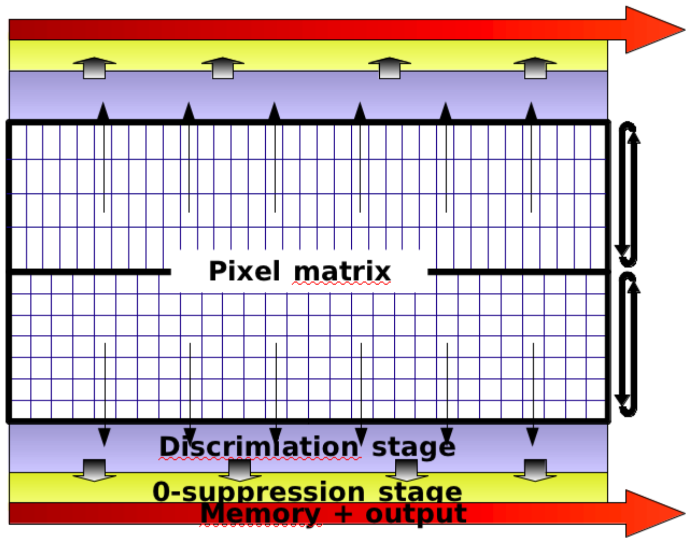
Pitch (µm)	20	20	30	35	40
Nb of bits	12	4	12	4	12
Epi. layer	low R.	low R.	low R.	high R.	low R.
$\sigma_{s.p.}$ (µm)	measured 1.5	re-processed 1.7	measured 2.1	extrapolated < 4	measured 3



DBD perspective: sensors

Inner layer sensors

- ✗ MIMOSA 30
- ✗ Two-sided readout
  - ➔ 256 rows with pitch 16x16 μm²
    - Spatial resolution < 3 μm
  - ➔ 64 rows with pitch 16x64 μm²
    - Spatial resolution ~5 μm
- ✗ 128 columns with binary output
  - ➔ with pixel clock @ 100 MHz
  - ➔ Readout time < 50 μs



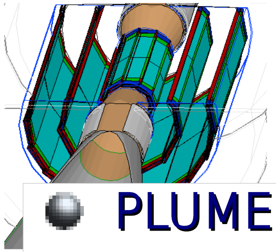
Outer layers sensor

- ✗ MIMOSA 31
- ✗ Pitch 35x35 μm² & 4-bits output
  - ➔ Spatial resolution < 4 μm
- ✗ 48 columns over 64 rows
  - ➔ Readout time ≤ 100 μs

For both sensors

- ✗ CMOS 0.35 μm technology
- ✗ fabrication Q4 2011 (if funding available)
- ✗ Beam test before mid-2012

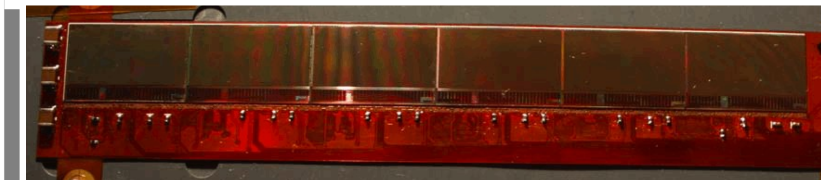
→ Translation into 0.18μm techno. underway



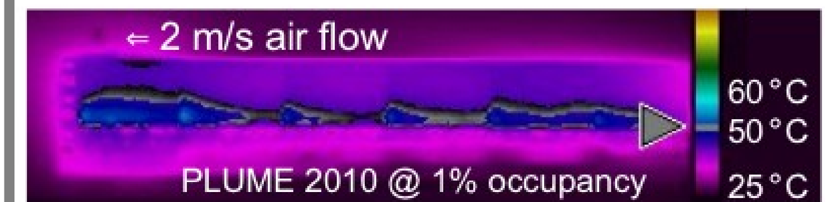
DBD perspective: ladders

PLUME ladder 2010 design

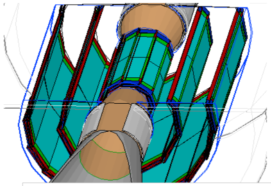
- ✗ Focus on functionality (8 Mpixels, 9 W cont. readout 100 µs)
- ✗ Material budget ~ 0.6% X0 (= 2x target value)
  - ➔ low-mass cable very wide & uses copper traces
  - ➔ Stiffener SiC foam with 8% density
- ✗ Lab tests
  - ➔ Air cooling @ 2 m/s
  - ➔ Positioning precision + stability (ongoing)
  - ➔ Crude power pulsing test (MIMOSA 26 not optimized)
- ✗ Beam test : November 2011
  - ➔ Impact on resolution from air cooling & power pulsing



Thermal measurement



Mechanical prototype with dummy (smaller) sensors



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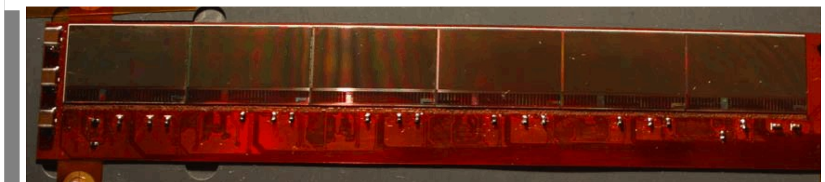

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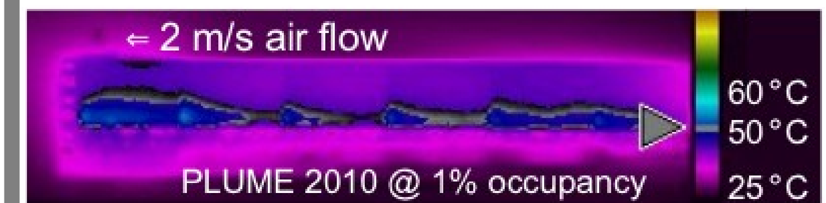
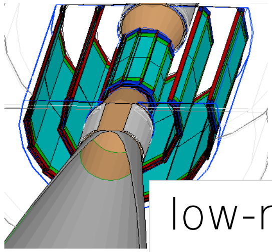


PLUME ladder 2011design

- ✗ Optimized for <u>material budget</u>
  - ➔ Final figure depends on cable mass & stiffener (design finalized Spring'10) assuming 13 µm aluminum traces & 4% SiC foam
  - ➔ Transversal cross-section ~ 0.29 % of X0
  - ➔ Average over the ladder surface (weight/sensitive area) ~ 0.47 % of X0
- ✗ New low-mass cable fabrication Summer 2011
  - ➔ First ladder ~ fall 2011, Beam test summer 2012

Extrapolation with:
- same concept
- thinner sensor
- thinner cable

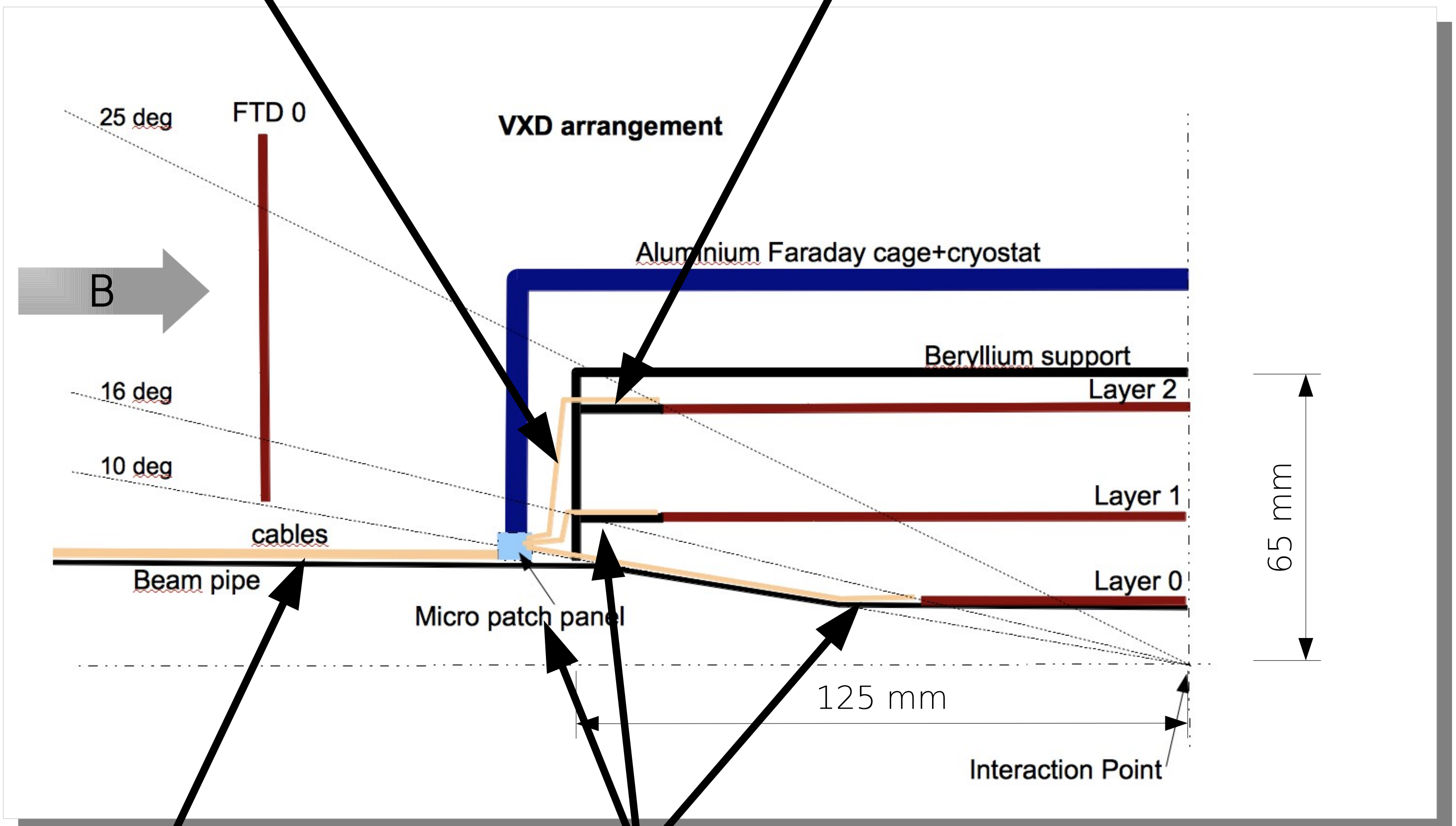
→ **average ~0.3 % X0**



DBD perspective: system 1/3

low-mass cables
+ optic fibers
+ air delivery

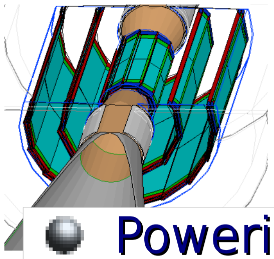
Data concentration + opto-couplers



Model from
CAD tool
& simulation
(except for
air delivery)

copper cables for power
+ optic fibers
+ air pipes

Power re-distribution
& potentially converters



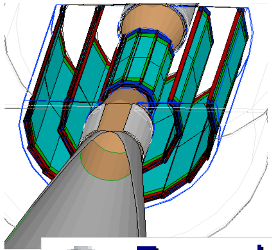
DBD perspective: system 2/3

Powering

- Estimation done:
  - Overall dissipation during train (power on) ~ 900 W (0.35 µm techno) ↘ 700 W (0.18 µm techno.)
  - Duty cycle 1/50 to 1/100 → 20 to 30 W in average
- Delivery strategy to be optimized:
  - Cable size for 700W seems OK / material budget (< 10 g/ cm on pipe)
  - BUT potential gain with DC-DC converters and/or regulators and/or capacitor
  - Location of converters and patch panel not fixed
  - Several scenario to be identified for DBD
- Sensor-level power delivery studies ongoing @ IPHC
  - Timeline beyond DBD

Data flow

- Estimation done:
  - Driven by the first layer with an average rate of 5 part/cm^2/bunchX x 10 (security factor x fluctuation)
  - During train: *O*(1)Tbps data throughput within 1 ms
- Optimization with serializer & opto-converter
  - Work in collaboration with SMU-Dallas (ATLAS)
  - Will not converge for DBD



DBD perspective: system 3/3

Faraday cage & cryostat

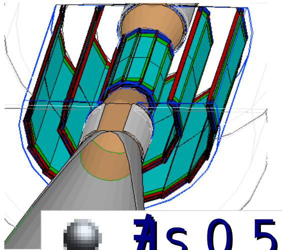
- ✗ Current model extrapolated from SLD
- ✗ No recent work...
  - ➔ Option to share with first FTD stations ?
- ✗ Potential tests with PLUME ladders but not scheduled yet

Mechanical support

- ✗ Current Beryllium support model extrapolated from SLD
- ✗ No changes expected within 12 months

Cooling

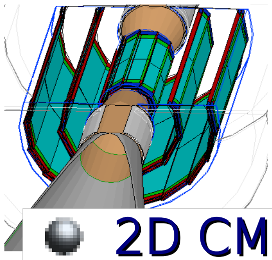
- ✗ Air cooling “seems” sufficient for 20 to 30 W but which air speed?
- ✗ Study for 1 ladder will be completed within PLUME
- ✗ Simulation for whole detector possible @ DESY
- ✗ No work on the air delivery pipe yet



Beyond the DBD

$\sqrt{s}$ 0.5 → 1 TeV

- ✗ Effects: beam bckd x2, physics x$\sqrt{s}$, longer decay distances
- ✗ Impacts:
  - ➔ Sensors with shorter integration time
  - ➔ Geometry may be revisited



Beyond the DBD

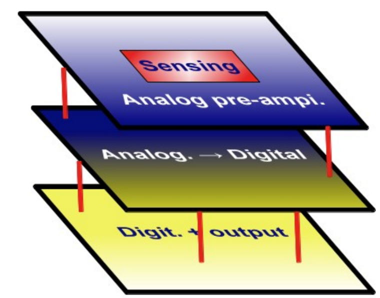
2D CMOS 0.18 µm technology upgrade

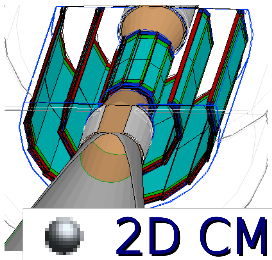
- ✗ Lower power or higher speed (20 to 30%)
- ✗ Also: higher data reduction, smaller pitch, higher radiation tolerance, smaller size peripheral circuitry, stitching
- ✗ First prototype to submit in Q4 2011
  - ➔ 4-5 years program to reach “final” sensors

3D integration technology

- ✗ Optimizes CMOS techno. for each functionality / tier
- ✗ Very high expectations: $O(10)$ µm pitch with $O(1)$ µs readout or 50 ns time-stamping
- ✗ First prototypes fabricated within consortium coordinated by FNAL
  - ➔ Long term program

3D pixel





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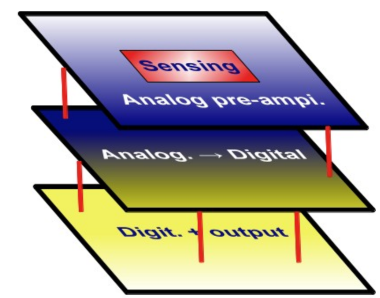
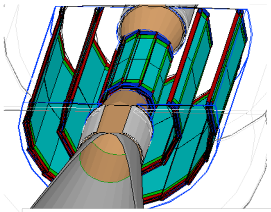


Ladders

- ✗ Further decrease mat. budget
  - ➔ Stitching, embedded sensors
- ✗ single-sided ladders
- ✗ cooling/support alternatives



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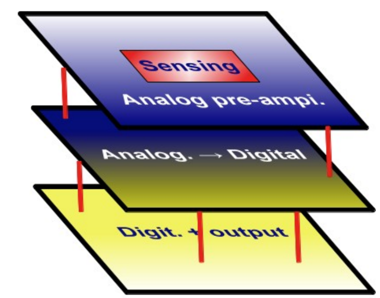
3D pixel



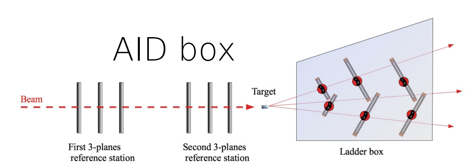
Ladders

- ✗ Further decrease mat. Budget
  - ➔ Stitching, embedded sensors
- ✗ single-sided ladders
- ✗ cooling/support alternatives

Algorithm studies

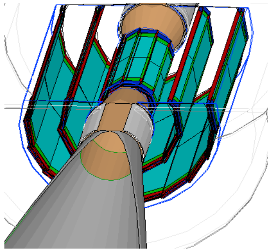
- ✗ Validated on tbeam within AIDA project & PLUME collab.
- ✗ Benefits of 2-sided ladders
  - ➔ Alignment, track matching

AID box



Summary

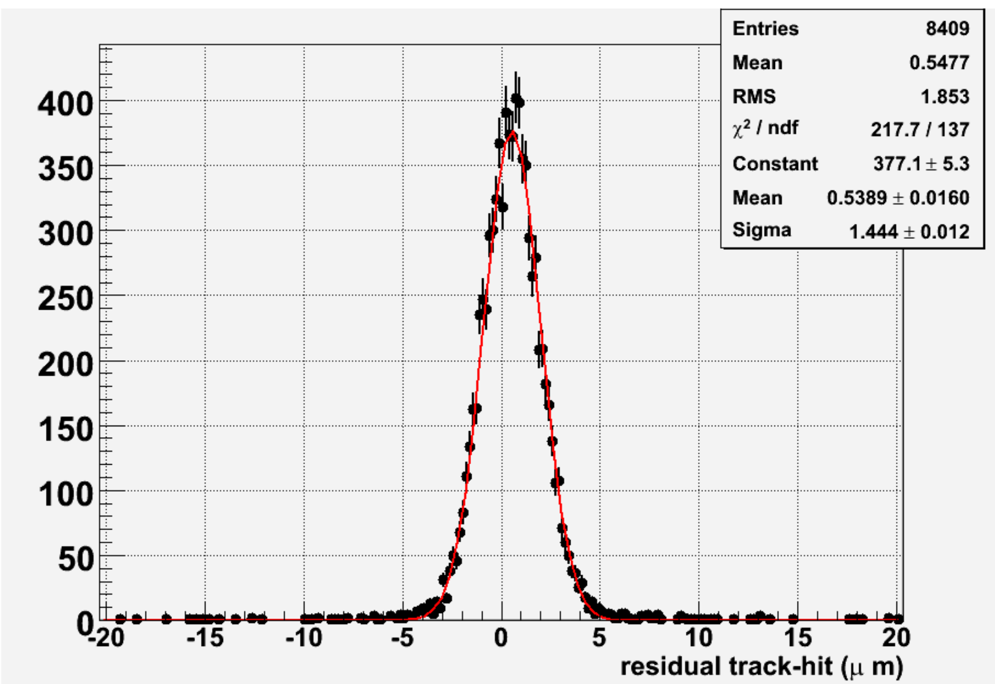
- The CMOS sensor VXD concept
  - ✗ 2 sensor flavors
    - ➔ inner layers: $\sigma_{s.p.}$ < 3µm for 40 /10 µs integration
    - ➔ outer layer: $\sigma_{s.p.}$ < 4µm for 100 µs integration
  - ✗ Based on well established MIMOSA 26 architecture
- Toward the DBD
  - ✗ Prototypes for the 2 sensor flavors fabricated & tested (beam)
  - ✗ Double-sided ladder with material budget of 0.6% X0 in 2011 ↘ 0.3 to 0.45 % X0 in 2012 fabricated & tested (beam)
  - ✗ Detailed needs estimated for services
- Beyond the DBD
  - ✗ Technology migration for enhanced performances (2D short-term, 3D long-term)
    - ➔ Mitigate integration difficulty (material budget, power)
    - ➔ Answer 1 TeV challenges
  - ✗ Development of services
  - ✗ Benefits expected from synergy with other projects: STAR, CBM, ALICE, AIDA → sensor stitching, readout speed, material budget, integration techniques



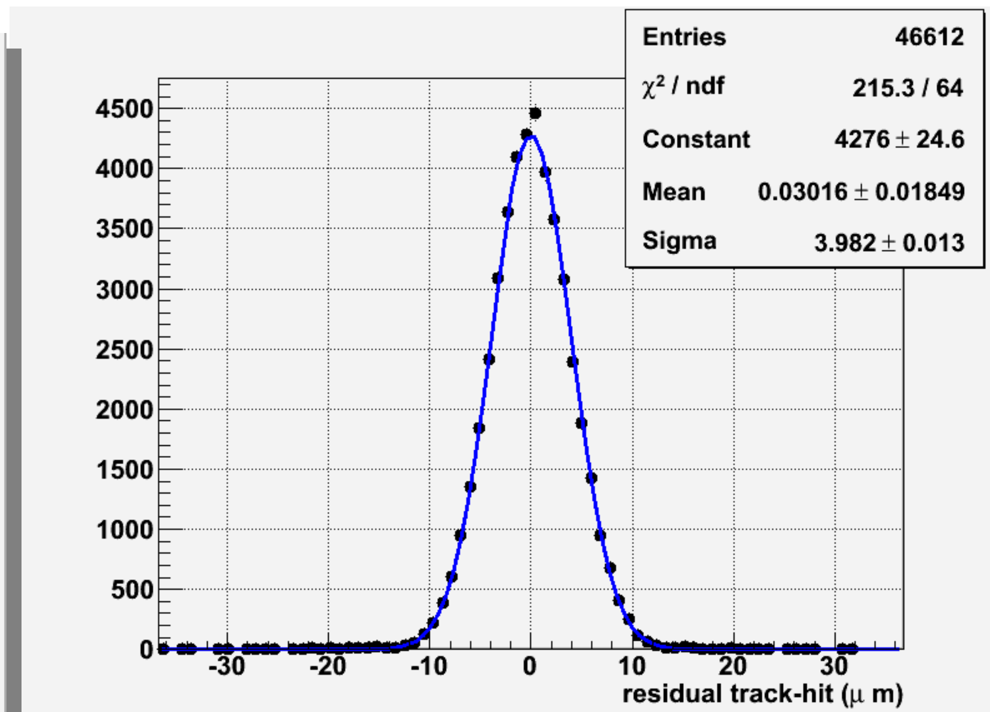
- **Additional slides**
  - ✗ Computing the spatial resolution
  - ✗ DEPFET status
  - ✗ Pixelated SiT
  - ✗ Power pulsing
  - ✗ Power & low mass cables
  - ✗ Parameter space for VXD

Defining the spatial resolution

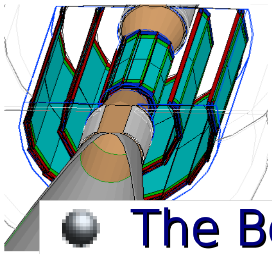
- **From the residual resolution**
  - ✗ Fit with a single gaussian
  - ✗ Spatial resolution = single gaussian std. deviation



Analog sensor case:
MIMOSA 18, pitch 10 µm



Binary sensor case:
MIMOSA 26, pitch 18.4 µm

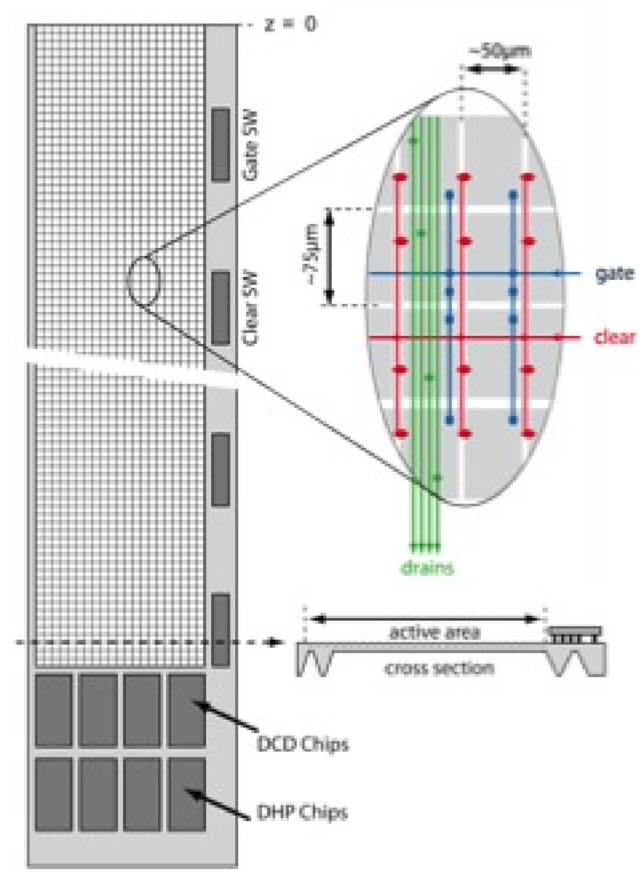


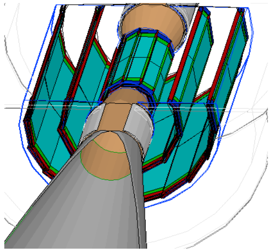
The DEPFET-based VXD

From L.Andricek, 2010

The Belle II VXD as ILD demonstrator

- 2 single-sided ladders with DEPFET APS ladders
- L1: radius 14 mm, 90x12.5 mm2, 8 ladders, 50x50µm2, 1600x250 pix/ladder
- L2: radius 22 mm, 126x12.5 mm2, 12 ladders, 50x75µm2, 1600x250 pix/ladder
- Thin (50µm) sensitive area, ladder concept like in ILD
  - ➔ 0.19 % X0 in fiducial volume
- Frame rate 100kHz (L1) and 50kHz(L2), continuous read-out
- Line rate: 12.5 MHz, "rolling shutter" mode
- Power dissipation per ladder (20 ladders)
  - ➔ Sensor ~1 W + switcher ~1 W
  - ➔ DCD+DHP chips ~ 8 W
- Radiation damage: a few Mrad/year
- No requirements in forward region relaxed end-of-ladder (EOL) specs for material and services
- no power pulsing possible, but aggressive (liquid) cooling on EOL allowed
- first Belle II data expected 2014

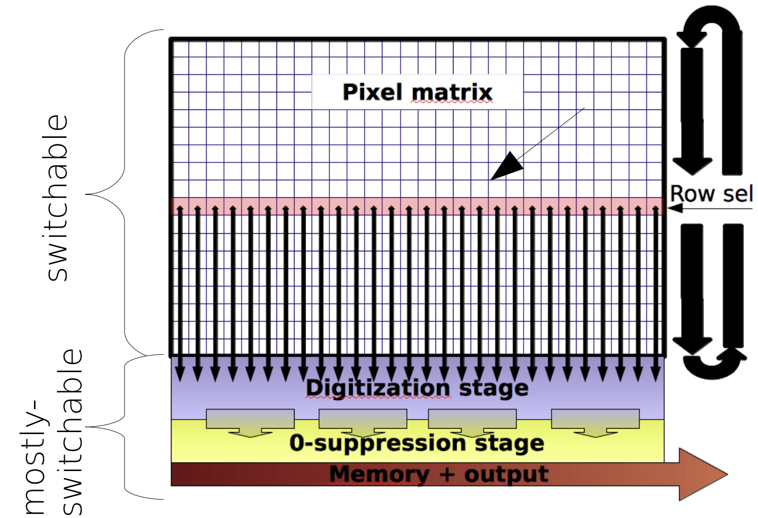




the pixelated SiT option

Power pulsing sensor

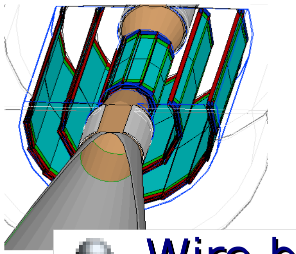
- **Pulsing strategy**
  - ✗ Activity period ~ 2 to 4 ms over the 200 ms train
    - ➔ Estimated duty cycle range: 1/50 to 1/100
  - ✗ For stability reasons, not all element switchable
    - ➔ Test started for the analog part
    - ➔ To be done for the digital circuitry



Assuming: 0.18µm techno. & 1.8 V voltage & continuous operation		sensor switch.	sensor not-swi.	sensor total	2-sided ladder switch.	2-sided ladder not-swi.	2-sided ladder total	whole detector switch.	whole detector not-swi.	whole detector total
inner layer	power (W)	1,575	0,025	1,6	18,9	0,3	19,2	688 W	12 W	700 W
	current (A)	0,875	0,014	0,89	10,5	0,17	10,67			
outer Layers	power (W)	0,490	0,010	0,5	5,88	0,12	6	382 A	7 A	390 A
	current (A)	0,272	0,006	0,28	3,27	0,07	3,33			

Average power (integrating pulsing) 20 to 30 W

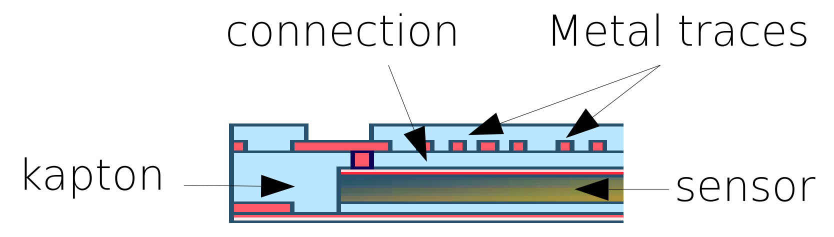
→ Air cooling probably good enough



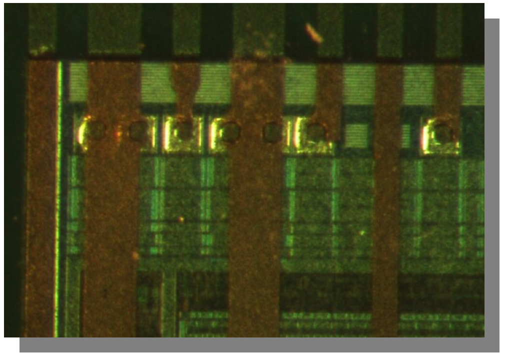
Power pulsing & low mass cables

Wire bonds

- ✗ Average current through powering wires ~10 mA
  - ➔ Small residual force in B=4T but vibrations possible
- ✗ Monolithic sensors are easy to handle
  - ➔ Possibility to embed in polyimide & connect through metallization
  - ➔ IMEC+CMST & CERN projects



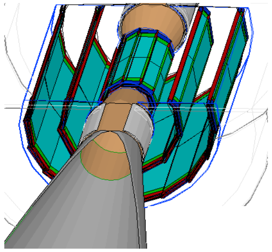
profile view



Top view
1st trial of a MIMOSA embedded by IMEC

Lorentz force on low mass cable

- ✗ Many "small" transverse traces
  - ➔ Residual force could reach few g ≈ cable mass!
- ✗ Double-sided structure could be used to counter-balance the effect
  - ➔ Cable design with reverse current path on each side
- ✗ Switching sensors with some delay and not simultaneously → reduce current
  - ➔ Require specific sensor functionalities



Parameter space for a VXD