DAQ session
Introduction & Short status

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LLR, École polytechnique

Calice eDAQ
LLR
09 /02/2011

TB DAQ modes

Single Event + Ext. Trig

- ► External trigger (from hodoscope or calibration system) = HOLD
    - ◆ Stop Acq, Hold analog data + sampling, Start Acq
- ► Noise & Beam condition safe (only 1 evt per trigger)

Single Event + auto-Trig   NOW USED IN SDHCAL TB

- ► **External trigger** (hodoscope) → DIF
    - ◆ Stop Acq, ReadOut (last evt ~ triggered one), Start Acq
      (AHCAL "validation mode" identical: no external trigger within memory depth = lost data)
- ► **Data sync** (for Event building)
    - ◆ On synchronized BC ID → **need for a SYNC @ MClk (100– 400 ns)**
    - ◆ On trigger timestamp (e.g. On DIF Timecounter on last internal trigger to ext. trigger):
      $\text{time} = (\text{BC-LastBC}) \times \tau_{BC} - \text{DiffCounter} \times \tau_{DiffCounter}$
    - ◆ **BUT: for the AHCAL/Spiroc:** the TDC signal needs a SYNC of the clocks **±1ns**
- ► **Rems:** RAMfull → Reset of SLAB with BUSY

ILC like

- ► StartAcq on Start-of-Spill signal (-δt)
- ► StopAcq & Readout on End-Of-Spill or RAMfull or a Given # Beam Trigger

CALICE DAQ2 scheme
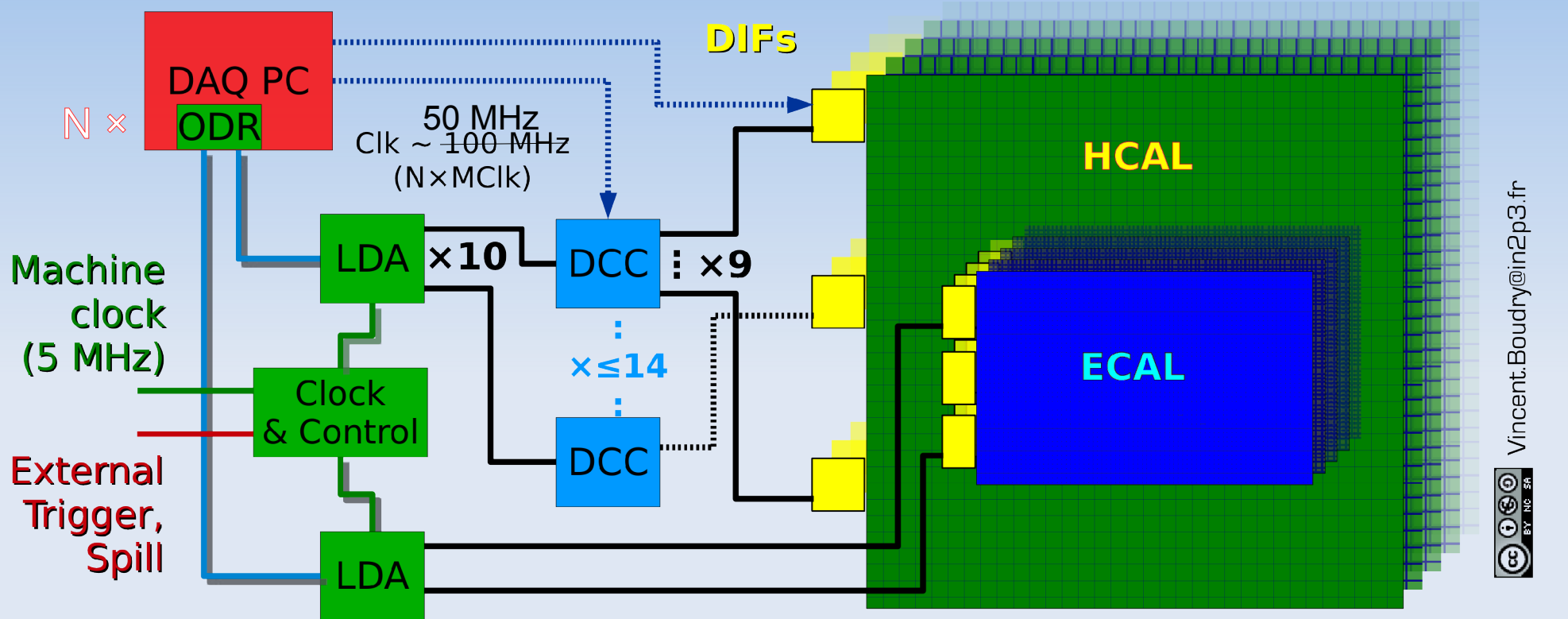
Legend:
- LDA-DIF on HDMI (Config, Control, Data, Clock, Trig, Busy, Sync)
- Clock, Trig, Busy & Sync on HDMI (compatible LDA-DIF)
- Optique (alt. Cable) GigE
- Debug USB
- External Trigger

ODR = Off Detector Receiver
LDA = Link Data Agregator
DCC = Data Concentrator Card
DIF = Detetcor InterFace
CCC = Clock & Control Card

HW availability

Card	#Avail	#Tested	#OK	Remark	
					All basic HW avail.
PC	6	6	6	OS needs upgrade	
ODR	10	4	4	(commercial board: no expected default)	
LDA	25	22	17		
HDMI Mezzanines	30	24	**13**	4 have faulty connectors and are being repaired. Not all cards have 10 conn. working	
GEth mezzanines	25+5	25	20	2 can easily be recovered	
CCC Adapter	25	17	16	Limits # of installations	
CCC	10	10	**10**	term adaptation maybe be needed	
DCC	2+20	22	21	1 faulty channel on 1 card; 1 burned to be repaired	
ECAL DIF	29	29	29	equipement for ~20 additional ones avail.	
SDHCAL DIF	190	190	185	2 dead ; mods needed for HR2 (ok for HR2b)	
AHCAL DIF	4*			*Being produced	

Complete list of HW pieces & location available on https://twiki.cern.ch/twiki/bin/view/CALICE/HardwareList

News from Matthew Wing:

- Remaining ECAL DIFs: We have **produced 20** *(ver. 2)*, with 10 each in system tests at LLR and UCL. The **remaining 20** will be produced soon. The people at Cambridge have another job to do at the moment, so if you want to give us a time-scale, that's fine, otherwise they will be done soon.

- CCCs. We are in the process of sending two more cards to Guillaume. This will mean that 9 have been distributed and we'll keep one at UCL.

- HDMI cables. We recently bought 50 cables and have distributed many of them. These were pretty cheap and we got 2m cables. The specs can be found at : http://www.toby.co.uk/content/catalogue/products.aspx?series=TRB-HH-C-xM

  - ▶ rem: 40 @ LLR ; not halogen free.

- The firmware for the trigger and busy and for the HDMI connections is done, as per Matt's e-mails. We consider that we have done as much firmware as our time will allow and are concentrating on getting the various bits of hardware tested and sent out.

- The hardware page in the twiki should be reasonably up-to-date, although we are checking this. And as said above we are going through all the loose ends, doing tests and will distribute all components. I assume we will send them all to LLR.

  - ▶ To everyone: please this page up-to-date
    https://twiki.cern.ch/twiki/bin/view/CALICE/HardwareList

Cables

Preliminary

- CERN requires halogen free cables
    - "IS23 does apply to above-ground installations and experiments."

- On shelf: only for HiFi freaks (or Pigeons):
    - beautiful 100€ apiece 5m-long shielded HDMI cable

- 1 reasonable offer (by Franck)
    - On demand PolyEthylene LSOH coating
    - ~ 25€/cable (5m long, ∅ 8.5mm) for 200+ cables.
    - pbm: 12 weeks delays (8wks by plane, +30%)
    - ~ enough funds on ANR to buy for the m^3 SDHCAL (150 needed)
        - Urgent : 12 weeks delay due to boat shipping from China
        - Other demands being surveyed:
            - µMegas (~30 ?)
            - AHCAL (50) and ECAL (30)
            - + 10% spares (enough ?) → 260–275
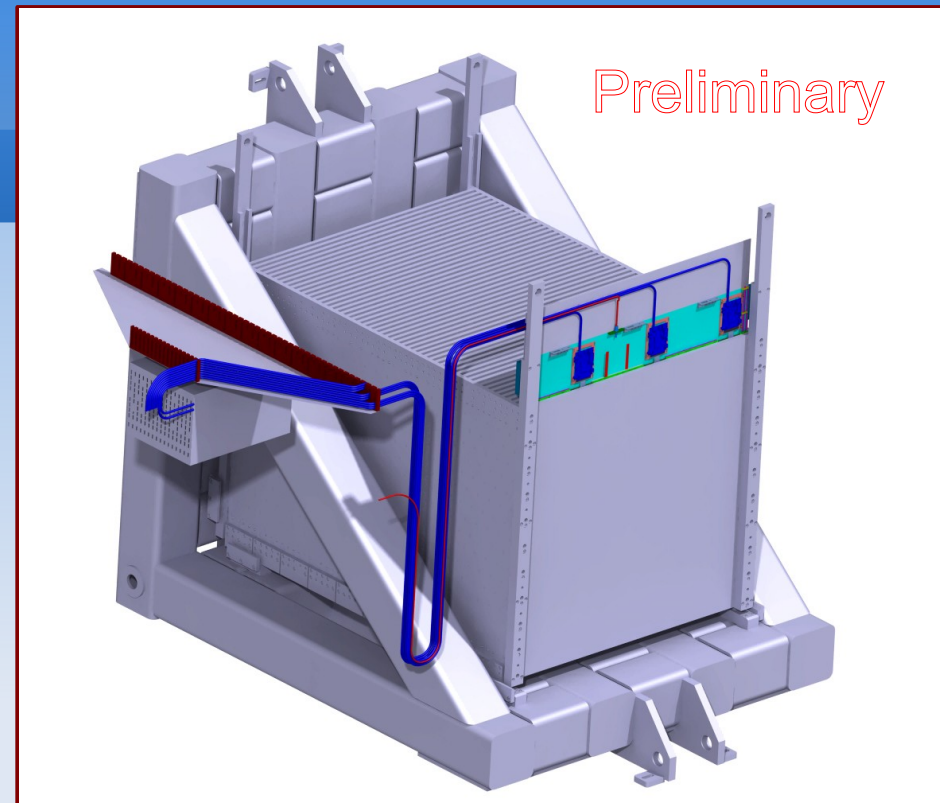
Check F. Davin presentation

Order today

FW Performance Map

F. Gastaldi (LLR) + M. Warren (UCL)

	LDA	DCC	DIF's
Ethernet	✔ at full speed		
CCC	Clk; Trig; Busy	Clk; Trig; Busy	Clk; Trig; Busy
Nlinks up	10 MUX OK @ 25 MHz Still instable for >6 @ 50MHz	9	1
Fast Commands	✔	✔	✔
Block transfert (Config loading)	✔	✔	✔
Data	✔ (< 50 MHz)	✔ (< 50 MHz)	✔ (<50 MHz)
ROC			Structure ✔ Adapt SDHCAL USB Config loading ✔ Rest on going

Generic code for all DIFs
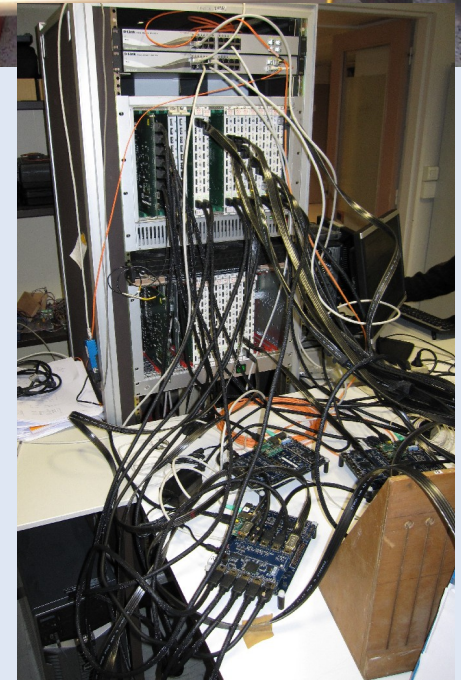G. Vouters (LAPP)+ R. Cornat (LLR)

Integration tests

- Working Bench test @ UCL, LLR, Cambridge and **now LAPP* and IPNL**

- Whole chain established :
  DAQ PC with ODR ⇔ LDA ⇔ DIF and CCC source

- Multiple 10 DIF ⇔ LDA links established @ high speed

- FastTrig and Busy signals functional.

@UCL

PC +ODR

ECAL DIFs

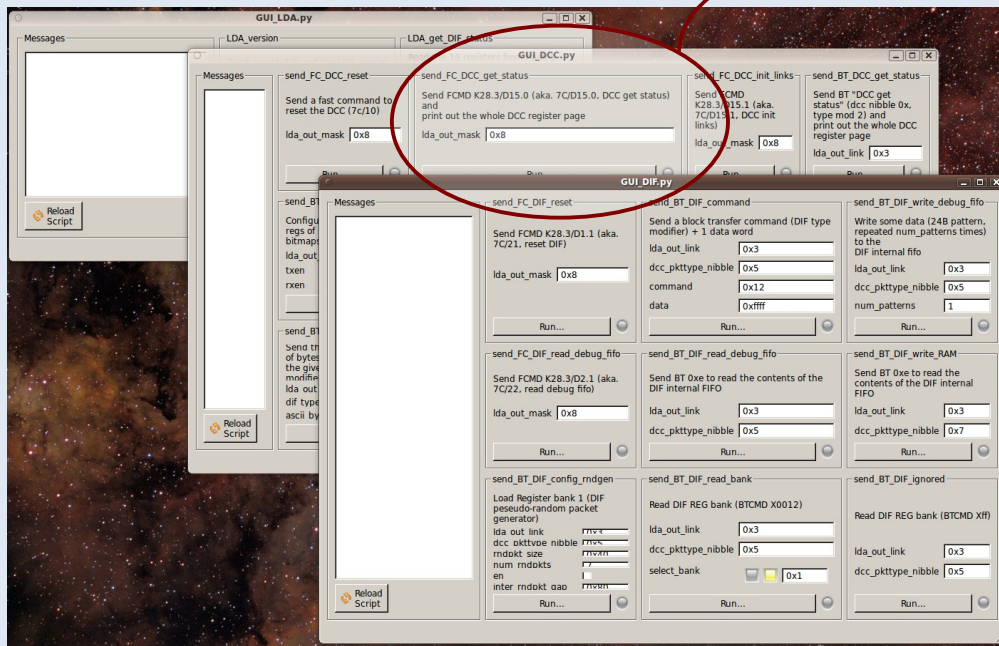ECAL FEV7
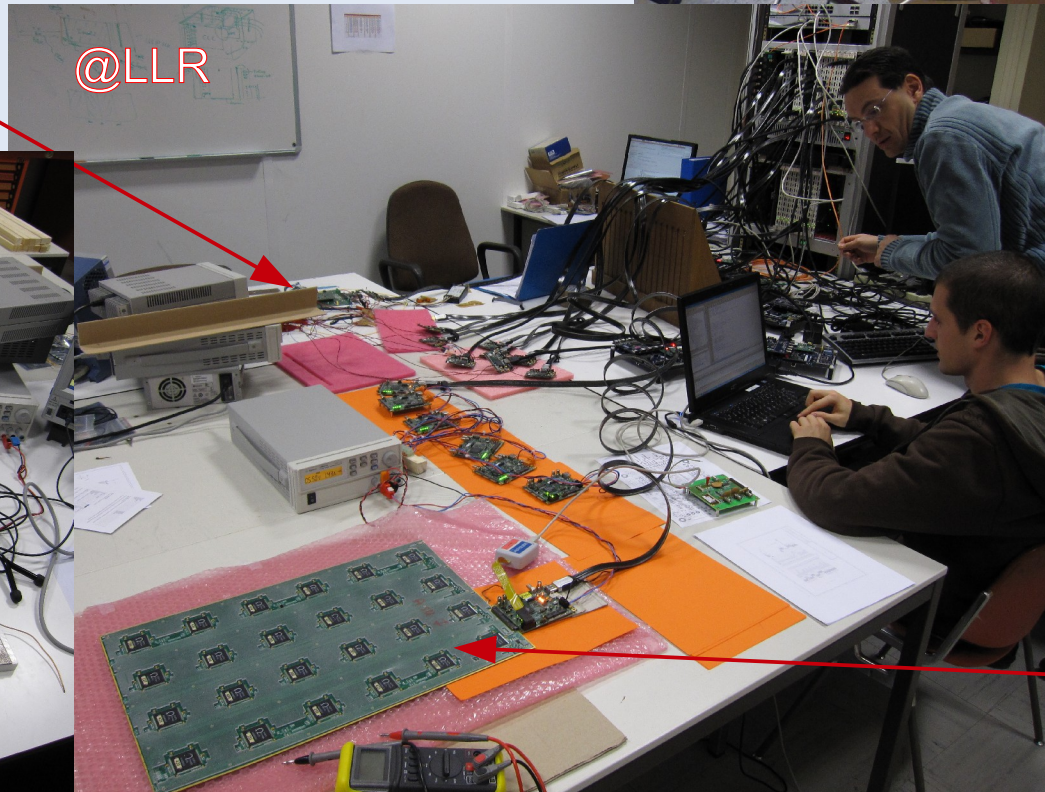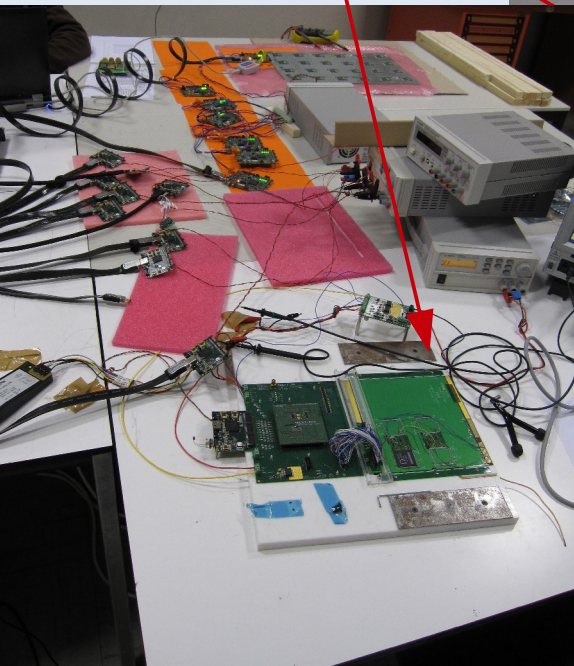
@LLR

RPC SDHCAL ASU

Somewhat "limiting factor"

Python Test toolkit

D. Decotigny → N. Roche

- **Interactive hardware test software (GUI)**
  - ▶ Each HW test easily scriptable: simple user-friendly python API: each function defined ⟷ 1 graphical pane with "Run" button
  - ▶ Available to anyone working with USB/RS/Ethernet devices

- **C libraries implementing the complete DIF Task force protocole → API**

https://svn.in2p3.fr/calice/online-sw/trunk/pyserdiag/

SW status

- Missing critical elements
  - ▶ Configuration DB (being worked on)
  - ▶ DAQ2 interface ↔ XDAQ being worked on
- Missing ancillaries
  - ▶ Semi-automatic noisy channels spotting & correcting (monitoring)
  - ▶ Clean Slow control
  - ▶ interface to CondDB;
  - ▶ event display : DRUID on LCIO file
  - ▶ interface to the GRID
  - ▶ interface to the machine (⊃ in AIDA WP8.6.2) Code exists in DAQv1

Implemented
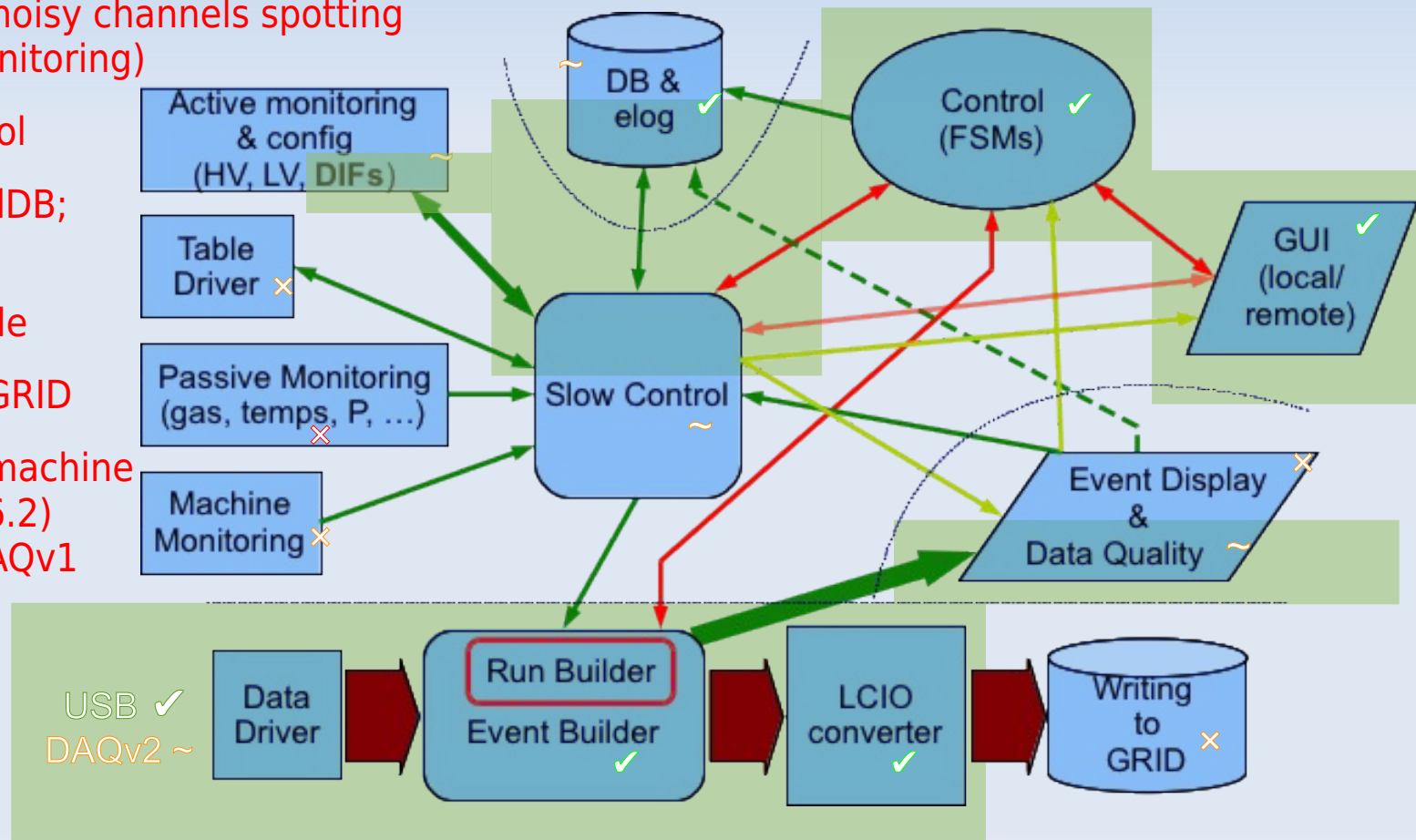
Pending questions for test beams

- November test with CALICE ECAL φal prototype → requires big adaptations
  - readout of CRC (VME 9U)… in xDAQ or in DAQv1⊕ DAQv2
    - Exp. from WHCAL + μMegas for HW sync → Idem or use a EUDAQ TLU ?
    - Much work for the SW: Paul not necessarily available
- Slow Control
  - DIM
    - tº measurement
    - pressure meas
    - HV
    - Humidity
- Machine interface
  - code available in DAQv1 (Sven Karstensen from DESY)
  - probably to be improved (slow) ↔ part of AIDA task
  - Readout of machine events → BIF card.
- Performances for μMegas : 4 partitions × no rate limitations → Highest BW ?

Pending questions for test benches

- Adaptation of configuration files (HR → Spiroc & Skyroc; µROC should be transparent)
- Adaptation of xDAQ online loops (threshold scans, calibration signal, …)
  - ► auto generation of config files
- Quick online analysis
  - ► Adaptation of DHCAL Marlin tools → pseudo online analysis.
- Priorities ?

Conclusion

- All HW is there and working "well enough"
  - ► Dispatching started (LLR, IPNL, LAPP, DESY)
  - ► still some non-perfect parts (esp. LDA)
    - ◆ extensive test of all LDA to be done
- Last two critical missing interfaces in good progress (∫ early january)
  - ► ROC handling through HDMI
    - ◆ allow for config loading
  - ► DAQv2 HW ↔ xDAQ driver
    - ◆ allow for heavy load testing of DAQ SW.
- Still much work needed on the SW side (check Laurent's talk)
  - ► Slow control to be developed (IPNL & LLR)
    - ◆ // development on ECAL now possible when SW adapted...

Spares

Clock and Control Card

- Developed at UCL (M. Warren, M. Postranecky)

- Distributes on 8 channels (HDMI, SMAs, NIM, …) via dedicated circuitry for **low jitter**
  - ▶ Int | ext clock
  - ▶ Fast Signal (Trigger | Sync)

- Sums-up BUSY

- Performs Trigger logics
  - ▶ CPLD

- Was used as DIF-Master (dev[t] of LAPP)
  - ▶ Aka also sending hard-coded commands to DIF directly
  - ▶ Standalone tests with USB readout
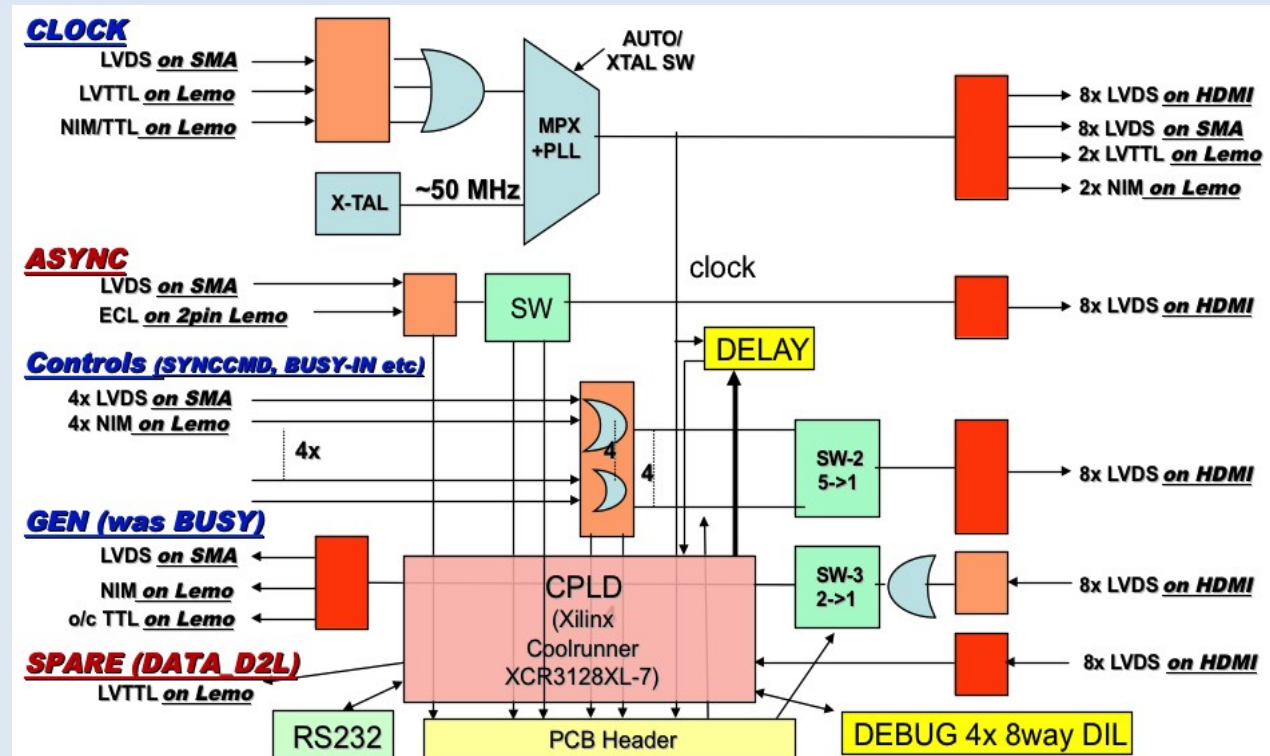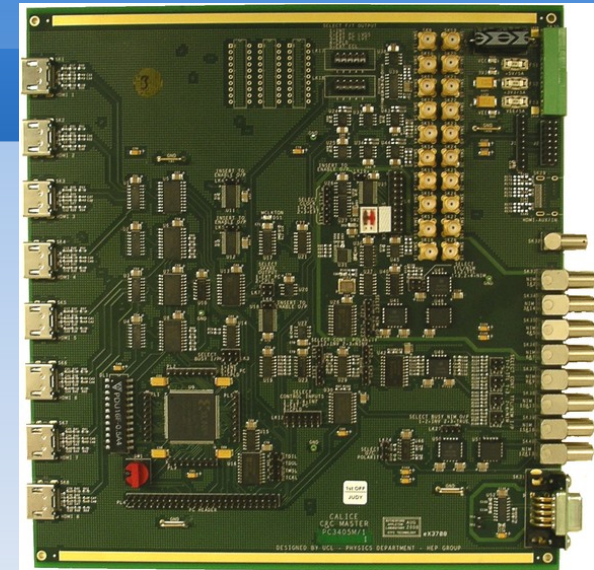
Software: XDAQ framework

- dev[ts] started @IPNL for electronics test using XDAQ in 2008
  - ► Ch. Combaret (IPNL)
  - ► Gained (a lot of) impulsion with involvment of L. Mirabito (resp. of DAQ SW for CMS tracker)
- Ran for ≥ 1 year in TB, Cosmics & Electronics test
  - ► USB readout
  - ► Interface to old LabView program
- Recent development
  - ► Writing of LCIO data in RAW format
  - ► versatile online analysis framework (root histos)
    - → Marlin Based
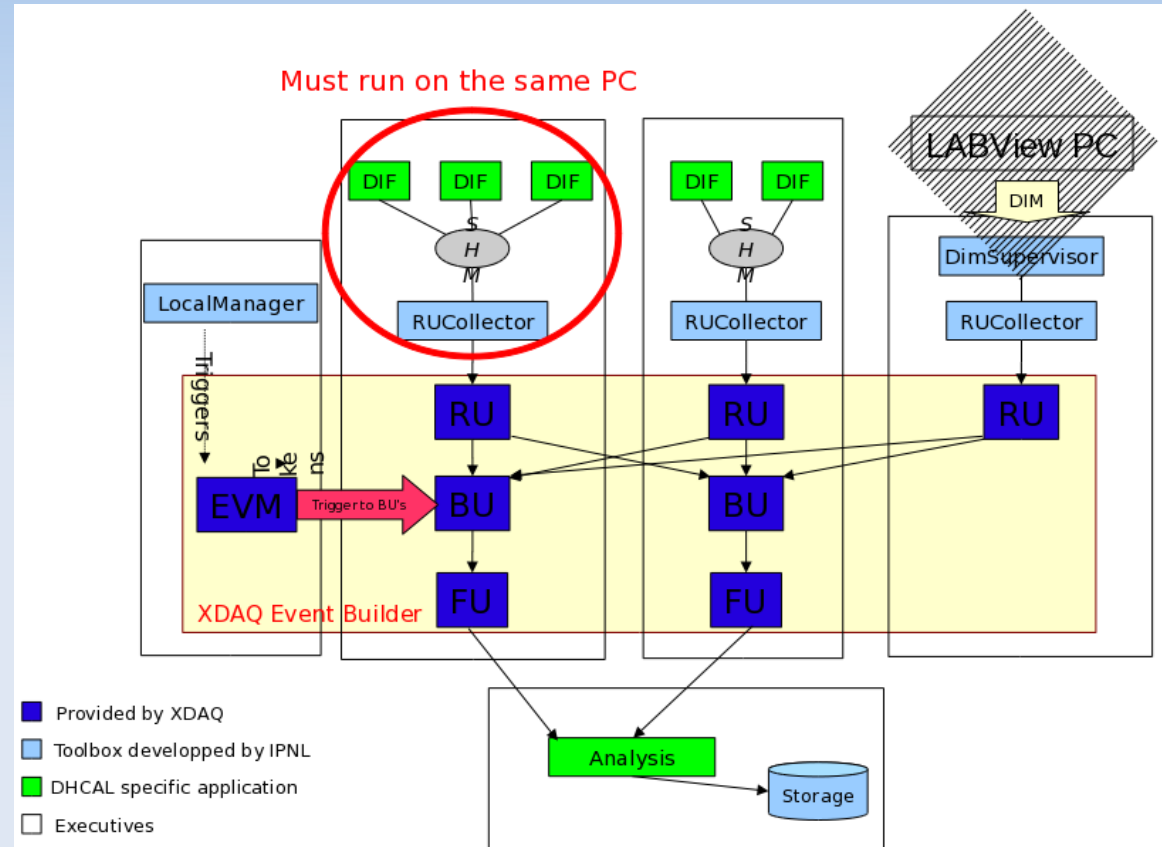
IPN Lyon

Performances

- Rather low demands in term of bandwidth
  (but >> @ ILC for same vol.)
  - ► SDHCAL : ~ 20MB/s in Spill
  - ► ECAL: ~100MB/s
  - ► AHCAL: ~ 300 MB/s
- **Data limited by ASICs readout**
  - ► Modes:
    - ◆ test beam single event
    - ◆ Test beam burst (≈ ILC-like mode)
- Some code (System C, by D. Decotigny) exists for simulation of full chain
- Full scale test scheduled (L. Mirabito)

DAQv2 data flux

N DIF/LDA	N DIF/DCC	LDA-DIF Dclk [MHz]	LDA-DIF FLUX [MB/s]	LDA Dclk [MHz]	LDA FLUX [MB/s]	ODR FLUX [MB/s]	Disk Flux [MB/s]
10	9	50	6.25	1000	125	1000	170

Detector	**DHCAL**	Evt Size	Mem Size	ASIC Dclk [MHz]	ASIC FLUX [MB/s]
		20 B	128	2.5	0.31

from LC-DET-2004-029

Mode	Calib/Noise Single	Calib/noise Burst	TB Single	TB Burst	Demo
N ASIC/DIF	48	48	4.8	4.8	4.8
σ (NASIC)	0	0	2.6	2.6	2.6
Touched DIF/pla	3	3	1	1	1
ASIC	20 B	2 560 B	20 B	2 560 B	2 560 B
R/O time 1	64 μs	8 192 μs	64 μs	8 192 μs	8 192 μs
R/O time ALL	3 072 μs	393 216 μs	307 μs	39 322 μs	39 322 μs
DIF	960 B	122 880 B	96 B	12 288 B	12 288 B
R/O time	154 μs	19 661 μs	15 μs	1 966 μs	1 966 μs
LDA w/o DCC	9 600 B	1228 800 B	320 B	40 960 B	40 960 B
R/O time	77 μs	9,830 μs	3 μs	328 μs	328 μs
DCC	8,640 B	1,105,920 B	288 B	36,864 B	36,864 B
R/O time	1 382 μs	176 947 μs	46 μs	5 898 μs	5 898 μs
LDA w/ DCC	86,400 B	11,059,200 B	2,880 B	368,640 B	368,640 B
R/O time	691 μs	88 474 μs	23 μs	2 949 μs	2 949 μs
ODR	172,800 B	22,118,400 B	5,760 B	737,280 B	737,280 B
1000MB/s	173 μs	22 118 μs	6 μs	737 μs	737 μs
Disk	172,800 B	22,118,400 B	5,760 B	737,280 B	737,280 B
170MB/s	1 016 μs	130 108 μs	34 μs	4 337 μs	4 337 μs
Max R/O time	3 072 μs	393 216 μs	307 μs	39 322 μs	39 322 μs
Min Freq	0.33 kHz	0.00 kHz	3.26 kHz	0.03 kHz	0.03 kHz
Min. evts Freq		0.33 kHz		3.26 kHz	3.26 kHz

Occupancy for 100 GeV π in TB evts

Mean	4.8
sigma	2.6
+3σ /√MemSize	5.49

Parameters codes
- Hardware (~fixed)
- DAQ (achievable)
- Physics (occupancies)

19MB/s

Reliability tests

Stress tests using pseudo-random generator

- 9×DIF → 1×DCC → 1×LDA → PC
    - ▶ 9 DIFs (ECAL & SDHCAL) generate pseudo random data
- Results
    - ▶ Direction DIF → LDA ✔
    - ▶ Maximum DCC → LDA link occupancy (40Mbps) ✔
    - ▶ Up to 5.6 TB transferred (2 weeks), no error

End-to-end test: FIFO write/read

- PC ↔ 1×LDA ↔ 1×DCC ↔ 1×DIF
    - ▶ Tests both fast-commands and block transfer "read" requests
- PC ↔ LDA Ethernet OK
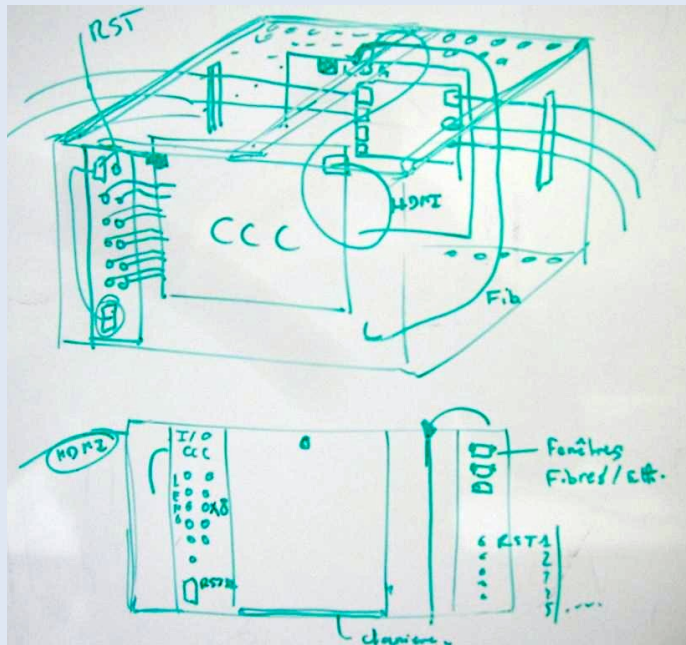
ROC config loading & checking ✔

To be done

- FW

  - Stress tests of LDA (needed: HW sometimes uneven)

  - SW: recognition & recovery of HW failures (plug-in / out)

  - Measurement of Clock & trigger dispersion

- HW support for CCC & LDA

  - LDA mechanics "unconventional" and fragile

F. Gastaldi, N. Roche

(longueur = 22.5 cm : Largeur = 14.5 cm; hauteur = 6 cm)

ALIM | Fibre Ethernet | HDMI CCC | Reset

HDMI DCC

HDMI DCC

HDMI DCC

HDMI DCC

HDMI DCC

HDMI DCC

HDMI DCC

HDMI DCC

HDMI DCC

HDMI DCC

$\rightarrow$ **M. Anduze**
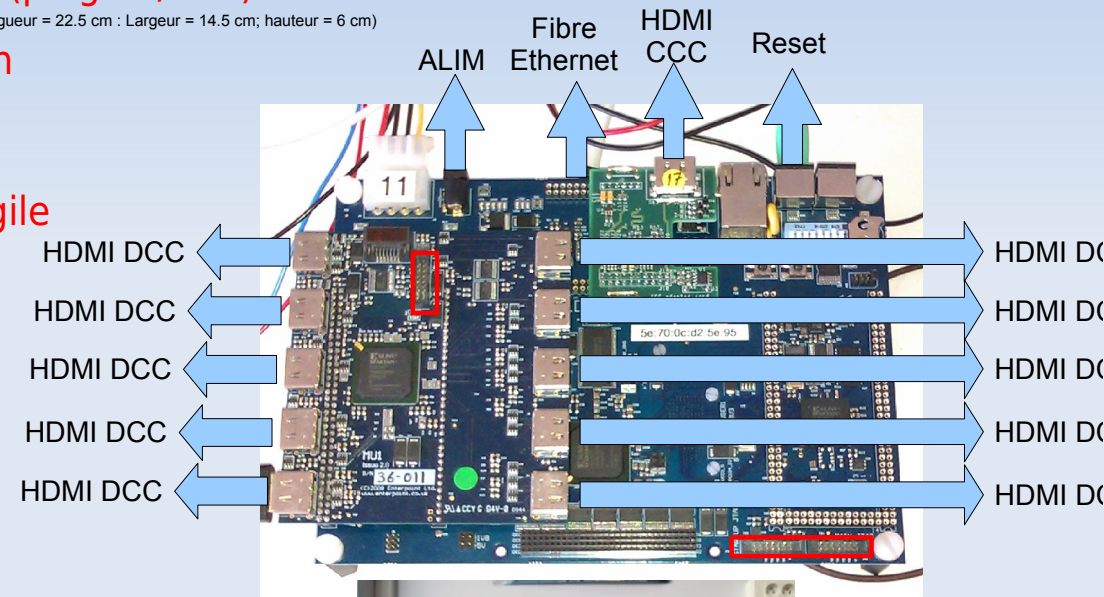
- Man power available, no show stopper…

FW status

- DCC : not much to say

  - ▶ 1 card with 1 channel to be repared

  - ▶ 1 card with P/S burned last week

  - ▶ Distribution: 1 @ LAPP, 1 @ IPNL

- LDA

  - ▶ Still some problems: not all channels working on all cards (HDMI mezzanine "tricky")

    - ◆ Works @ 25 MHz

    - ◆ Unstable @ 50 MHz with triggers (passing nearby) on some channels

  - ▶ Multiplexing working fine on 6 channels (long running),

    - ◆ somewhat OK on 7 (several days),

    - ◆ problematic on 8–10 channels (blocking of card @ high data rate)
      but OK with pauses in data flux (as it should be the case for TB).

- CCC

  - ▶ ~OK

    - ◆ with 1 µs-long signals (due to AC coupling)

    - ◆ Jitter on all chain to be measured… (no pbm for SDHCAL)

DIF FW

- FW still in building:
  - ▶ Done:
    - ◆ Data pseudo-random pattern sending
    - ◆ Config reception, storing and echoing
    - ◆ Config of ROC chips (on RPC ASU, ECAL FEV7) with X-Check yet
    - ◆ Soft Reset
    - ◆ Trigger/Busy echo
  - ▶ Existing but to be integrated & tested
    - ◆ Readout
    - ◆ State machine for Acquisition
      - • ⊃ BUSY output...
  - ▶ To be done
    - ◆ Data formatting: on-going
    - ◆ Sync mechanism (5 MHz clock out of 50 MHz on trigger signal)

Beam InterFace card

Basis:

- CALICE chips use auto-trigger

  - ► Readout can be triggered by single event using external trigger (e.g. beam hodoscope)

    - → "Single event" mode

    - History of Chip is usable (e.g. in case of selective ext. trigger)

  - ► Readout triggered by environmental internal or extern trigger

    - ◆ Chip full

    - ◆ ILC-like mode (end-of-spill)

- Require some device to readout the beam line parameters

  - ► Scintillators; Cherenkov PM (coding of CEDAR bits)

  - ► Time of event (⊃ rec for wire chambers) within a 5 MHZ clock period

Implementation

- 2 solutions

  - ► Add-hoc card for interfaces with a CALICE ROC (SPIROC ?) + 1 DIF

  - ► Small adaption (buffers) card on a DIF + "simulation" of a digital ROC in the FPGA

    - ◆ Part of the coding can be "tricky"

- Both offer full compatibility with CALICE DIF for the DAQv2.

- To be implemented for 2nd version of CALICE beam test

- One of the task of AIDA (WP8.6.2)

  - ► For "standalone" CALICE tests

  - ► Functionnalities ⊃ in JRA1 TLU

Use of sub-ns TDC for CERN wire chambers until then ?