Part of the HW integration

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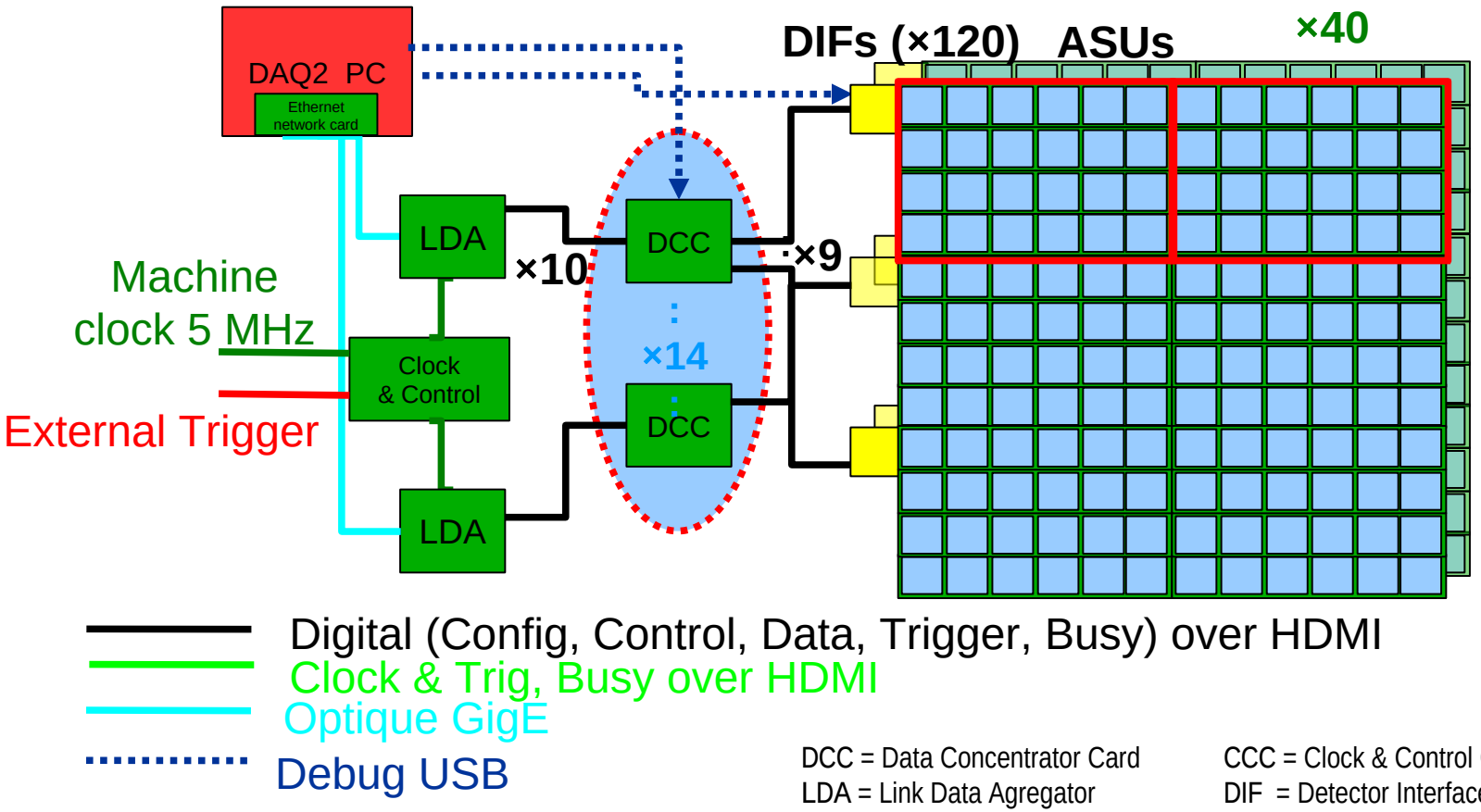
CALICE DHCAL DAQ overview



DCC

Not much to say since Casablanca Calice week

- Firmware : Stable today
- Production:
  For DHCAL, we need 14 cards.
  - 20 have been produced
  - All have been tested;
    - One card with 1 channel have been repaired (capacitor mounted instead of resistor)
    - One card with 1 regulator in default

- Currently, one DCC at LAPP, One at IPNL

Sources available at :
https://svn.in2p3.fr/calice/hardware/trunk/DCC/production/Projet_dcc_prod_hdl/hdl/dcc/

LDA

- There are still some issues to resolve
  - Each channel works independently, but not together :
    - Multiplexing works well on 6 channels (long running)
    - Beyond 6 channels, the LDA is blocked after few data acquisition
      But can work with some pauses in data flux
    - Matt Warren has been able to get all channels with 25 MHz clock
      with 50 MHz, HDMI card introduces a skew between clock and data from channel to channel (next slide)
  - Check the behavior of trigger and busy on DAQ chain regarding the diagram that Matt has sent to us.

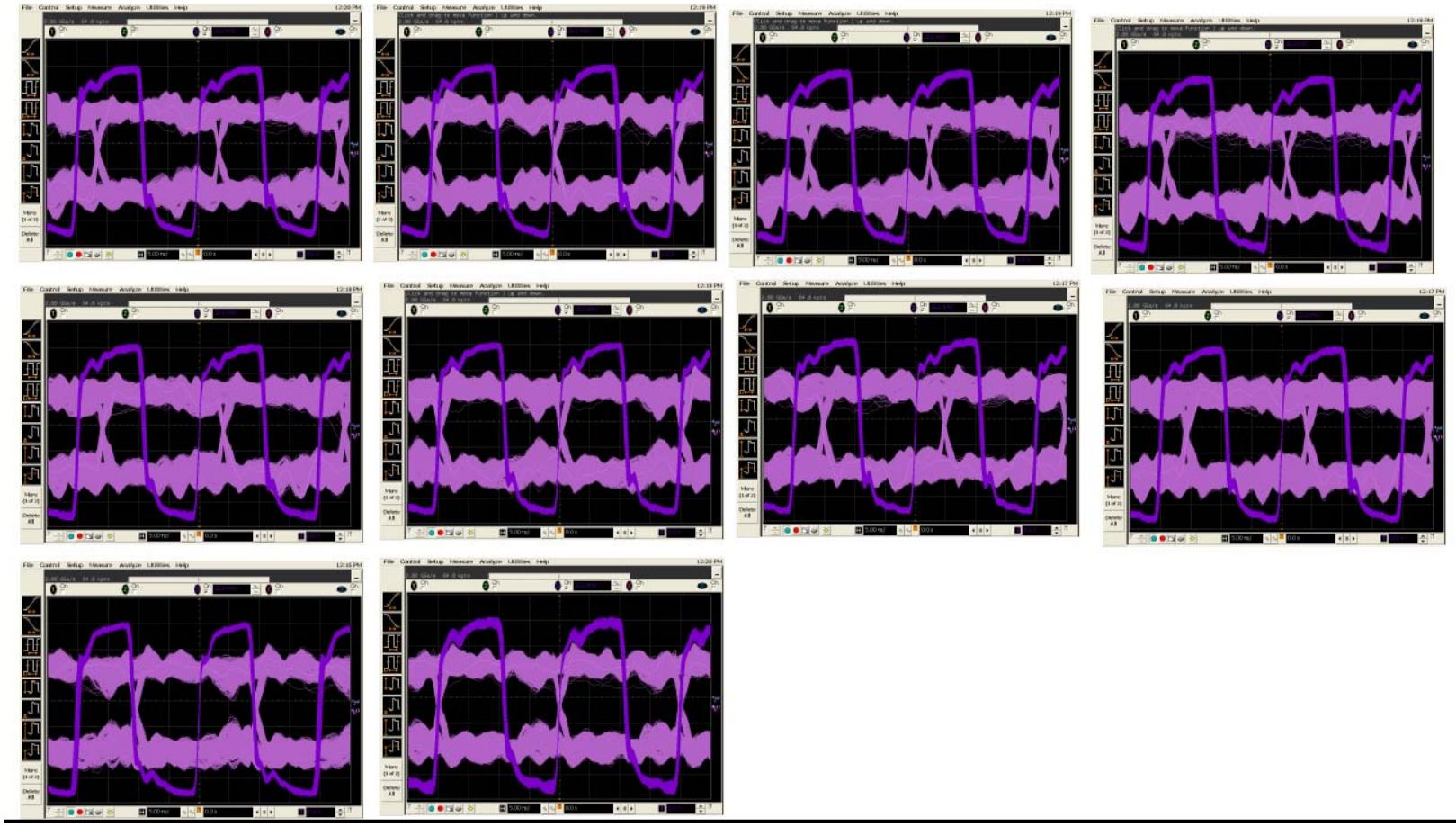
- …For this, we need to make several tests to get a stable firmware

Remark : the LDA firmware contains a XILINX IP Gigabit Ethernet that is obsolete in new ISE version 12.

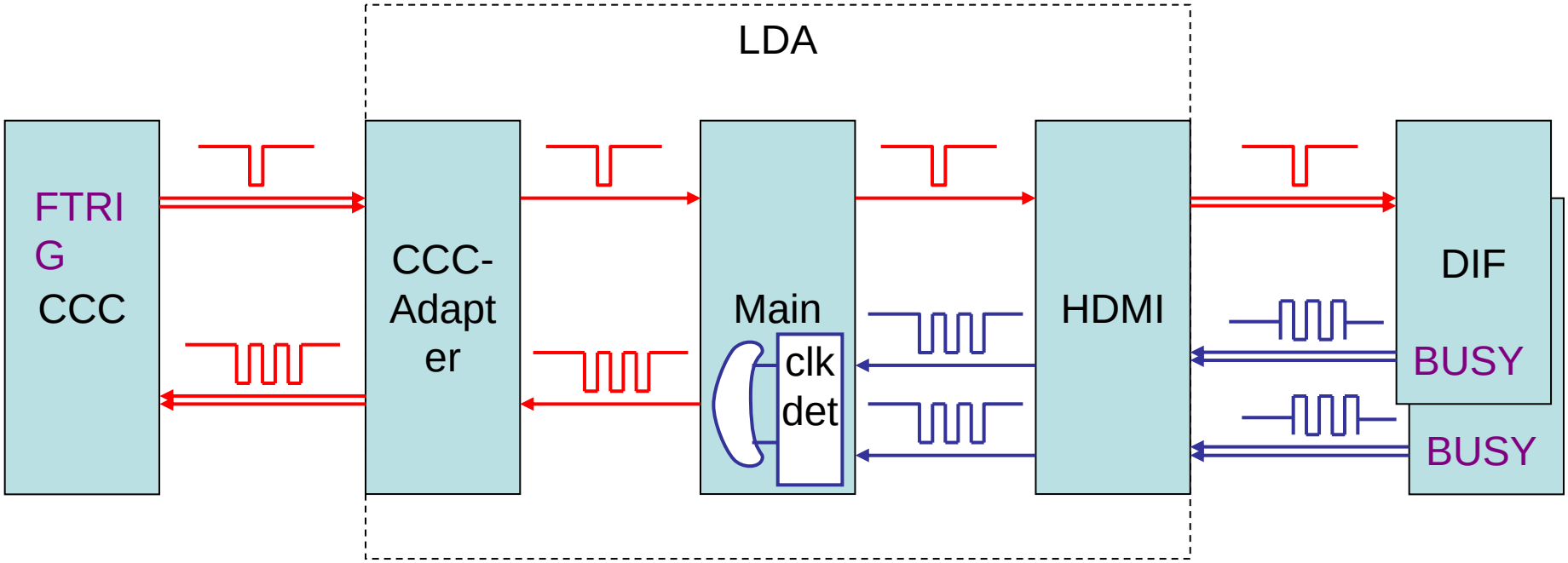
To maintain the LDA, we need to keep ISE version 11, and this IP works only on this version.

Source available at : https://svn.in2p3.fr/calice/hardware/trunk/UK_firmware/LDA/

Skew on hdmi cards (from UK)



Trig, busy diagram (from UK)



Last e-mail from UK

- ECAL DIFs. We have produced 20, with 10 each in system tests at LLR and UCL. The remaining 20 will be produced soon. The people at Cambridge have another job to do at the moment, so if you want to give us a time-scale, that's fine, otherwise they will be done soon.

- CCCs. We are in the process of sending two more cards to Guillaume. This will mean that 9 have been distributed and we'll keep one at UCL.

- The firmware for the trigger and busy and for the HDMI connections is done, as per Matt's e-mails. We consider that we have done as much firmware as our time will allow and are concentrating on getting the various bits of hardware tested and sent out.

- The hardware page in the twiki should be reasonably up-to-date, although we are checking this. And as said above we are going through all the loose ends, doing tests and will distribute all components. I assume we will send them all to LLR.

Hardware list

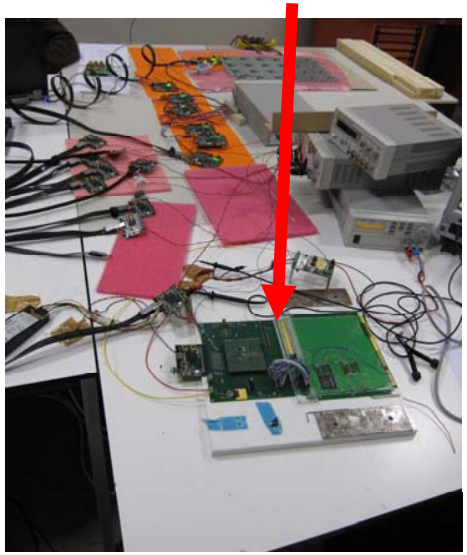
Card	Nb	Status	Location	Notes
LDA	25	15 ok 5 untested 5 failed	9 in UK 8 ok at DESY 4 ok & 2 failed at LLR 1 ok at LAPP 1 ok at IPNL	Failed = stuck in reset or bad contact on Ethernet card
LDA HDMI	30	16 ok 3 partially ok 11 failed	2 partially ok at LLR 1 partially ok at LAPP 8 ok at DESY 4 ok at LLR 1 ok at IPNL Others in UK	Failed = broken pin on connector or no link
LDA Ethernet	30	25 ok 5 failed	8 ok at DESY 6 ok at LLR 1 ok at IPNL 1 ok at LAPP Others in UK	
CCC	10	10 ok	2 at LLR 1 at IPNL 1 at LAPP	
DIF ECAL	22	22 ok	9 at LLR Others in UK	
DCC	20	19 ok 1 Failed	18 at LLR 1 at LAPP 1 at IPNL	Failed = regulator in default

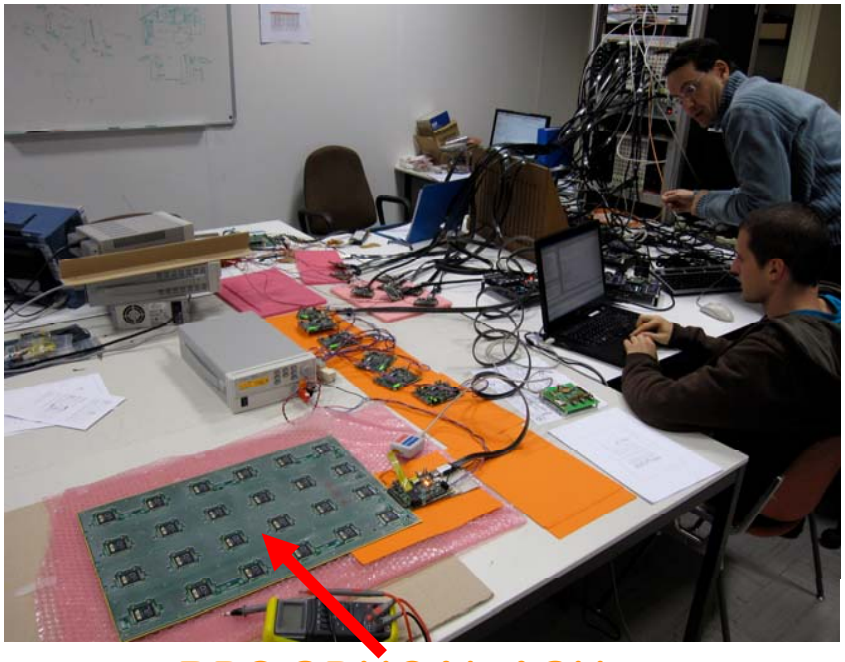
Integration tests

Whole chain establishing :

DAQ PC ⇔ CCC ⇔LDA ⇔ DCC ⇔ DIF

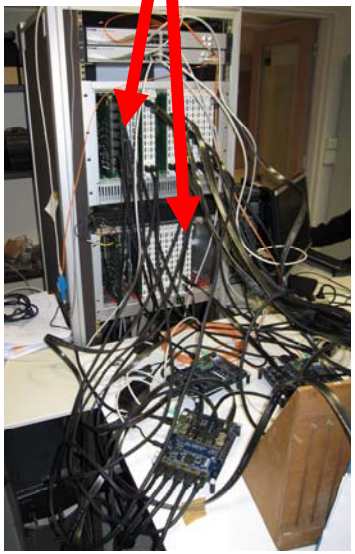
ECAL FEV7





RPC SDHCAL ASU

DCC – CCC crate



Tests

- We make 2 kinds of tests:
  - Functionality tests : Python scripts
  - Intensive tests : C++ language

- Reliability tests
  - Stress tests using pseudo-random generator
    - 9 DIF → 1 DCC → 1 LDA → PC
      - DIF generates pseudo-random data
    - Results
      - DIF → LDA link works correctly
      - Maximum DCC → LDA link occupancy (40 Mbps)
      - Up to 5.6 TB transferred without error during 2 weeks
  - Single test : FIFO read/write
    - PC ⇔ 1 LDA ⇔ 1 DCC ⇔ 1 DIF
      - Tests both fast-command and block transfer “read” requests

- Tests with SDHCAL ASU and ECAL FEV 7
  - Several tests have begun with Guillaume and Remi to check the right transmission of slow control on the ROC.
  - Currently, the slow-control is sent correctly on the ROC but some improvment is necessary to re-read these datas.

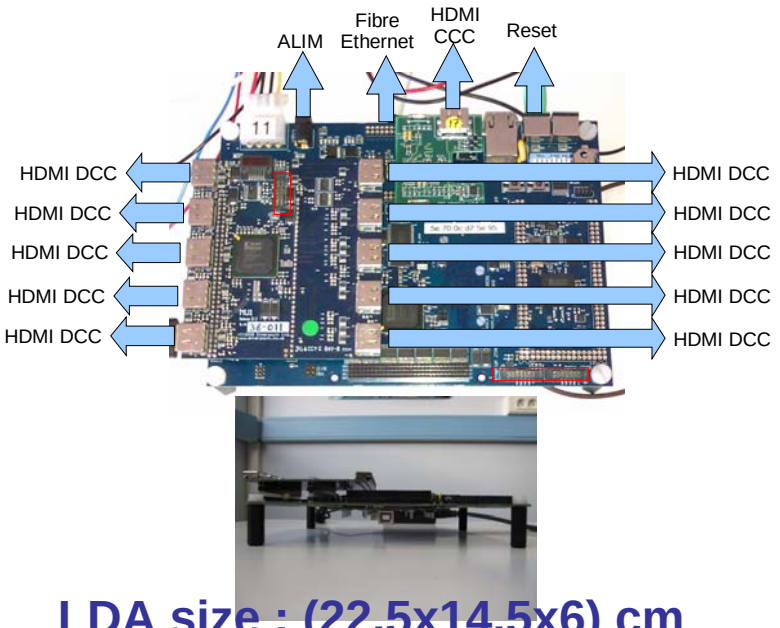
https://svn.in2p3.fr/calice/online-sw/trunk/pyserdiag/examples/llrtests/

Conclusion (to be done)

- Firmware:
  - Intensive tests of all LDA channels
  - Recovery of datas after an hardware failure (plug-in/out connector)
  - Measurement of clock and trigger dispersion between each channel

- Mechanical aspect :

  Resolve Hardware mechanical setup
  CCC and LDA do not have a standard size and the connections on LDA are fragile



LDA size : (22.5x14.5x6) cm