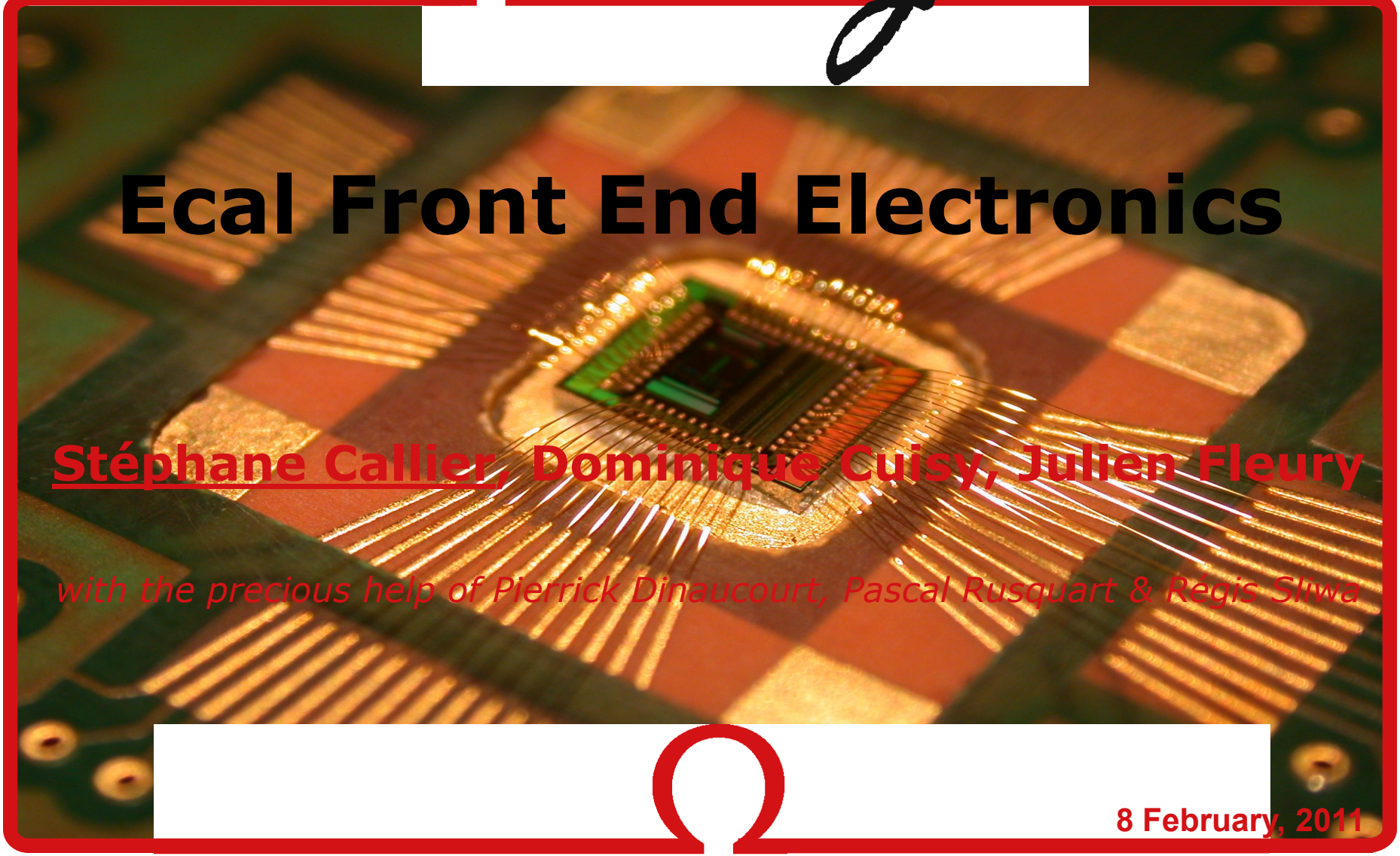
IN2P3 CSNSM

Omega

Ecal Front End Electronics



Stéphane Callier, Dominique Cuisy, Julien Fleury

with the precious help of Pierrick Dinaucourt, Pascal Rusquart & Régis Sliwa

8 February, 2011

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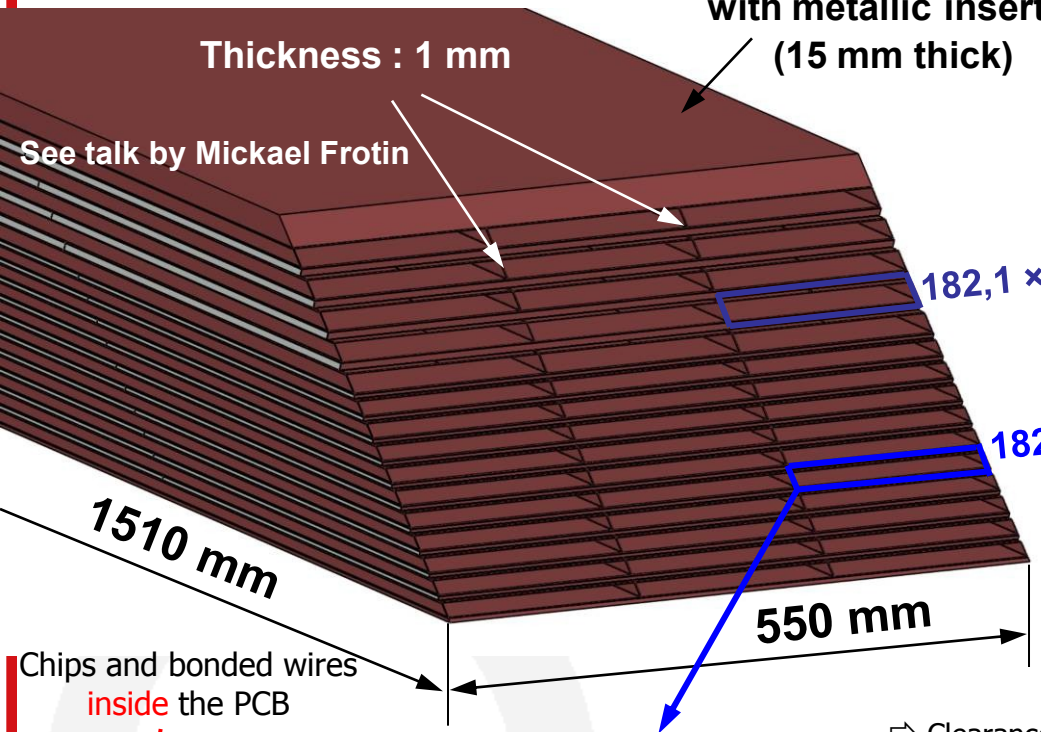
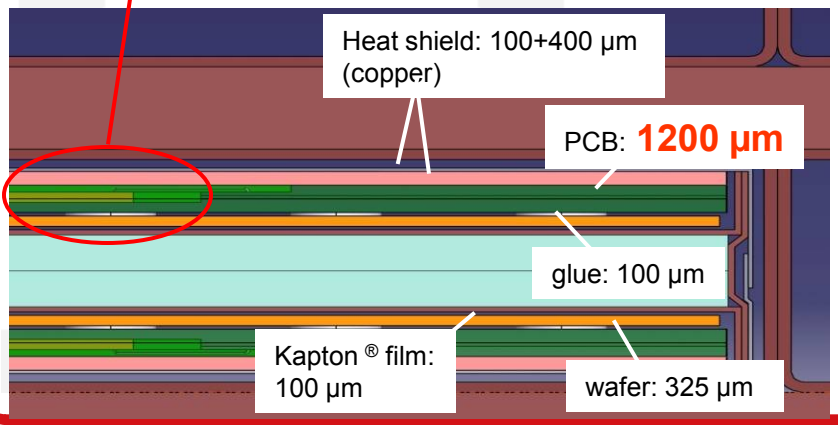
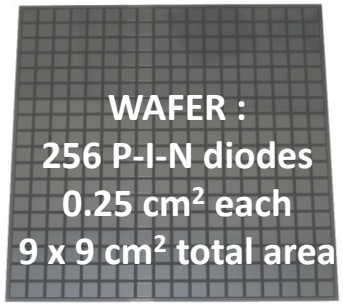
E-CAL DESIGN



See talk by
Jean François Roig



- ⇨ Clearance (slab integration) : 500 µm
- ⇨ Heat shield : **400 µm ?** →
- ⇨ PCB : **1200 µm ?** → design possibilities
- ⇨ Thickness of glue : 100 µm
- ⇨ Thickness of wafer : 325 µm
- ⇨ Kapton® film HV : **100 µm ?** → tests
- ⇨ Thickness of W : 2100/4200 µm (± 80 µm)

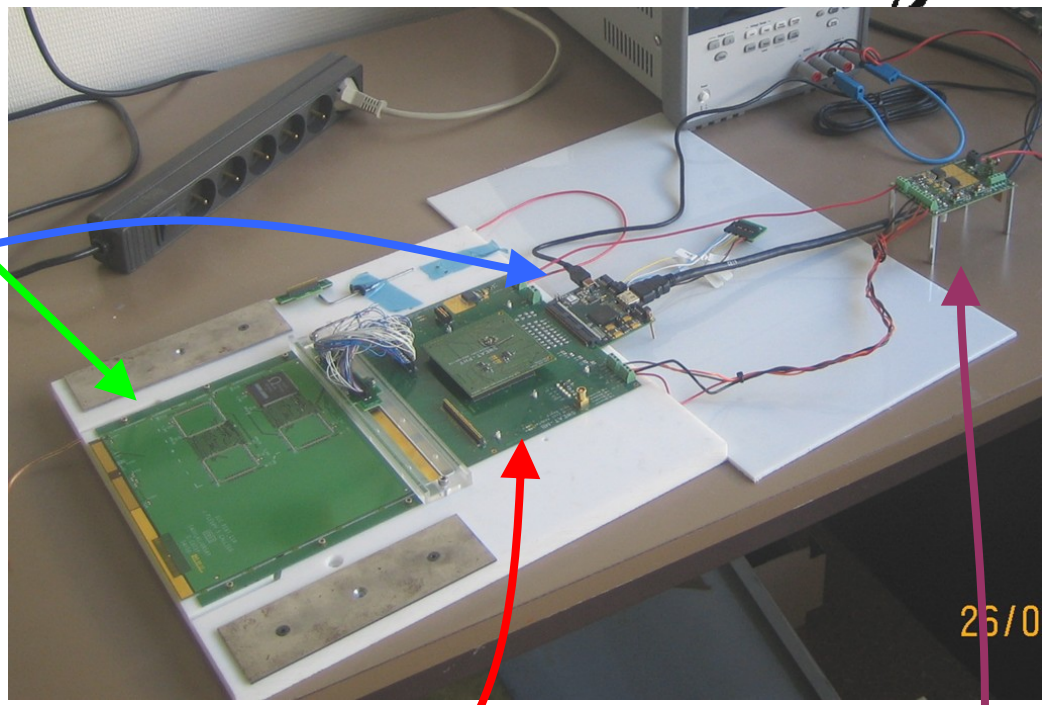


See talk by Remi Cornat

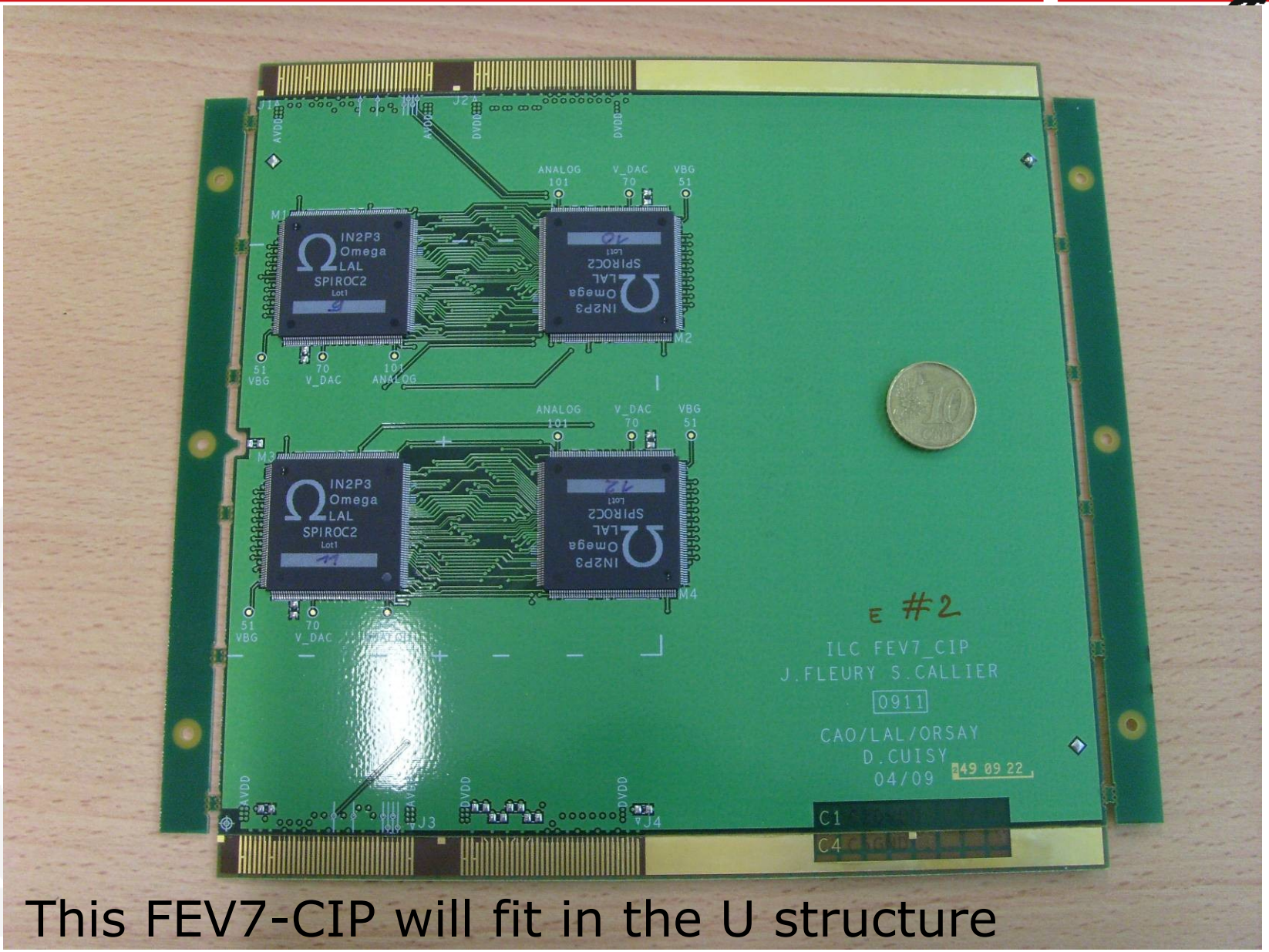
Courtesy :
Marc Anduze - LLR

FEV7s Test Bench

- Test bench @ LLR using now FEV7-CIP (with 1 chip only)
- The DIF is ready to communicate with the adapter board (using HDMI link)
- The adapter board (SWEAT)
  - 2nd version for FEV7 is under study (compliant with cooling system) *[See talk by JF Roig]*
- The power management PCB (necessary due to SPIROC2 slow control loading issues)



FEV7-CIP



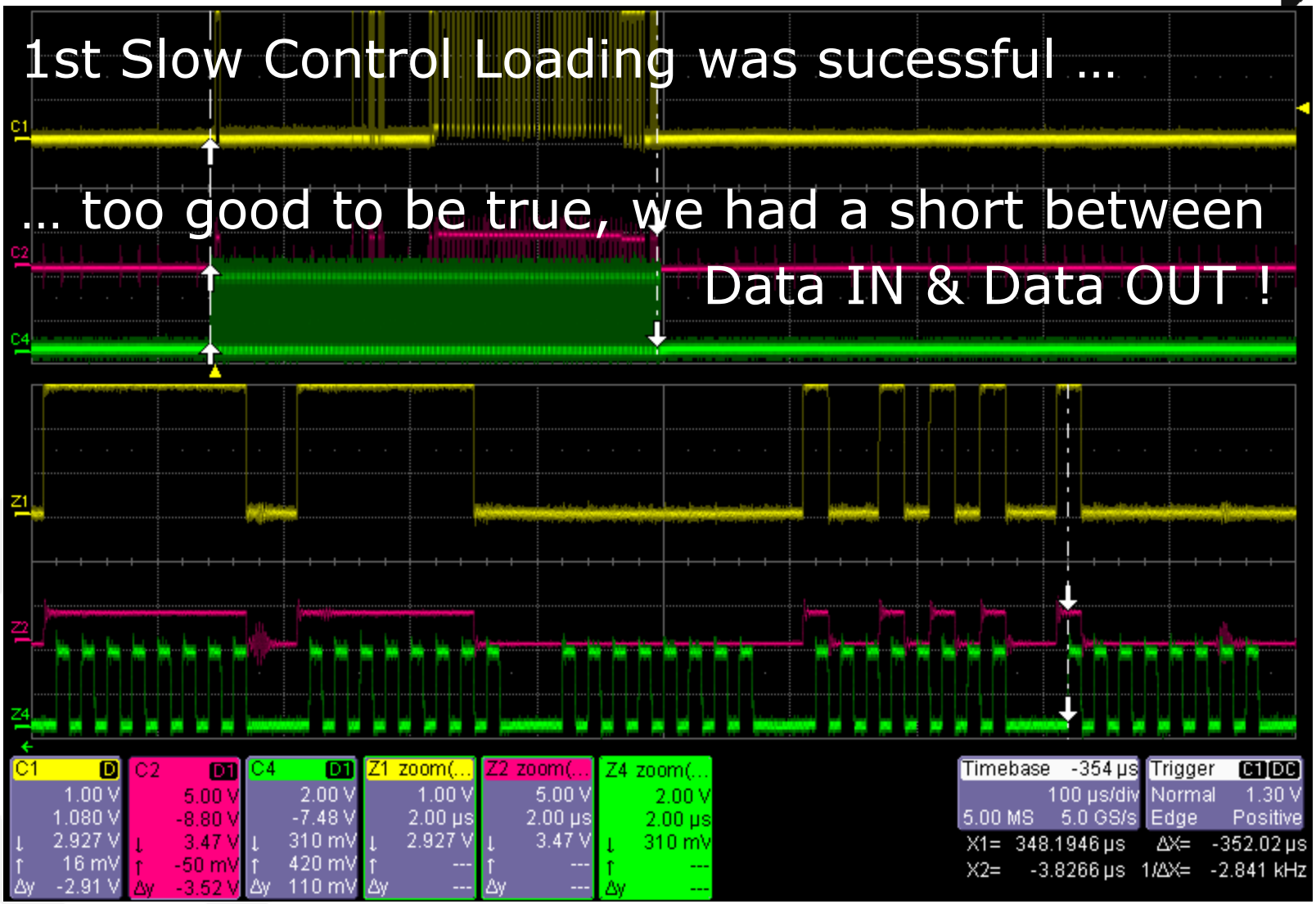
- This FEV7-CIP will fit in the U structure

FEV7-CIP First Tests Setup

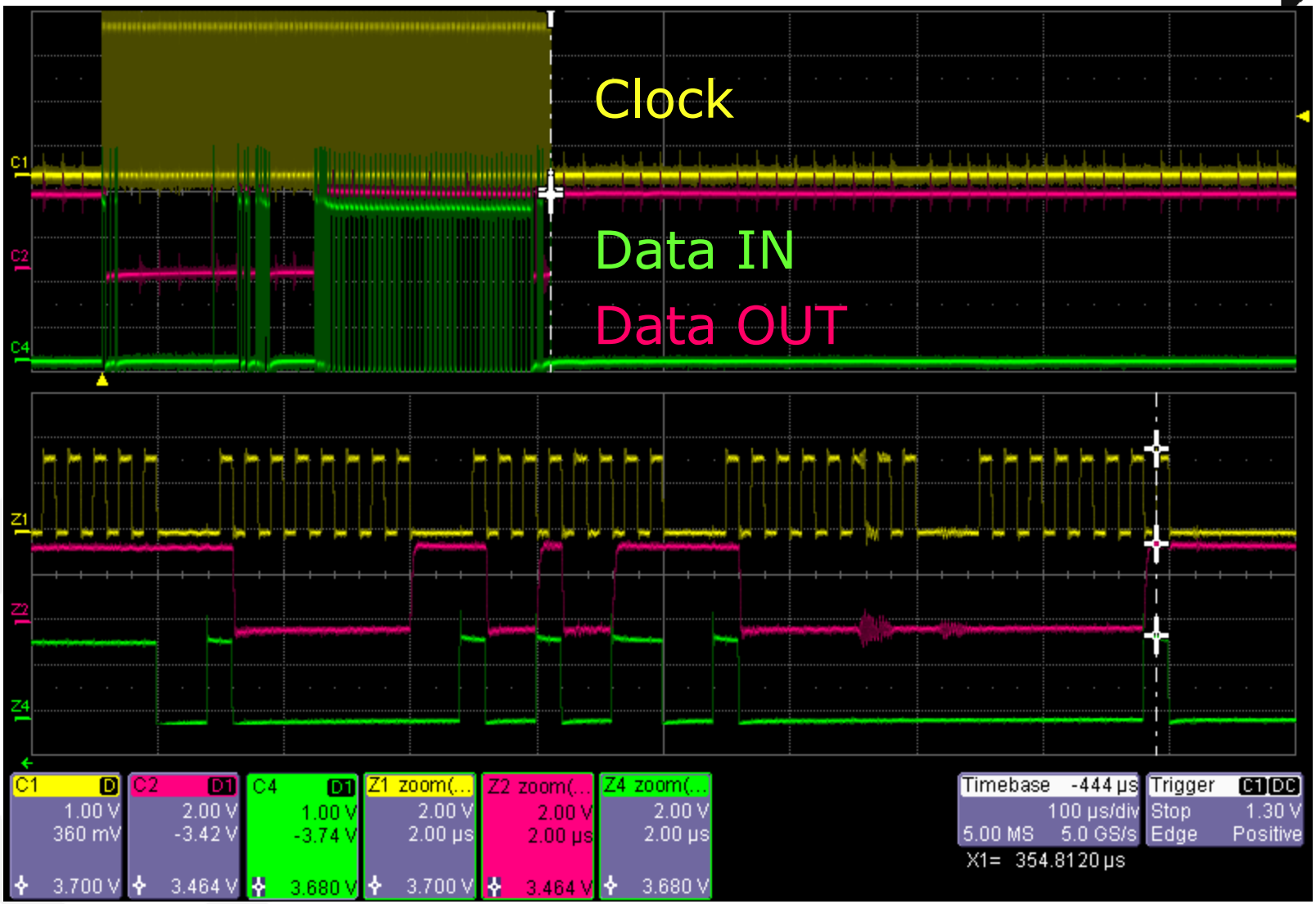
- Thanks to DIF TaskForce (Remi + Guillaume), we have 1 working DIF
- Slow Control files generated by SPIROC2 test software from 1 windows OS Notebook …
- … these files are copied to a Linux OS Computer…
- … where data is afterward loaded in the memory of the DIF by the Python software and finally transferred to the FEV !

  -> Not user friendly !!!

FEV7-CIP with 1chip (Slow Control)

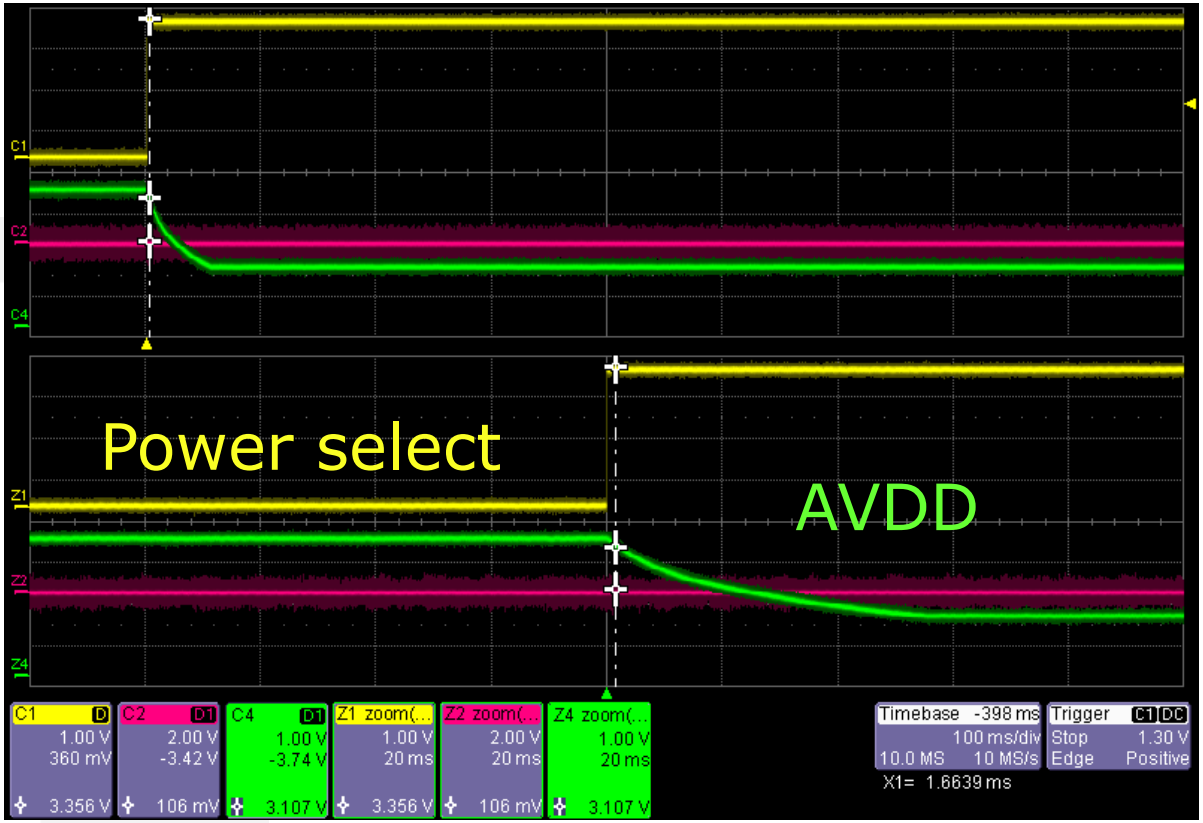


FEV7-CIP with 1chip (Slow Control)



FEV7-CIP with 1chip (Slow Control)

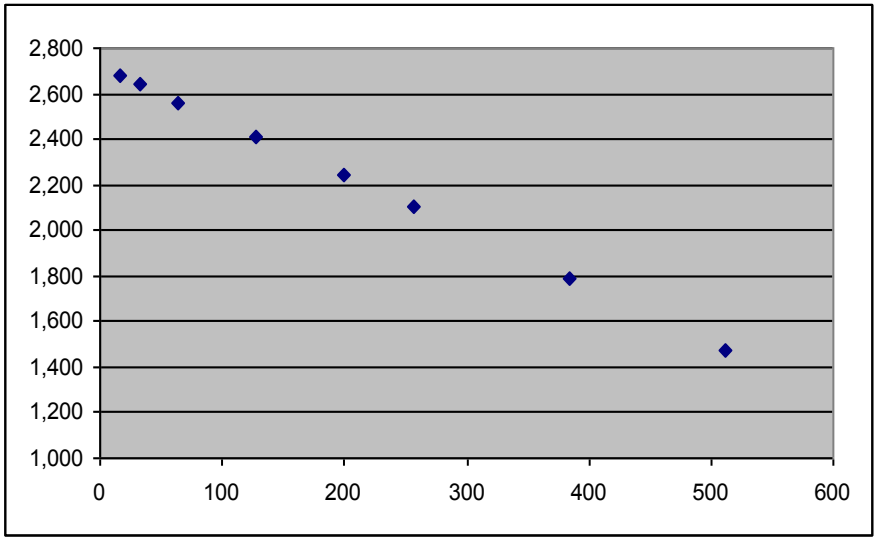
- The power switching needed by SPIROC2 works fine … for 1 ASIC !
  - 60 ms needed to switch AVDD from 3.3V to 1.5V



FEV7-CIP with 1chip

- Bandgap stable @ 2.671V (GND on board = 0.13V)
- We played with POWER_ON_DAC command looking at Bandgap and DAC_Threshold : OK !
- We then launched a COARSE linearity with the procedure described before …

DAC Value	DAC Voltage (V)
16	2,680
32	2,643
64	2,563
128	2,412
200	2,239
256	2,100
384	1,787
512	1,470



FEV7-CIP with …

- …1 chip : We could work that way for the following tests (pedestal hold and conversion using external trigger) but nothing is automated !!!

- …1 chip : How will we perform advanced test ?
  - Calibration test !
  - Which software to control DAQ ? (user friendly requested)
    - Interraction between ASIC's slow control & test performed
  - Who will do that ? (volunteers ?)

- …4 or more chips : How to proceed for the slow control generation ? GUI ? Automated tests ?
  - 80% of the parameters will be identical
  - Chip ID NEED to be different for each devices !
  - Some other parameters can be tuned individually …

FEV7-COB1/2

- For test with FEV7-COB / FEV7-COB2, debug will be even harder due to bonding on PCB !
- Same remark for FEV8 board, which *SHOULD/MIGHT* be a Chip-On-Board version !
- Test with more A.S.U. connected together (up to 7)

-> Need to ask RPC/µmegas DHCAL and AHCAL people for they thought, and use it as a starting point

Summary

- Assuming that :
  - FEV8 board will be COB versions
  - In continuous mode, 1 SKIROC2 consumes 100mA
  - Each A.S.U. has 16 SKIROC2 chips
  - 1 fully equipped long SLAB *would* require more than 10A if not power pulsed
    - Test Beam ? Interconnections ? Adapter Board power supply ?
- Now, FEV7 tests have started, great !
- However, I fear that this could be very time consuming for non optimized results unless we solve the "environment" (GUI software/slow control/data analysis) issue

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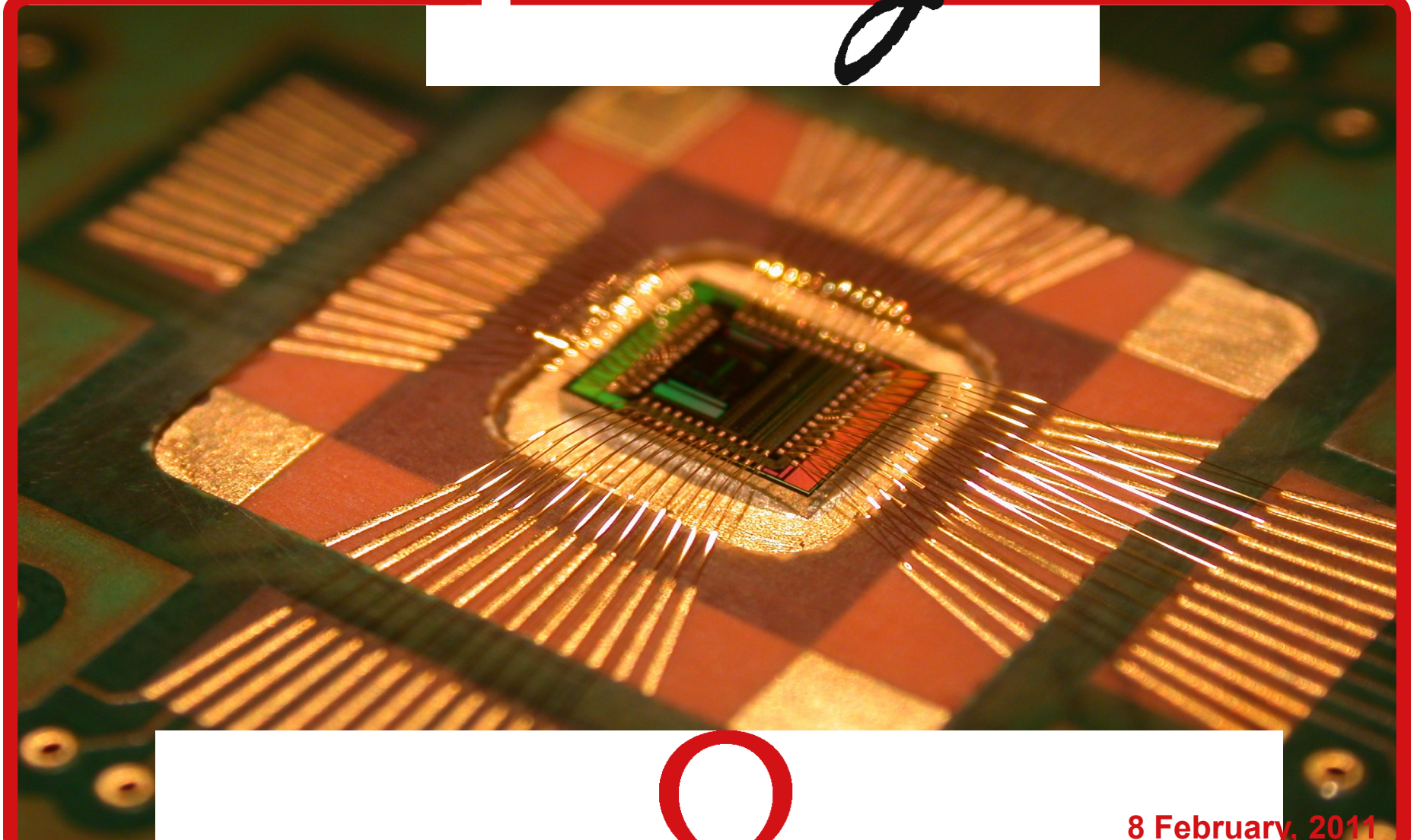

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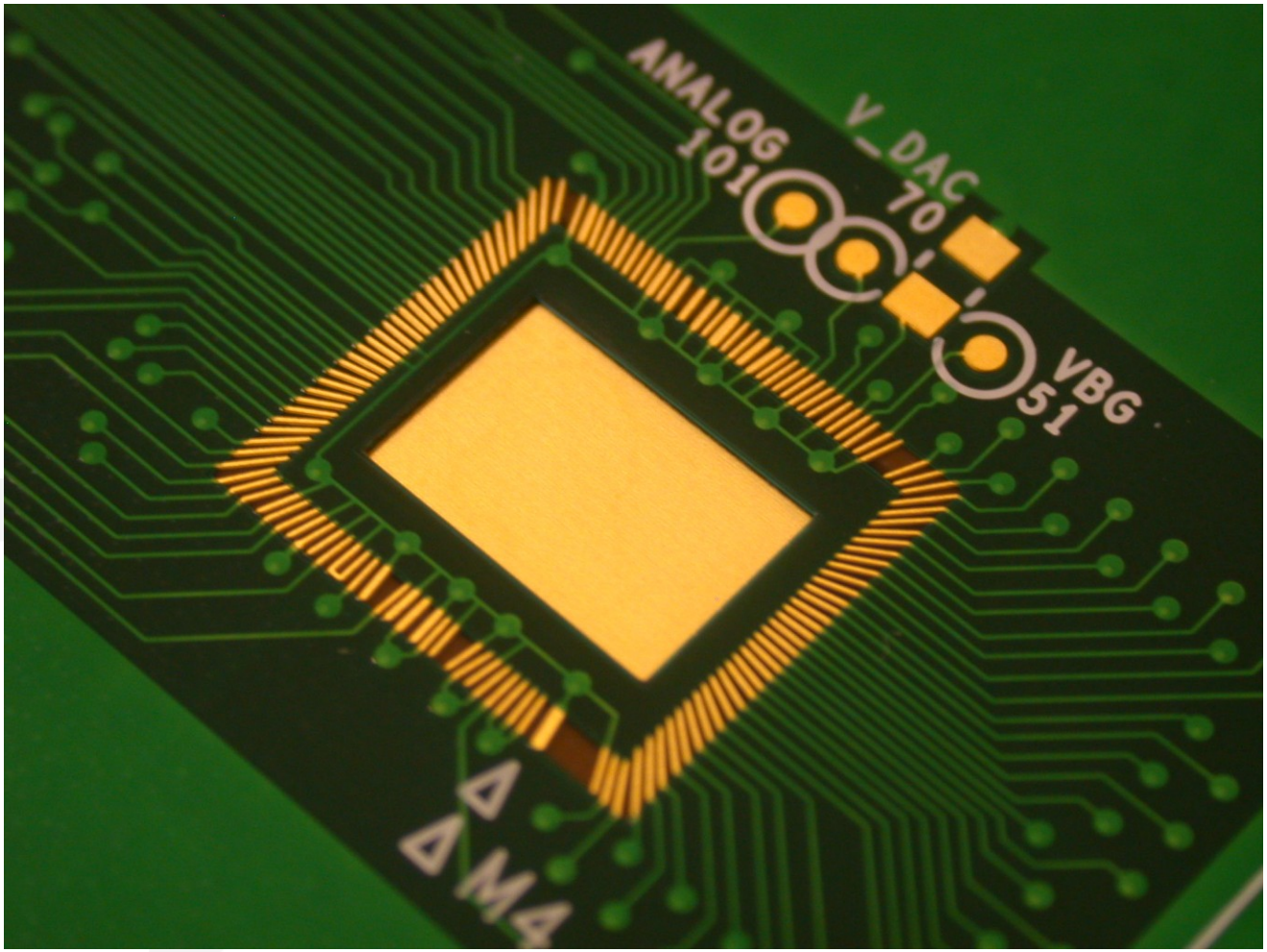
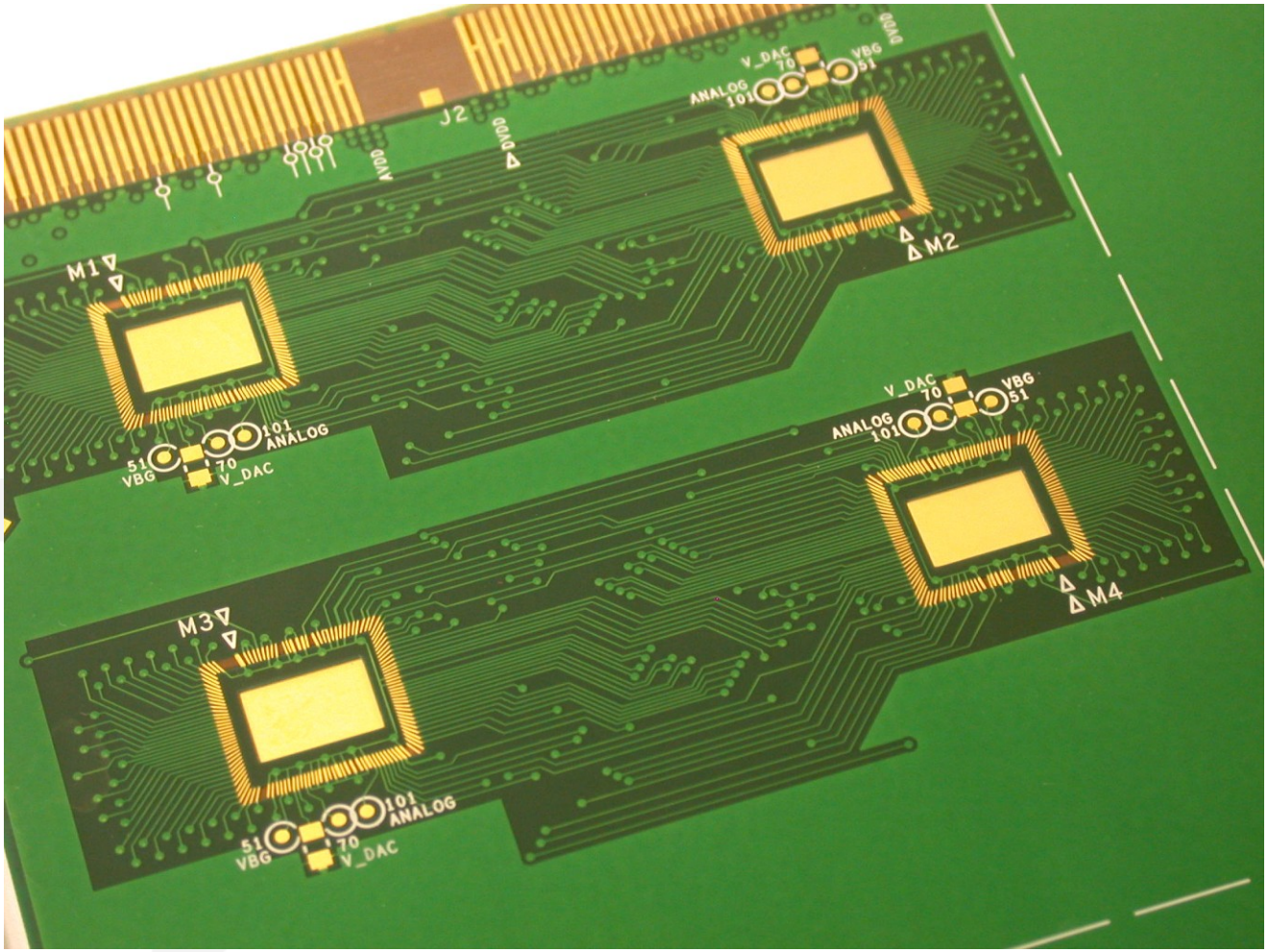
FEV7-COB



FEV7-COB



FEV7-COB2