R&D activity @ pole MicRhAu dedicated to High Granularity Si-W Ecal

The CALORIC chip

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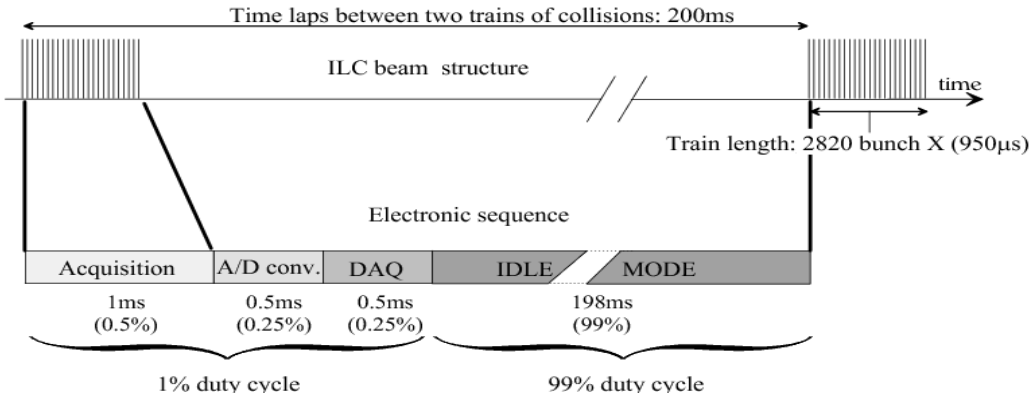
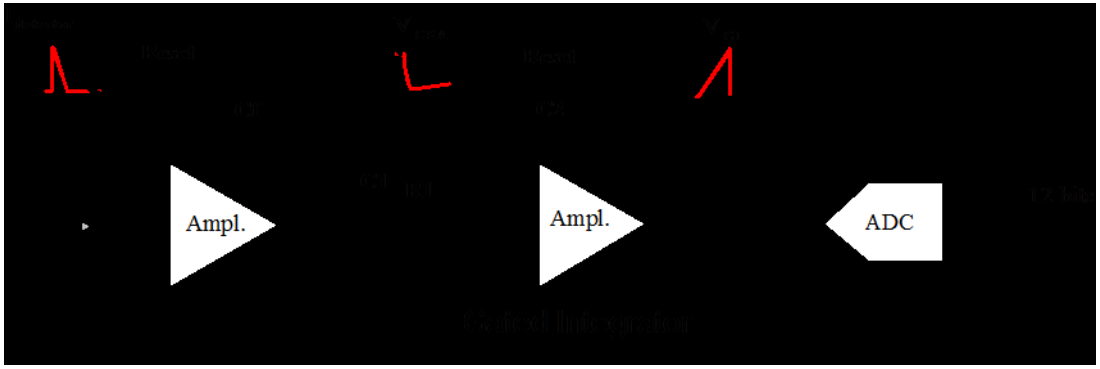
Readout Electronics for High Granularity Ecal

- **Electrical specifications of the readout electronics:**
  - Dynamic range of the signal delivered by a Si-diode : from MIP (4 fC) to 2500 MIPs (10 pC)
  - Level of noise limited to 1/10 MIP ➔ SNR ≥ 10
  - Error of Linearity:
    - < 0.1 % up to 10 % of the dynamic range (1 pC)
    - < 1% from 10 % and 100 % of the dynamic range
  - Power budget limited to 25µW per channel



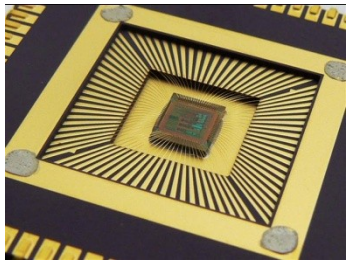
- **Axes of developments @ MicRhAu:**
  - Synchronous (with beam) analog signal processing: shaping with Gated Integrators, latched comparators
  - Fully differential architecture, except for the Charge Sensitive Amplifier (CSA)
  - One low-power ADC attached to each channel
  - Use of a pure CMOS technology, no bipolar transistors

First prototype channel

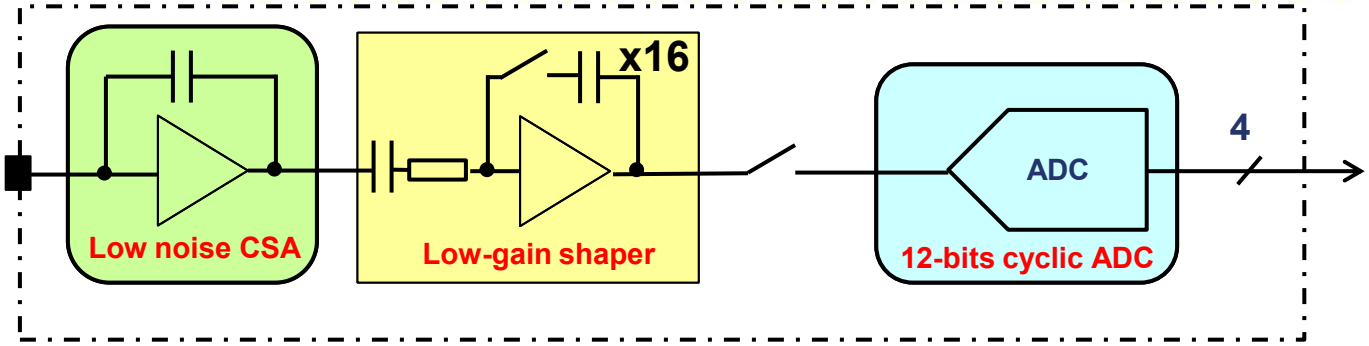


Status report presented at Desy in July 2010

- A VFE channel performing the amplification, the filtering, the memorization and the digitalization of the charge from Si detector has been designed and tested.
  - **Global Linearity better than 0.1 % (10 bits) up to 9.5 pC (2375 MIP).**
  - **ENC = 1.8 fC (0.5 MIP)** with a single gain stage
  - **Power consumption with power pulsing estimated** to 25µW (no digital part).



The **CALO**rimetry **R**eadout **I**ntegrated **C**ircuit



- New chip designed and now ready to be sent to foundry (CMP run of 14th February)
- Technology AMS CMOS 0.35 µm
- Architecture of CALORIC based on the previous channel tested, with some improvements:

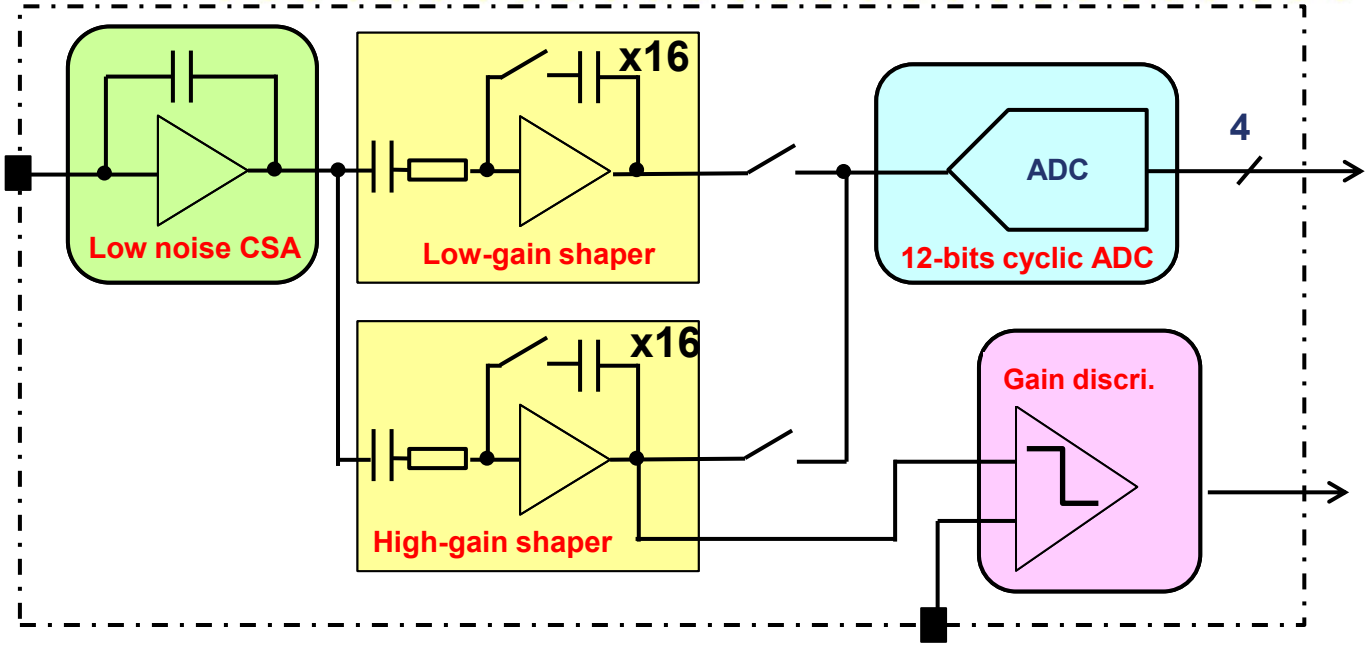
→ Reduction of the power consumption of the CSA

→ Reduction of the noise of the amplifier of the Gated Integrator

→ Increase of the analog memory depth to 16

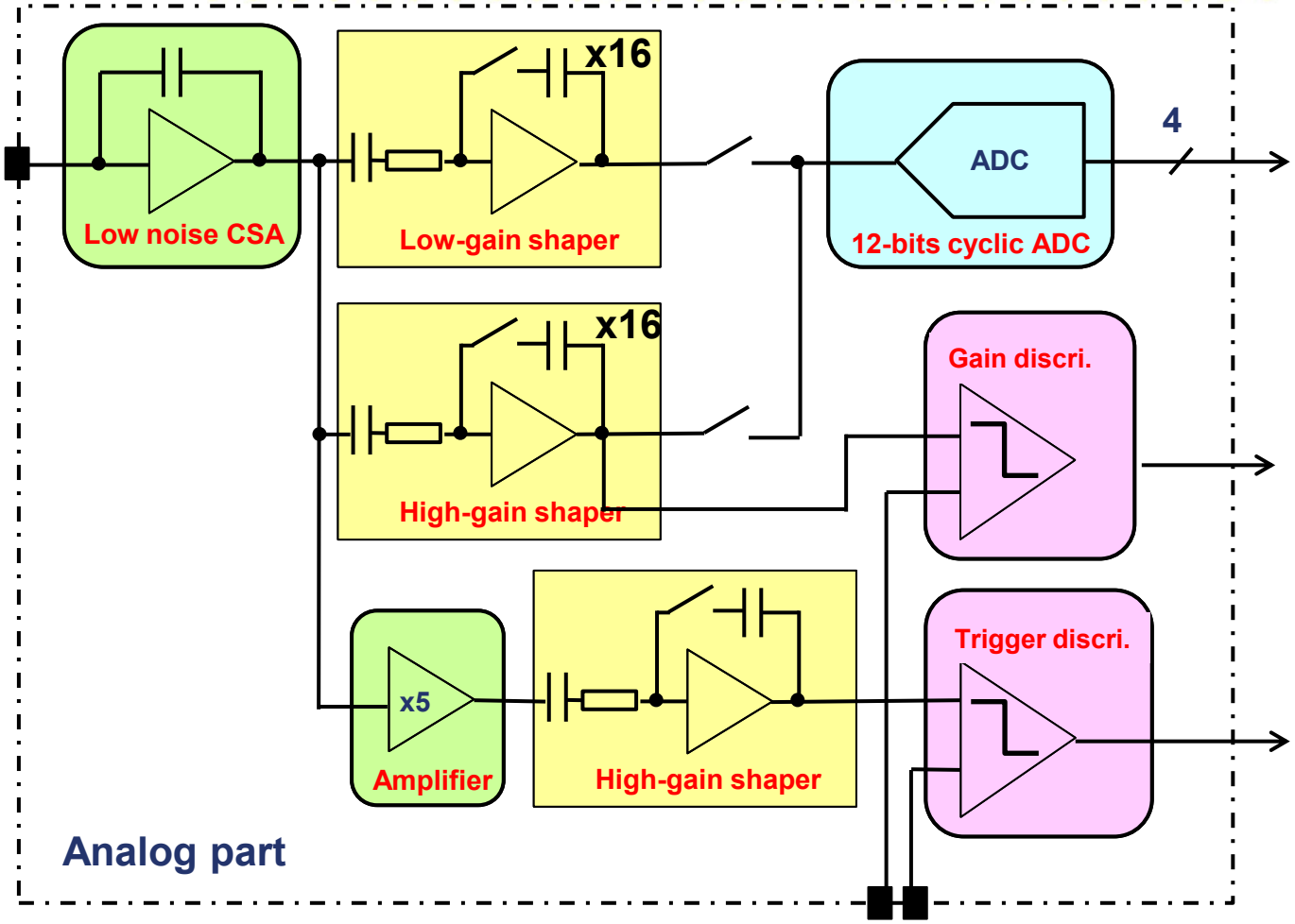
→ Fully power pulsed

The CALOrimetry Readout Integragted Circuit



- A High-Gain (about x 20) channel added to reach the MIP-to-noise ratio of 10.
- A discriminator indicates the dynamic range of the signal → select the signal to be converted

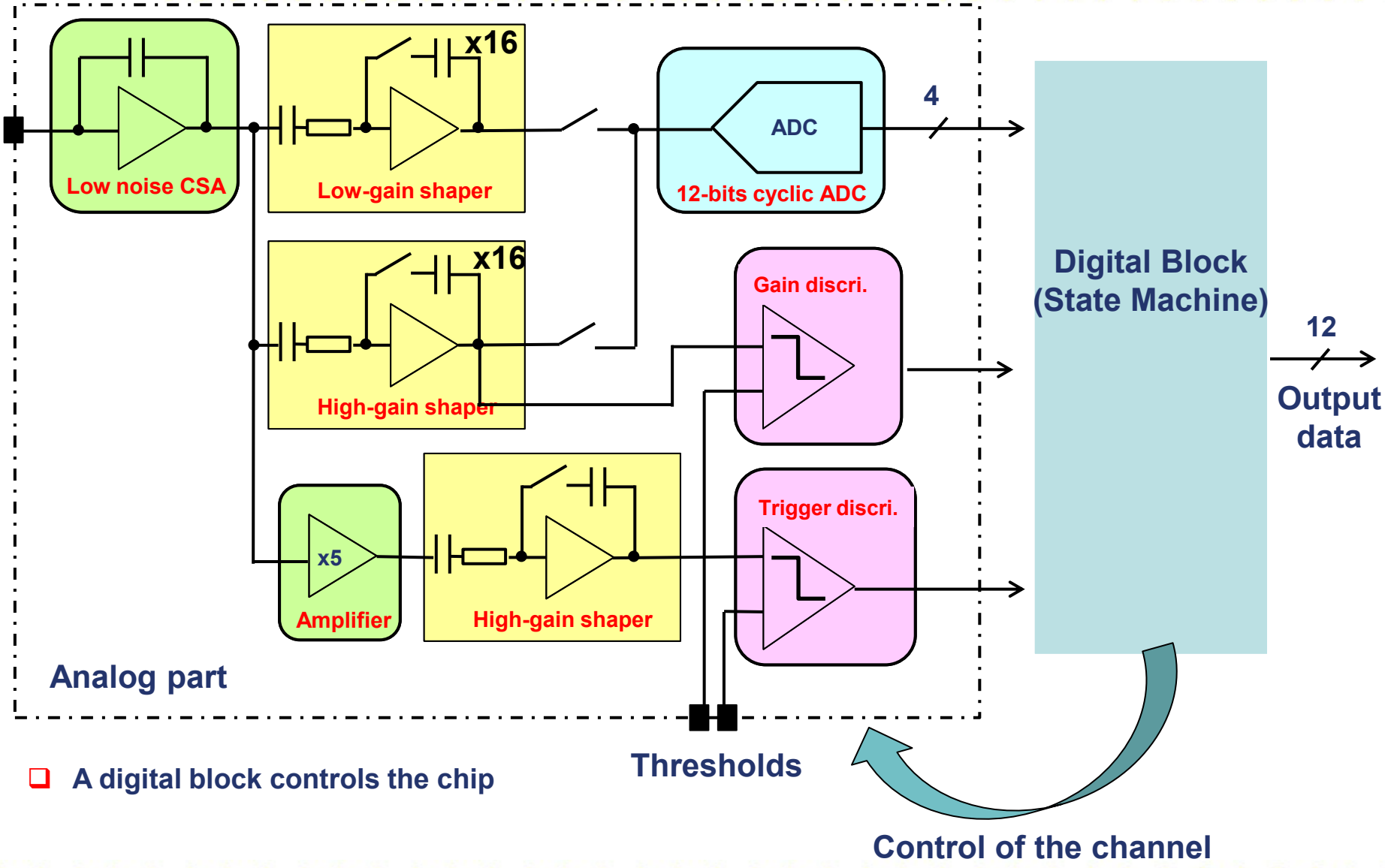
The CALOrimetry Readout Integragted Circuit



- A Trigger channel added to select events over the MIP

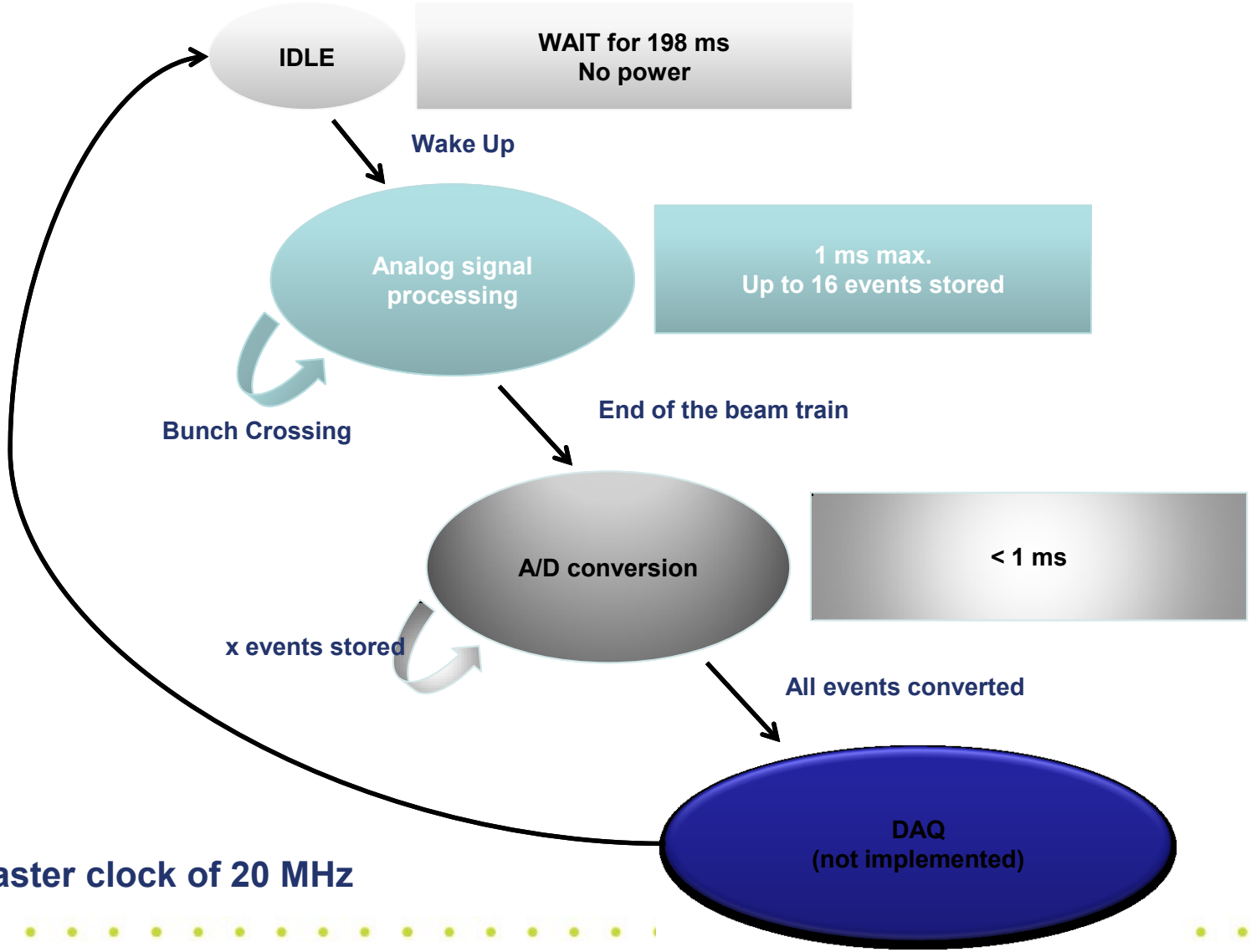
→ The trigger signal determinates if the active memory cell is reset or the signal kept into memory

The CALOrimeter Readout Integrated Circuit



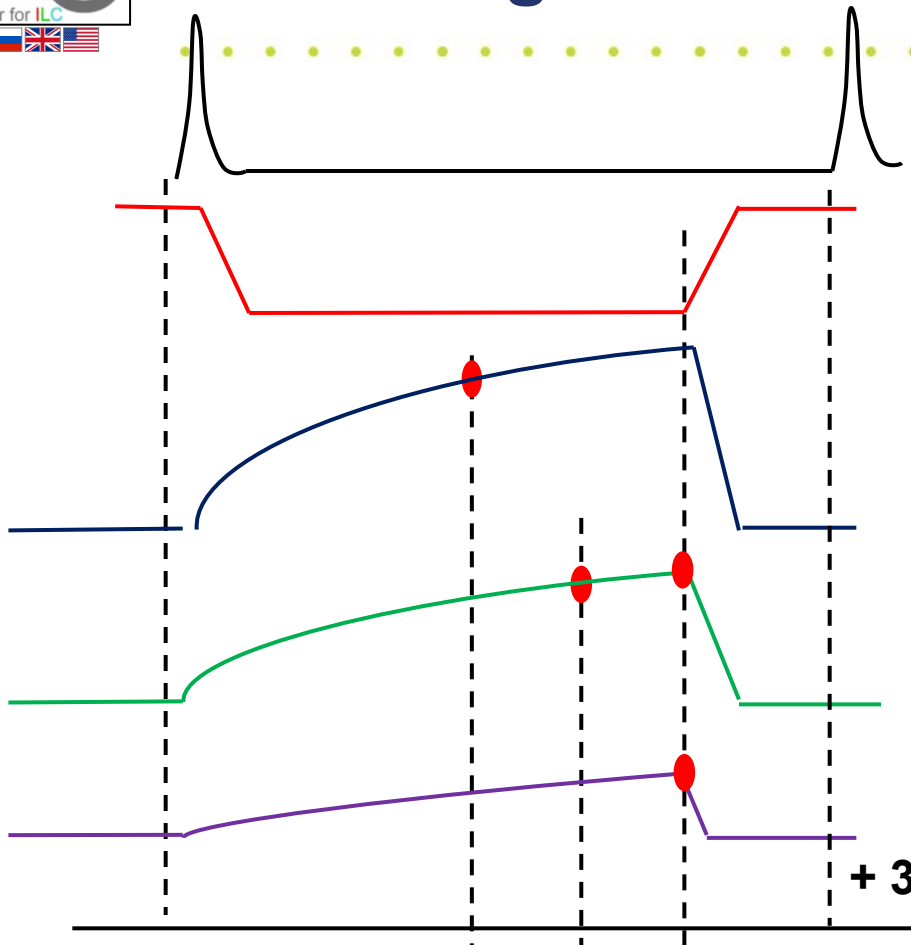
- A digital block controls the chip

Global State Machine



Master clock of 20 MHz

Timing of the analog processing



Signal delivered by the Si-diode

Output signal of the CSA

Output signal of the trigger channel

Output signal of high-gain channel

Output signal of the low-gain channel

+ 350 ns: ready to process next event

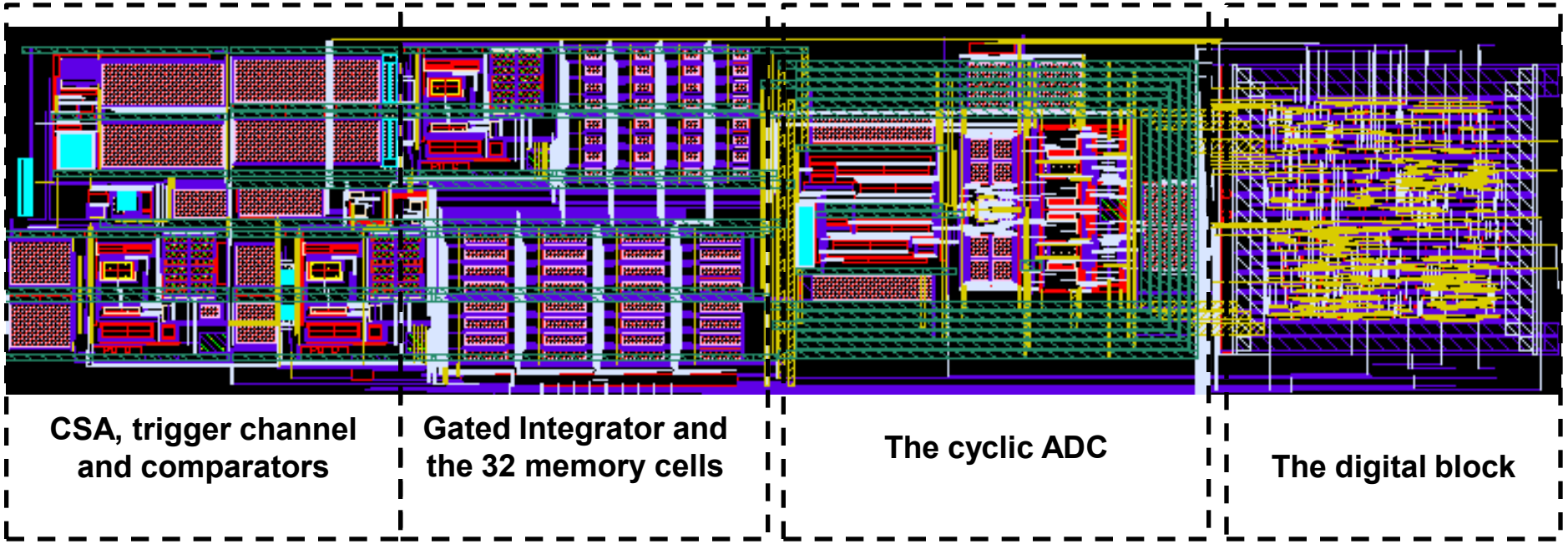
t = 0 ns: event synchronous w/ beam

+ 200 ns: decision of the trigger comparator

+ 250 ns: decision of gain comparator

+ 300 ns: end of integration: reset or memorization

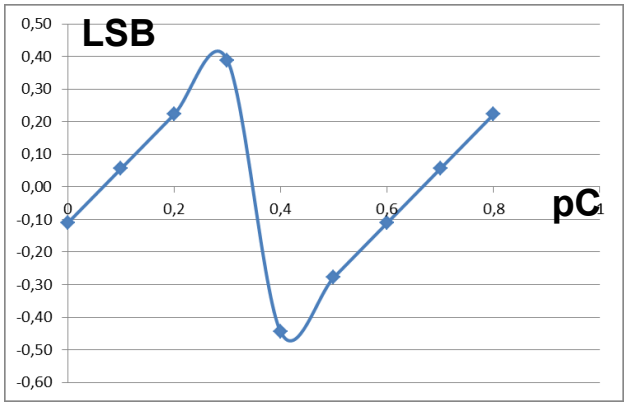
Layout of CALORIC



CSA, trigger channel and comparators	Gated Integrator and the 32 memory cells	The cyclic ADC	The digital block

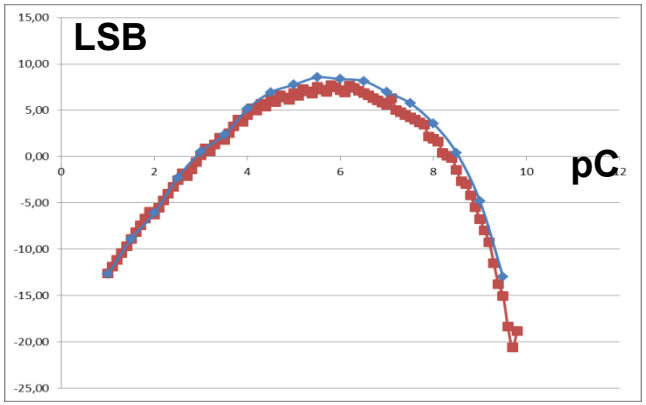
Simulated performance

Gain-20 channel



INL < 0.1%

Gain-2 channel



INL < 1%

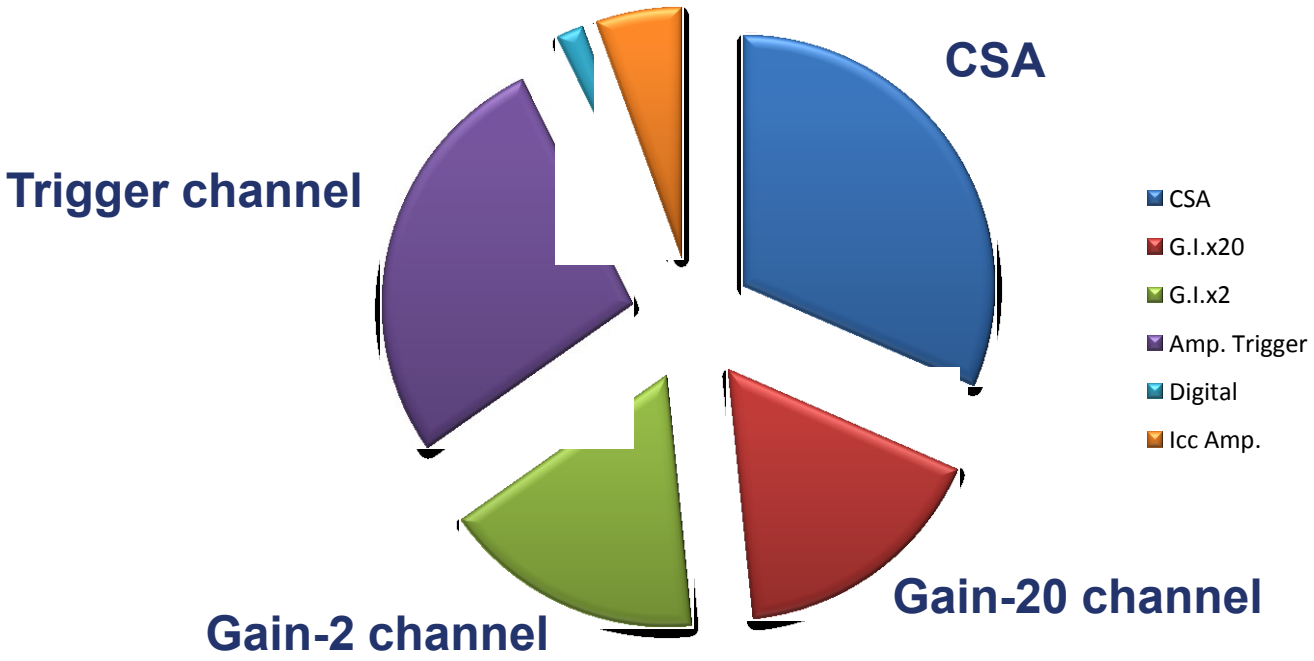
- ENC (rms value) = 0.4 fC = 2400 e^- = MIP/10

with the High-Gain channel and $C_{detector}$ = 30 pF

Power consumption

- **Evaluation using power pulsing with the ILC duty cycle:**

➔ **45 µW per channel**



Conclusion and perspectives

- The CALORIC chip is ready for fabrication.
- Simulated performance is in agreement with the requirements of Calice, except power consumption.
- The first measured performance is expected before summer.
- A multi-channel chip should be submitted for fabrication before the end of 2011

  → compatible with Calice DAQ

  → compatible with pinout of FEV board for test