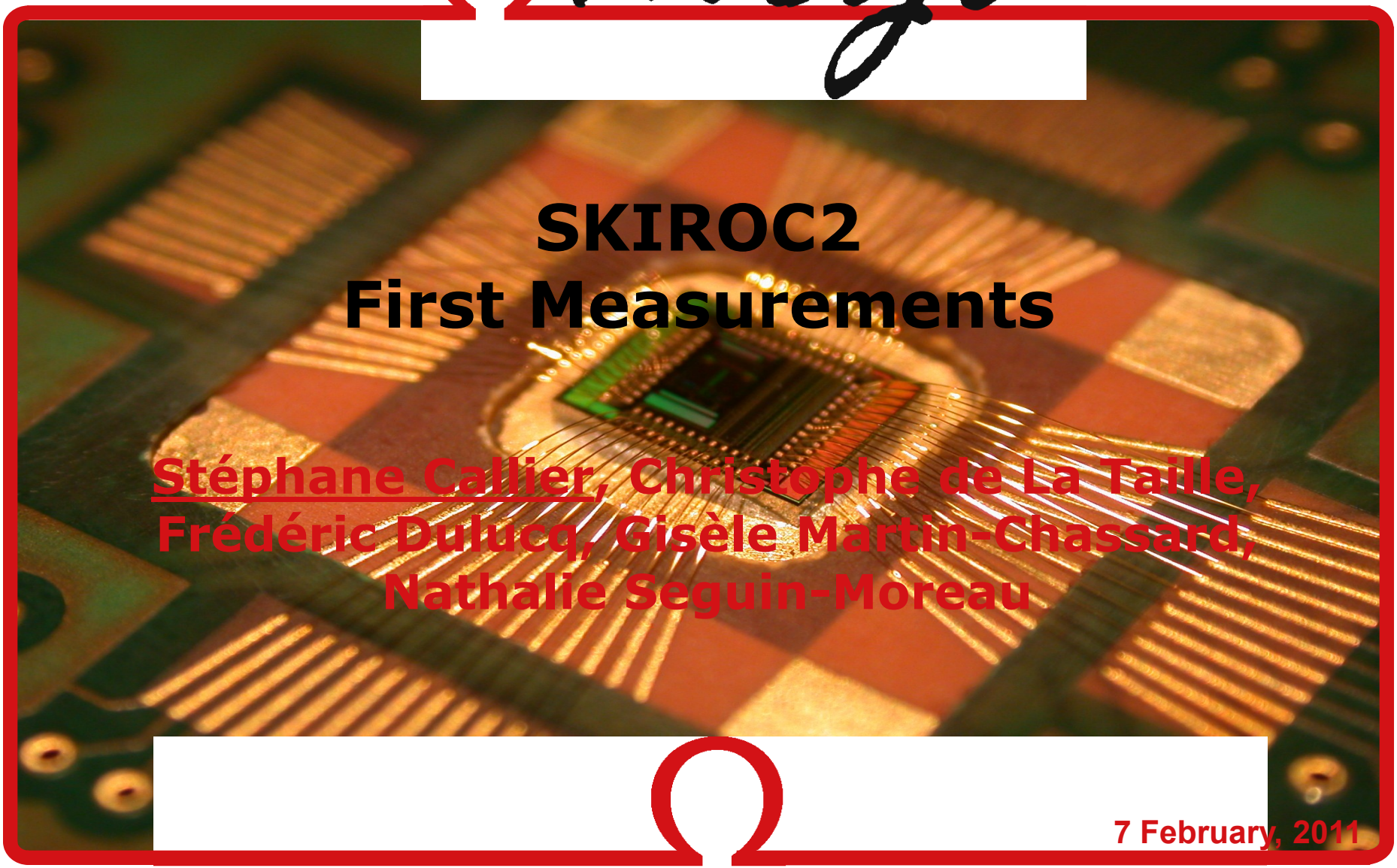
IN2P3 CSNSM LAL LPC IPN

Omega



SKIROC2
First Measurements

Stéphane Callier, Christophe de La Taille,
Frédéric Dulucq, Gisèle Martin-Chassard,
Nathalie Seguin-Moreau

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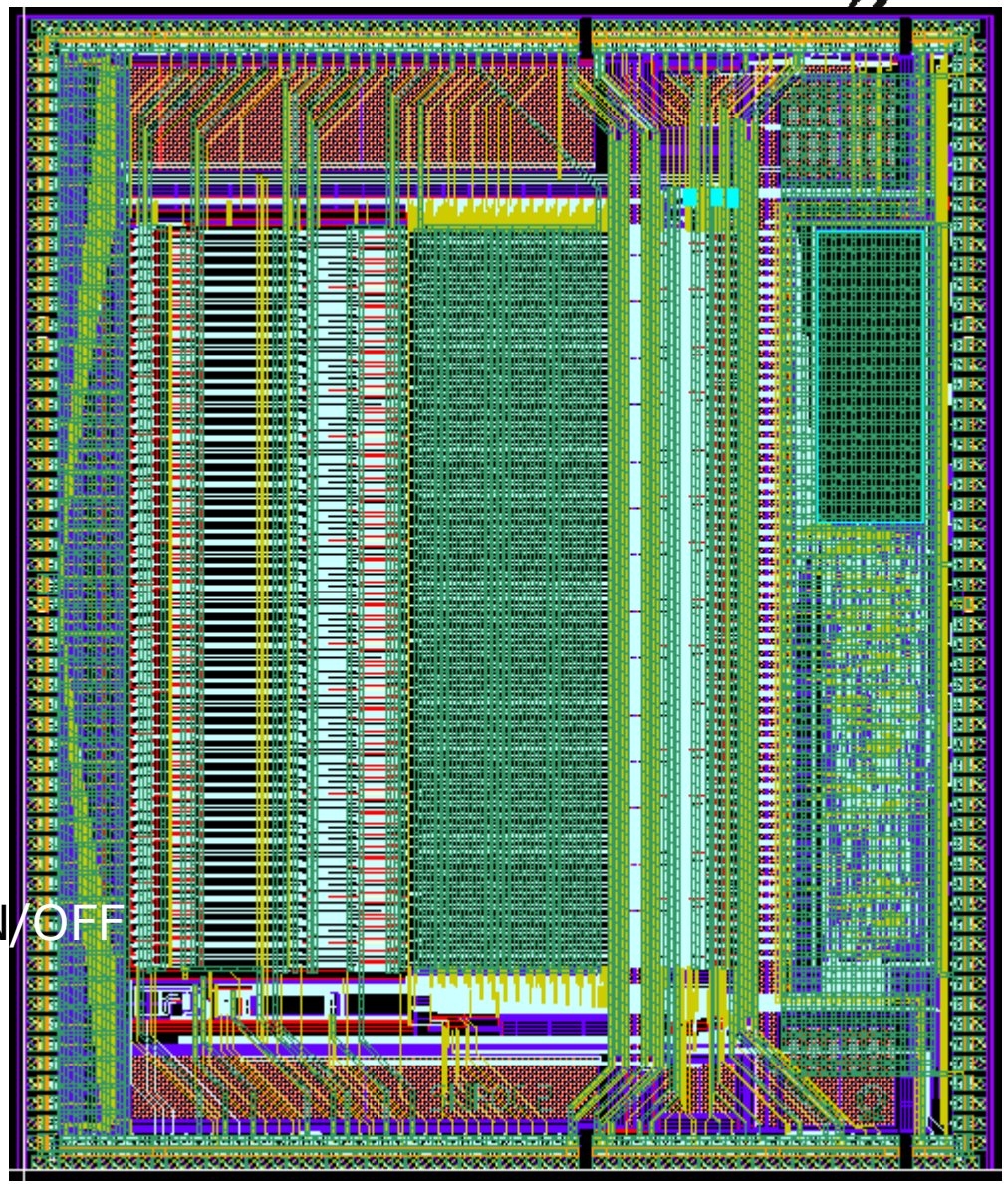
Orsay MicroElectronics Group Associated

SKIROC2 overview

- 64 Channels
- Vss split :
  - Inputs
  - Analogue part
  - Mixed part
  - Digital part
- 250 pads
  - 3 NC
  - 17 for test purpose only
- Enhanced Power control
  - Full power pulsing capability
  - Each stage can be forced ON/OFF
- Die size
  - 7229 µm x 8650 µm



SKIROC2 analogue features

- Bandgap (reference voltage from HardRoc2b)
- Dynamic Range : from ½ MIP up to 2500 MIP
  - With C*detector* = 20pF
- Analogue channel muting capability (PA can be shut down)
  - Common 4-bit adjustable gain
  - PIN diode leakage current swallow capability (up to 10nA)
- 180ns shaping time Slow Shapers for charge measurement
  - Optimized S/N
  - Antisaturation system in Gain 10 Slow Shaper
- Analogue signal-to-noise ratio : 17 (1500 e^- noise for 1 MIP)
- 2-bit shaping time adjustable Fast Shaper (50 to 100ns)
  - Antisaturation system in Fast Shaper
- Analogue Memory depth : up to 15 events can be stored

SKIROC 2 mixed features

- 10-bit DAC for discriminator threshold
  - With improved 4-bit adjustment on each channel
- Trigger Discriminator from Parisroc
  - Better performance
  - Mask on each channel
- External Triggers now follow same path as internal ones
- 8-bit adjustable delay for peaking maximum signal
- (10 or 12-bit) ADC Discriminator from Parisroc
- Digitization of either time and charge or of both charges

SKIROC 2 digital features

- Common features with hardroc & spiroc :
  - Multiplexed Slow Control & Probe
  - Redundancy on Data Out & Transmit On signal lines
  - 2 switchable StartReadOut Inputs & EndReadOut Outputs :
    - to prevent chip failure
- Improved Slow Control/Probe
- New Digital Part :
  - new layout (easier interconnections with analogue part)
  - minor modifications concerning some timings (allowing more latency to analogue signal during conversion)

SKIROC 2 extra features

- 1 ns TDC capability
- TDC facility to operate in ILC mode or in test beam mode
  - 200ns for ILC / 5µs for test beam

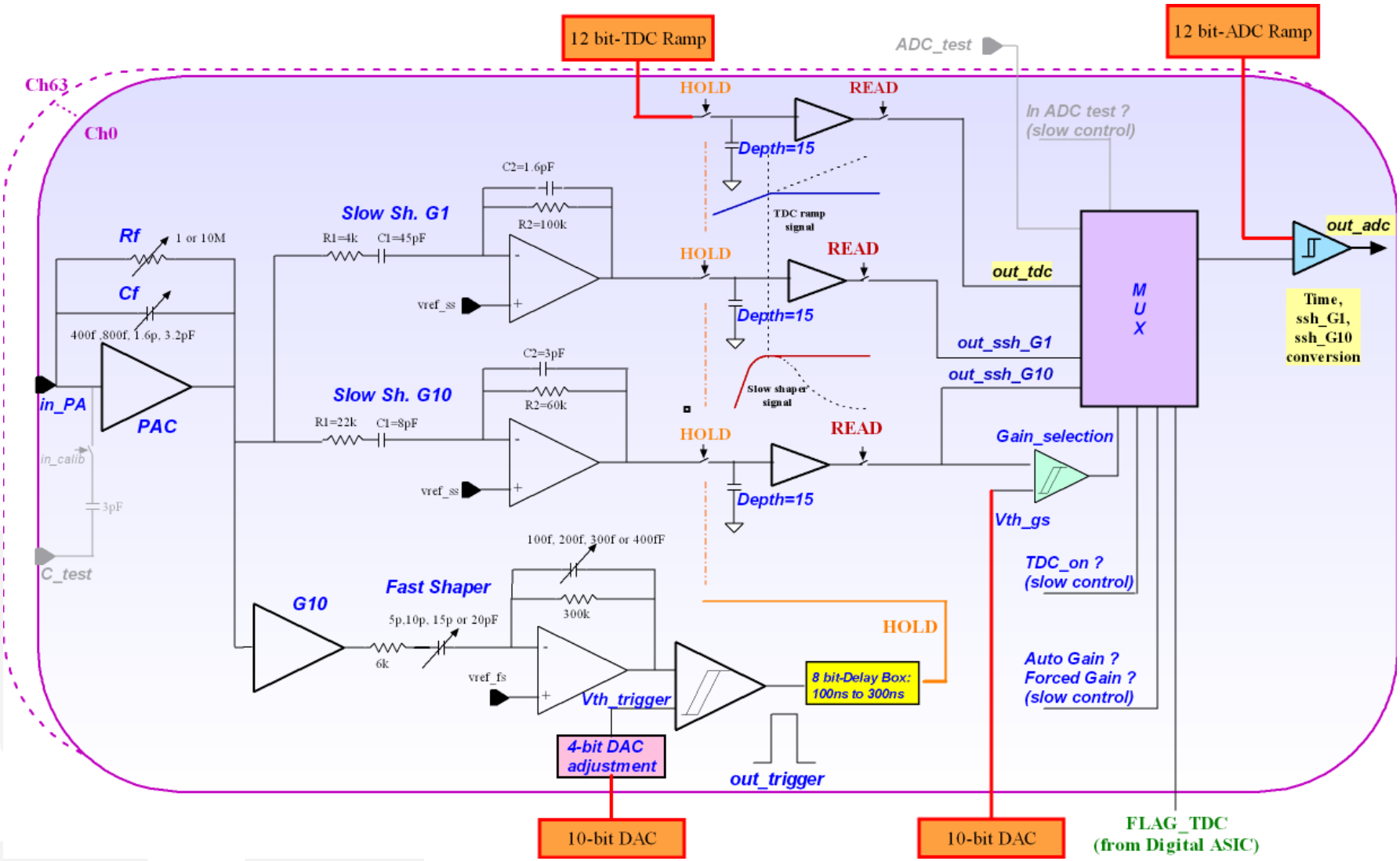
- Power consumption optimized
  - POD included for lvds receivers
  - Each stage can be totally disabled

- Analogue and Digital probe system

- Tri-state multiplexed Analogue output

- Test purpose : few pads required, single ended 40MHz needed, default slow control configuration, “only” Acquisition/Conversion/ReadOut Command necessary

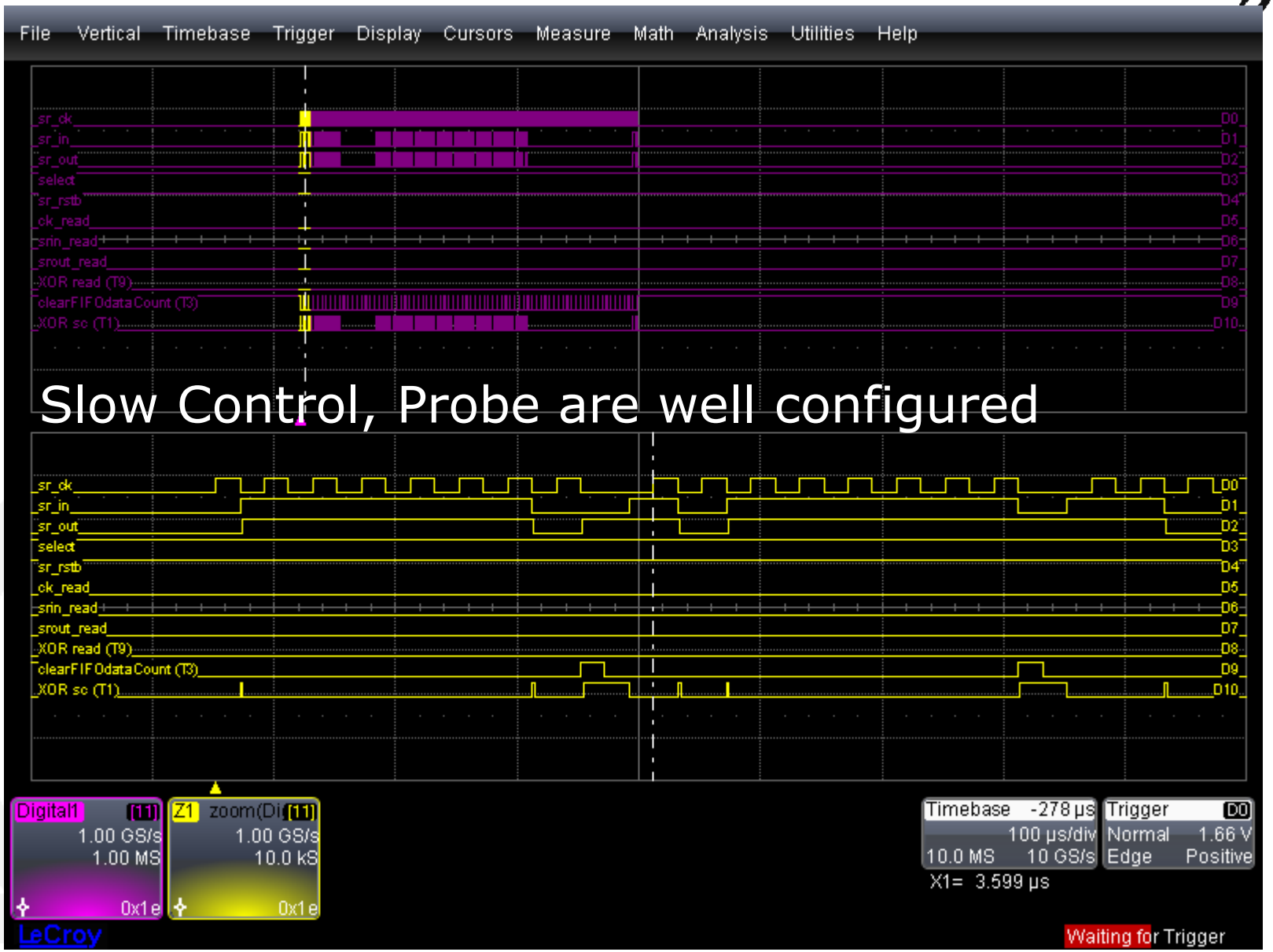
SKIROC2 Analogue core



SKIROC2 First Tests Setup

- Test Board manufactured and assembled in october 2010
- Firmware ready since november 2010
- Software still under development (LabView)
  - Main features already available (Slow Control, Probe, Read)
  - Digital ASIC control : step-by-step management
- Test performed on 2 different boards using 2 different chips

SKIROC2 Slow Control



SKIROC2 Analogue Simulations

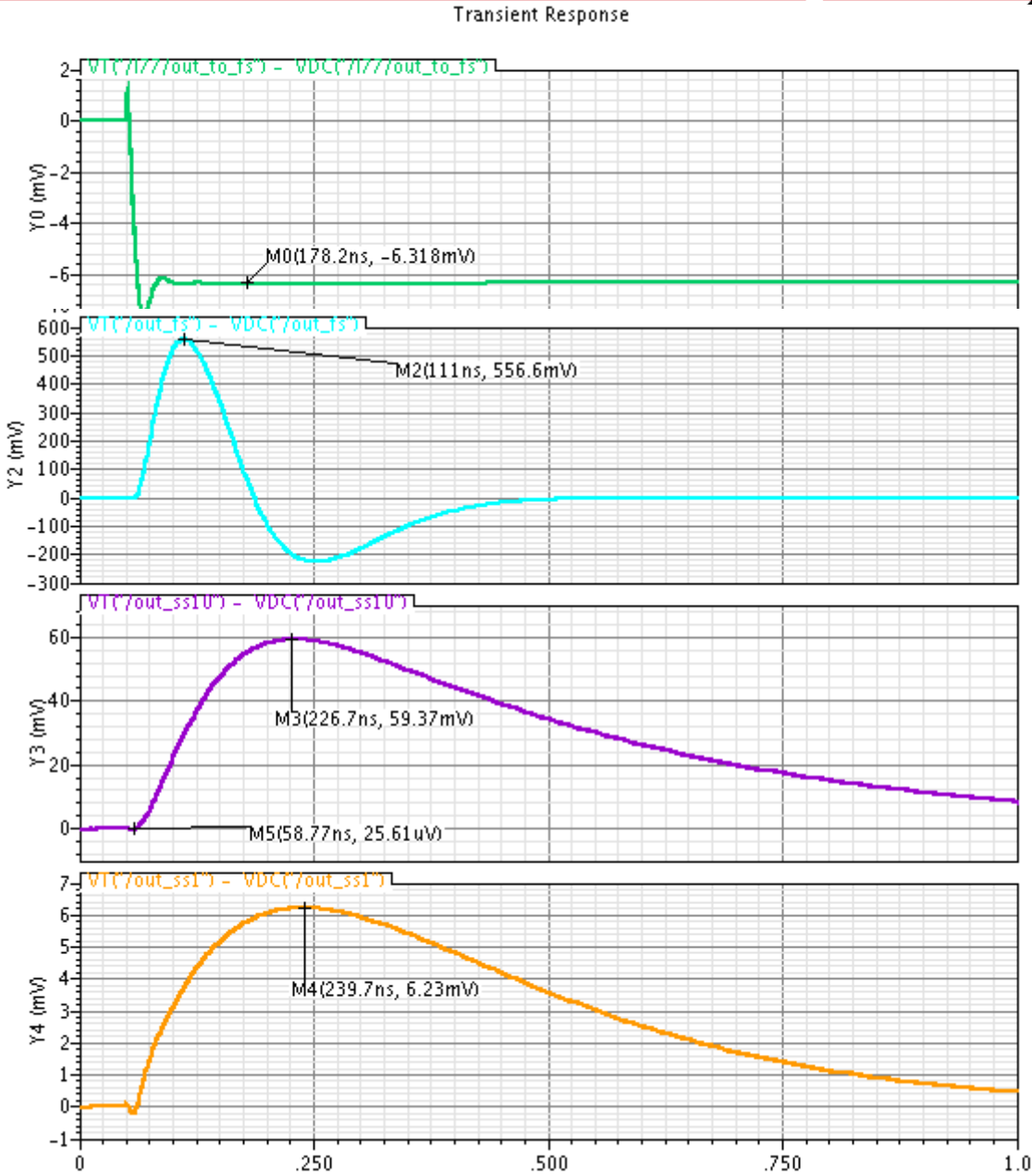
Q*inj* = 10 MIP

OUT_PA

OUT_FS

OUT_SS10

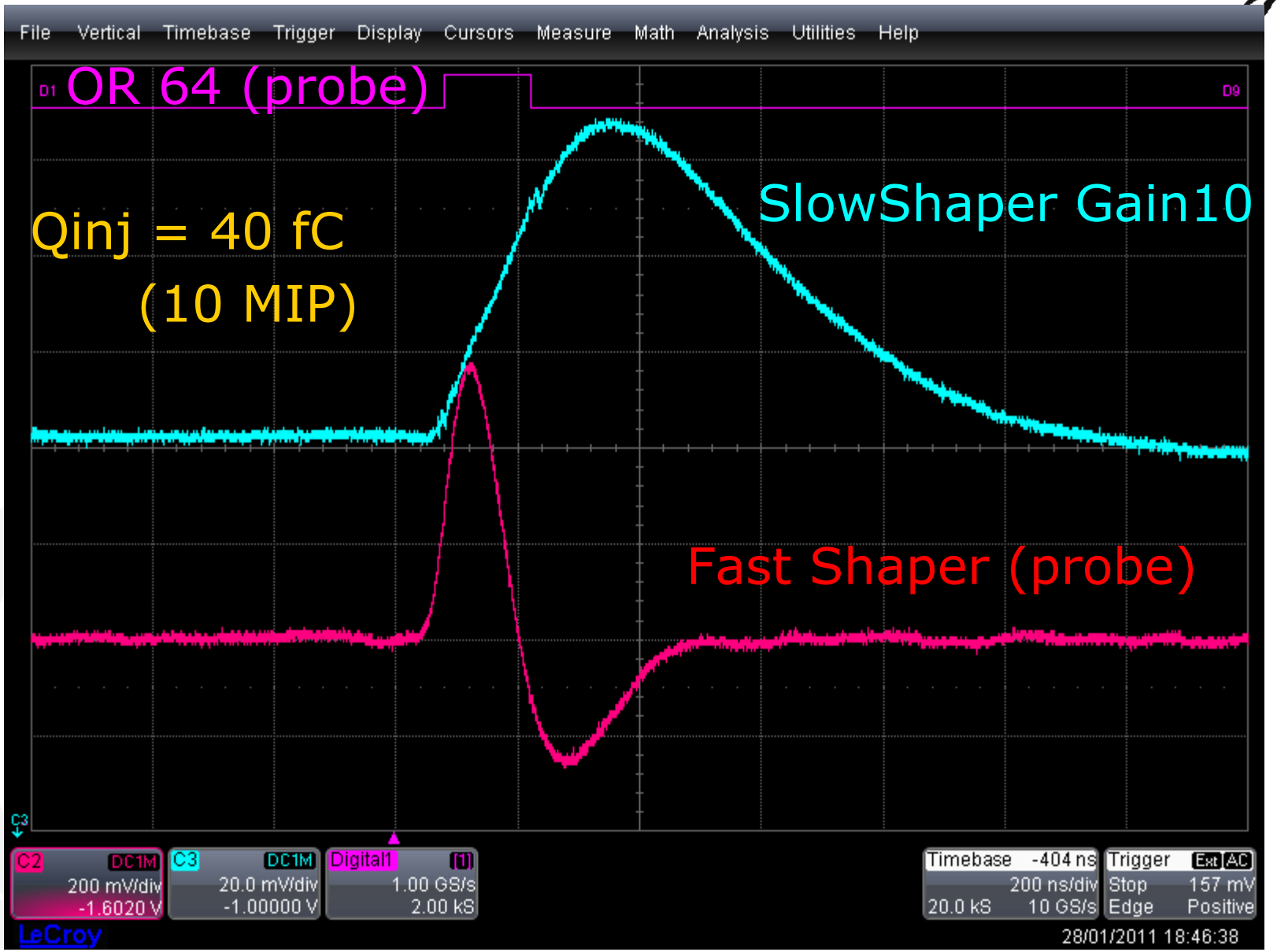
OUT_SS1



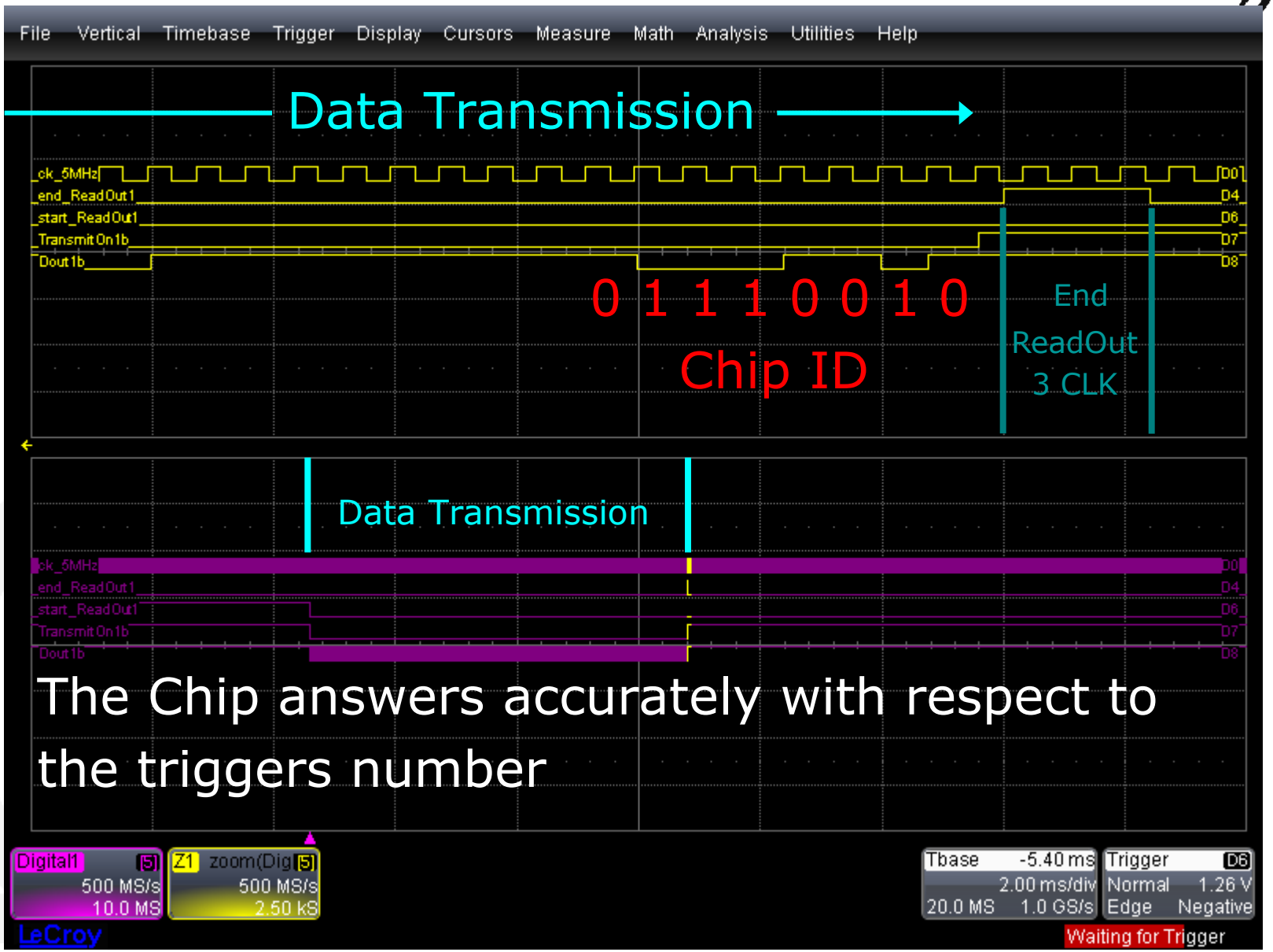
SKIROC2 Analogue Simulations

Q inj	Out_PA	Out_SS1	Out_SS10
1 MIP	639.6 µV	623.7µV	6.65 mV
10	6.32 mV	6.236mV	66.47 mV
100	63.2 mV	62.33 mV	664.1 mV
200	126.4mV	124.7 mV	1317 mV
500	315.9 mV	311.5 mV	Saturation to 1.5V
1000	631.6 mV	622.4 mV	
2000	1252 mV	1234 mV	
2500	1465 mV	1437 mV	

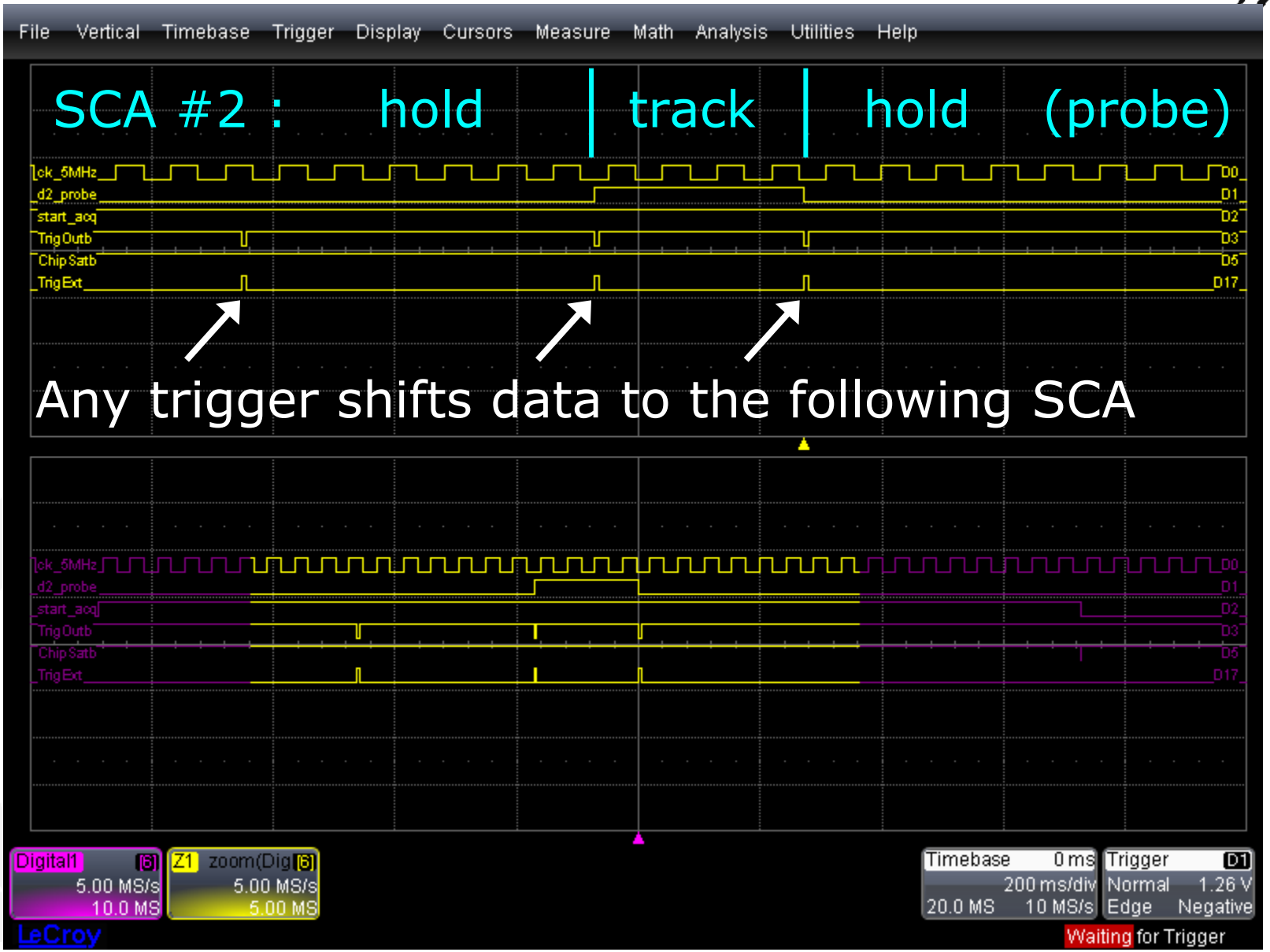
SKIROC2 Analogue Measurements



SKIROC2 Digital ReadOut



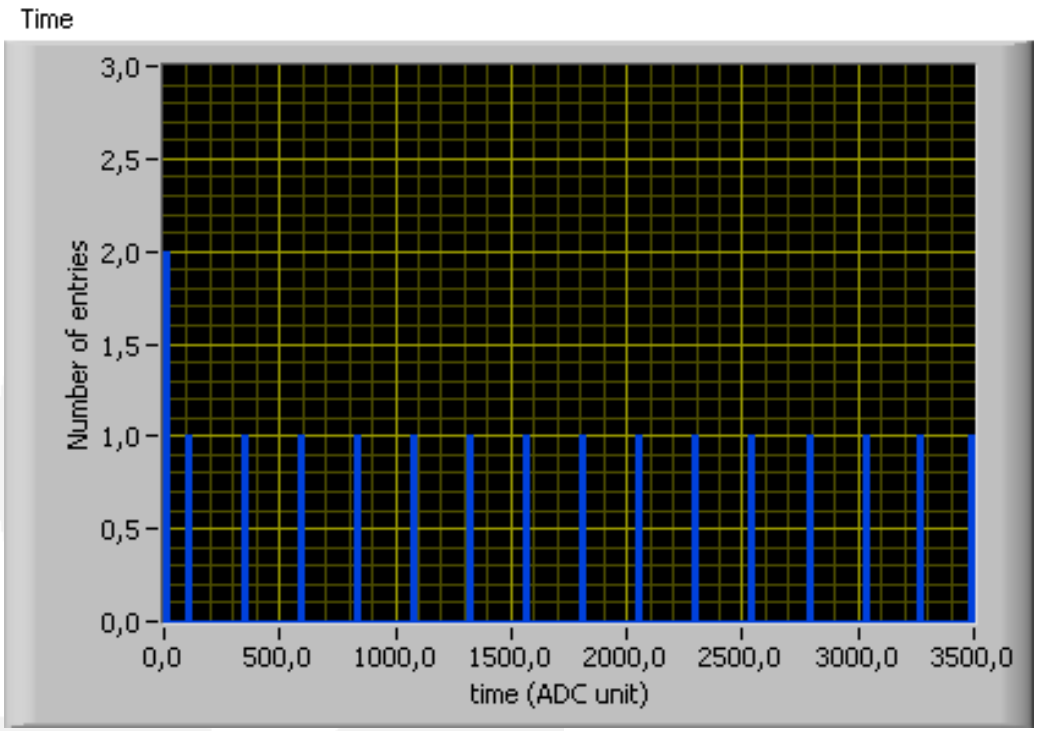
SKIROC2 Digital Features



SKIROC2 ADC Test

Using DC voltage as input and manual step-by-step acquisition system

(using only 1 sample !)

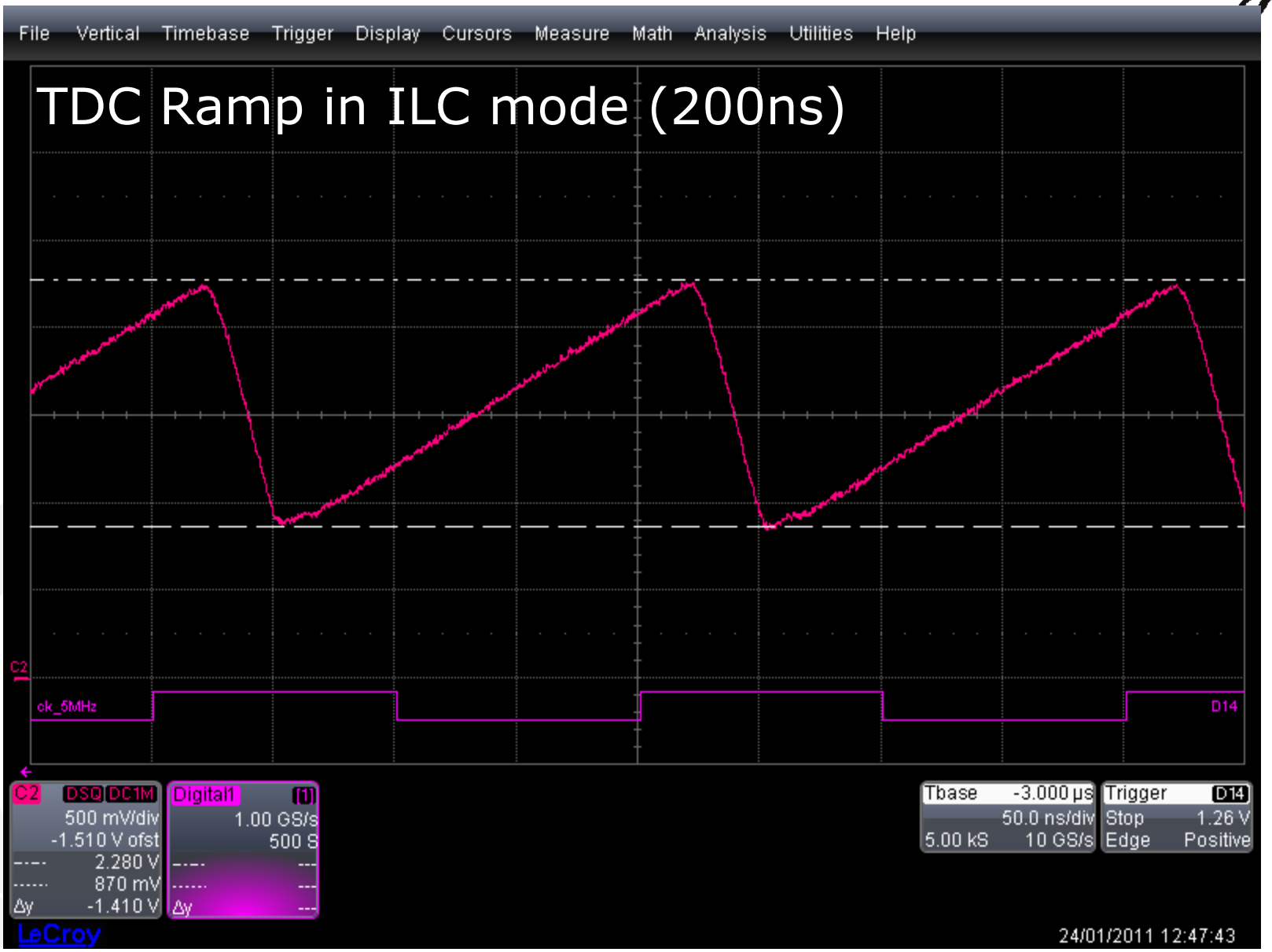


V DC	ADC count
0,6	5
0,7	5
0,8	99
0,9	342
1	586
1,1	829
1,2	1075
1,3	1316
1,4	1565
1,5	1810
1,6	2053
1,7	2298
1,8	2542
1,9	2786
2	3031
2,1	3268
2,2	3493
2,3	1

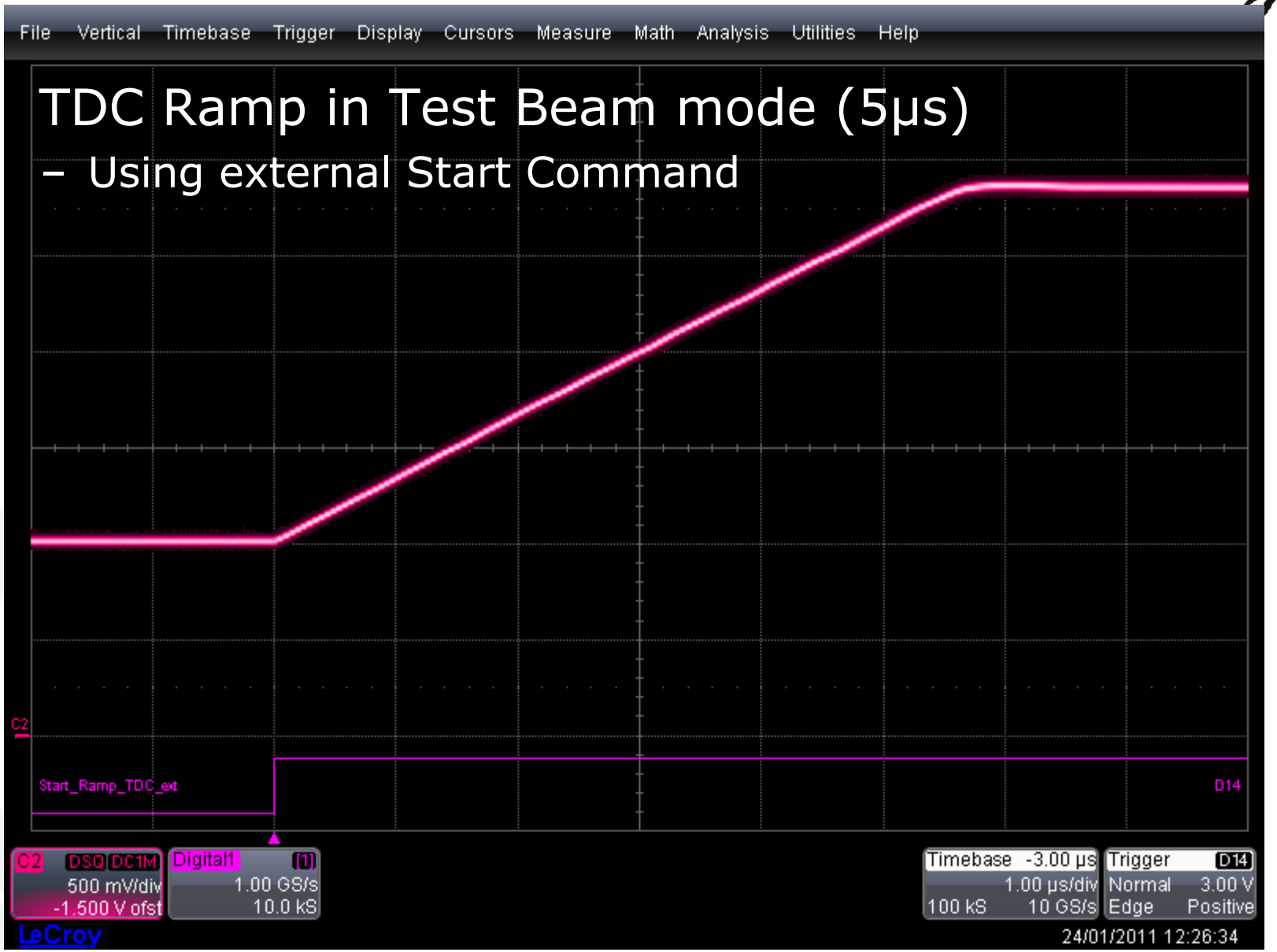
Underflow

Overflow

SKIROC2 TDC Ramp



SKIROC2 TDC Ramp



SKIROC2 Summary

- First measurements seems to be compliant with simulations

- Next steps (next tests) :
  - Analogue DC dispersion of PA, SS1, SS10 & FS
  - Analogue linearity of : DACs, PA, SS1, SS10, FS, ADC
  - S-curves (Trigger efficiency)
  - Digital data to analyze (using ADC)
    - Pedestal + Charge injected
    - TDC characterization
  - Bandgap, Power Pulsing, 4-bit DACs and others …

- 16 SKIROC2 chips will be integrated on next FEV8 boards to read out 1024 channels
  - Chip on Board require test using a Probe station