

MICROMEGAS Read-Out Chip

CALICE electronics meeting
LLR-Palaiseau, France
feb 9th, 2011

R. Gaglione and N. Seguin
for the MICROMEGAS DHCAL team

Laboratoire d'Annecy-le-Vieux de Physique des Particules,
Université de Savoie, CNRS/IN2P3
FRANCE

February 9th, 2011

Outline

Introduction

Tests at LAPP

Tests at LAL

Status

Outline

Introduction

Tests at LAPP

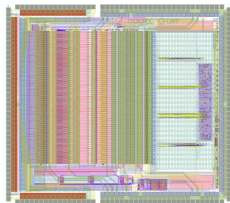
Tests at LAL

Status

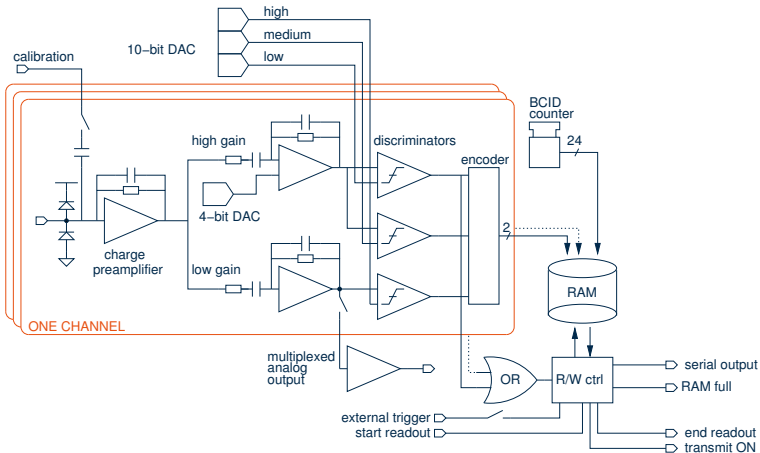
Introduction

MICROROC is a 64 channels integrated circuit packaged in TQFP160 intended to be used with MPGD-based DHCAL (MICROMEAS or GEM).

- MICROROC is a fruit of the collaboration between LAPP and LAL/OMEGA based on the experience of previous ASICs (DIRAC and HARDROC) and on multiple test beam results
- Same Digital part as HARDROC2b, but charge preamplifier input stage + sparks protection [R. Gaglione] and slower shaping + 4-bit DAC offset correction per channel [N. Seguin]
- MICROROC is pin a pin compatible with the HARDROC2b to minimize boards modifications (see Cyril's talk).



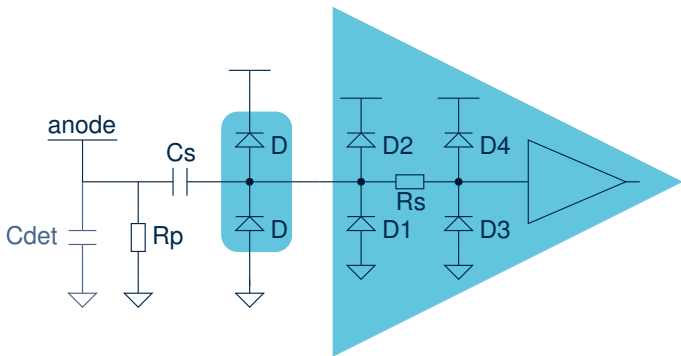
Global architecture



Performances

- Technology: AustriaMicroSystem SiGe 0.35 μm
- Die size: 4.85×4.3 mm
- Dynamic range: 500 fC
- C_{det} : 80 pF
- Preamplifier gain: 2.38 mV/fC
- Noise rms: 1 fC at preamplifier output, 0.24 fC with 200 ns shaping
- Peaking times: 30, 50, 100 and 200 ns
- Minimum threshold: ~ 2 fC

Protection against sparks



$R_p=1\text{ M}\Omega$, $R_s=10\ \Omega$, $C_s=470\text{ pF}$, D are ON-Semiconductor NUP 4114, D_x are integrated fast diodes.

Outline

Introduction

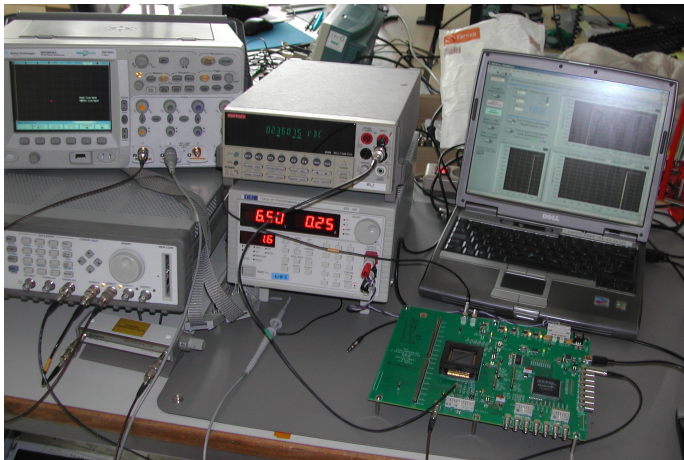
Tests at LAPP

Tests at LAL

Status

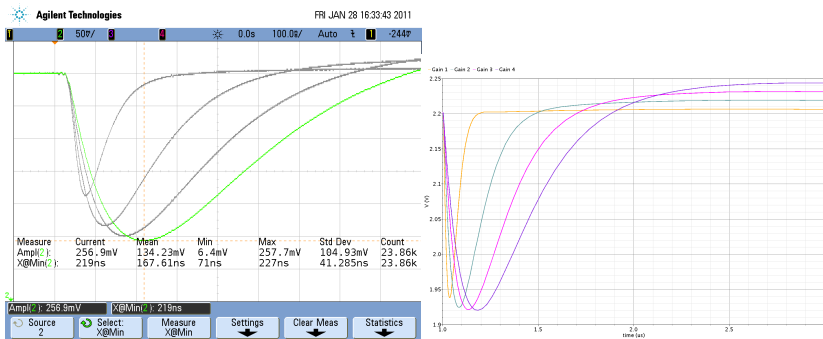
Test bench

The test board and labview software have been provided by OMEGA/LAL.



Waveforms

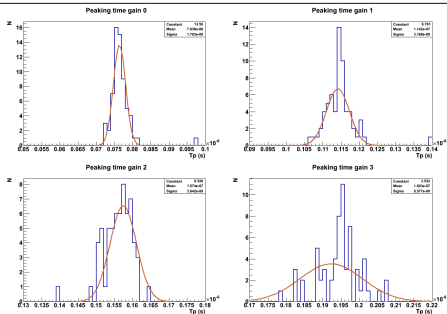
This is the output of high gain shaper, for the for settings (measure against simulation), with 25 fC charge injection (MIP-MPPV):



Good agreement between simulation and real behaviour.

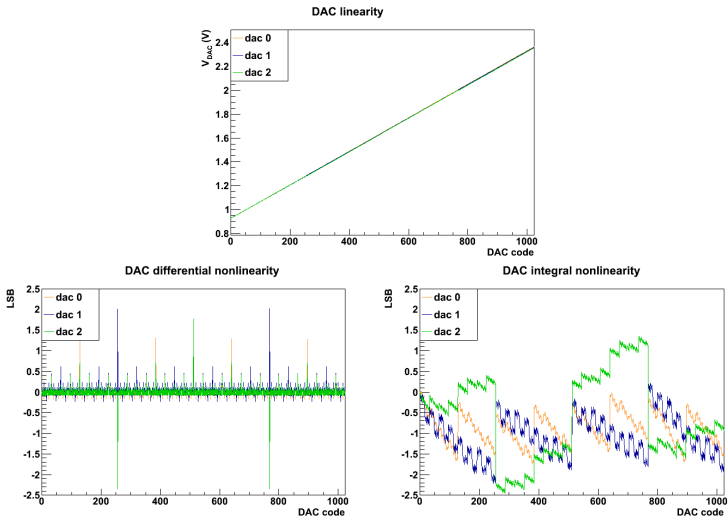
Shapers

Setting	Measure		Simulation	
	Gain (mV/fC)	Tp (ns)	Gain (mV/fC)	Tp (ns)
00	7.6	76.3	10.5	30
01	9.7	114.2	11.0	100
10	9.8	157.4	11.1	150
11	10.2	192.3	11.2	200



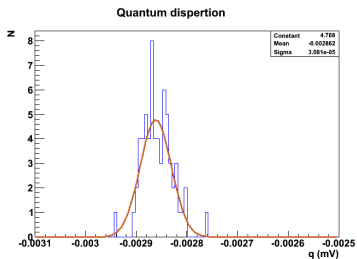
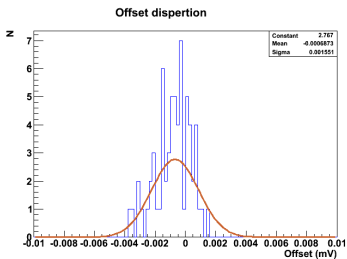
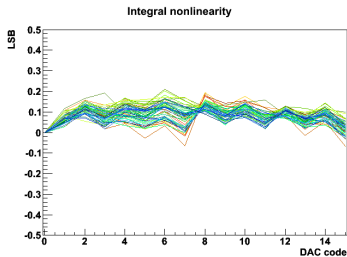
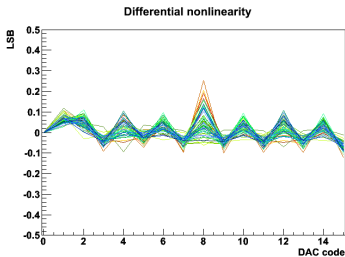
Good agreement between simulation and real behaviour.

Thresholds DAC



For each DAC, the linearity is about 3 DACU.

Offset correction DAC



The linearity is better than 1 DACU and $q=2.8$ mV.

Outline

Introduction

Tests at LAPP

Tests at LAL

Status

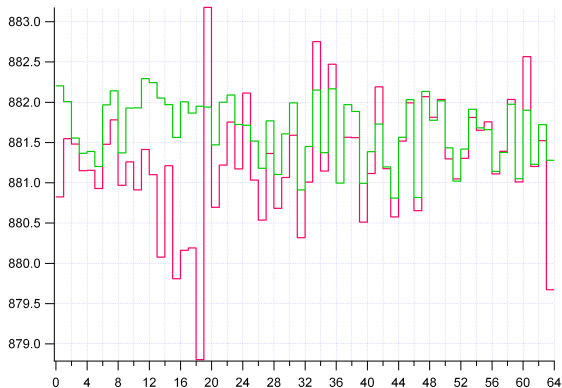
Pedestals compensation

$V_{avg} = 881.2$ DACU

$V_{sdev} = 0.74$ DACU

$V_{avg} = 881.6$ DACU

$V_{sdev} = 0.4$ DACU



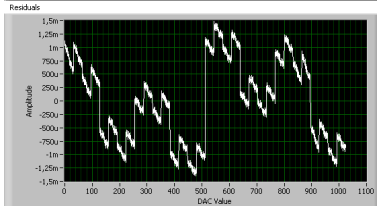
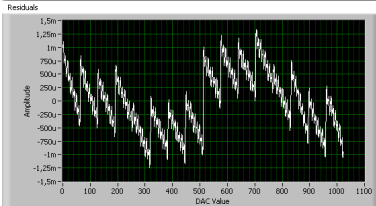
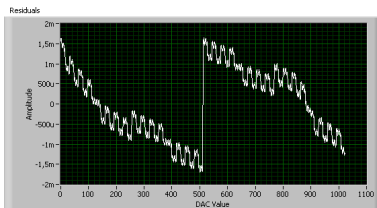
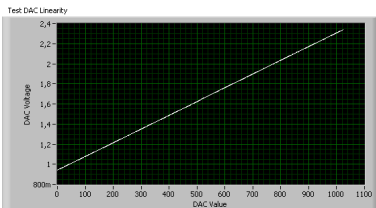
Difference before and after correction, for high gain shaper: **2 factor**
on pedestal dispersion !

Threshold DAC tests

dac0 slope:
1.37 mV/DACU
942.06 mV to 2.34 V

dac1 slope:
1.38 mV/DACU
943.32 mV to 2.35 V

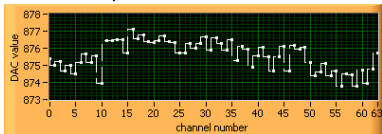
dac2 slope:
1.37 mV/DACU
943.35 mV to 2.34 V



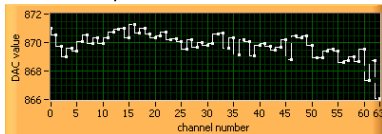
INL: ± 1.5 mV

Scurves measurements $C_{det}=88$ pF

50%estimation per channel

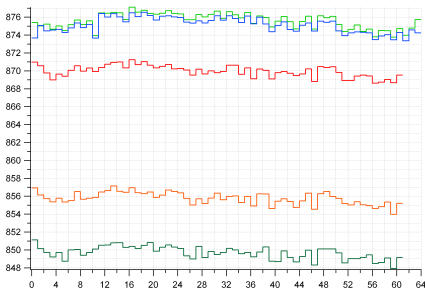


50%estimation per channel



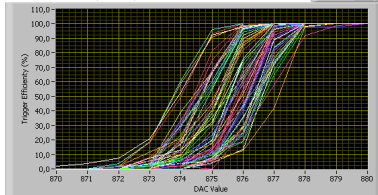
Pedestal: $V_{avg}= 875.6$; $V_{sdev}= 0.85$

2 fC: $V_{avg}= 869.9$; $V_{sdev}= 0.65$



pedestal, 1 fC, 2 fC, 4 fC, 5 fC

Test S-curve vs Threshold (Automated)



Outline

Introduction

Tests at LAPP

Tests at LAL

Status

Prototypes tests

The chip has been sent in MPW run in June 2010 and 5 prototypes have been received in September 2011. The behaviour of the prototypes is very satisfying.

Production

After prototypes tests in LAL and LAPP, an order has been placed for 350 chips. 341 chips have been received last week, and tests should be started very soon !

A production HR2b board has flashed with DIF firmware (see Guillaume's talk) and is used with LAPP Labview to test the 341 chips.