

Micromegas DHCAL SLAB with Hardroc2/Microroc

1. Result in 2010
2. Works for 2011



Micromegas DHCAL SLAB with Hardroc2/Microroc

1. Short Resume Result in 2010

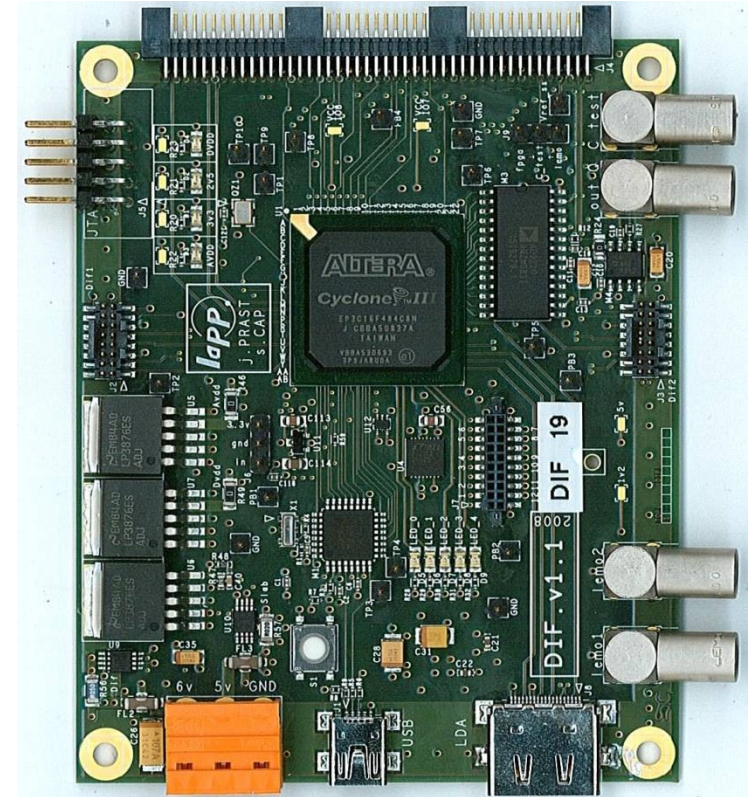
DIF product, M² Hardroc2 product

2. Works for 2011

DIF

DHCAL DIF production for the Cubic Meter

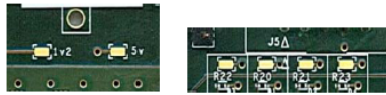
- 190 DIFs have been produced
- Boards have been tested at LAPP with a special Test bench (Boundary scan + functional tests).
- 185 out of 190 DIFs are fully operational
- DIF Boards have been sent to IPNL (137) and LLR (18)
- They are compatible with ECAL (SPIROC) AHCAL (SKYROC) and DHCAL (HARDROC and MICROROC) detectors



DIF

Test Bench and test procedure

1) Verifier les courts circuits entre les alims



→ 15 combinaisons à effectuer

2) Brancher le connecteur **ALIM** et alimenter la carte

Vérifier le courant !!

3) Verifier les valeurs des alimentations



4) Couper l'alimentation

5) Brancher les autres connecteurs :

- Dif-dif - JTAG
 - Lemo - mezzanine
 - HDMI
 - USB
- voir couleur*

6) Plugger la carte en tirant la poignée vers la droite.

7) Alimenter la carte de nouveau

8) Lancer le test



PASS

FAIL

T) Trouver la cause et recommencer au 8

14) Débrancher les connecteurs

13) DéPlugger la carte en tirant la poignée vers la gauche.

12) Couper l'alimentation

11) Tester la liaison USB avec le programme en LabView

10) Programmer le FPGA

9) Débrancher le **JTAG** et brancher celui de Quartus

PC



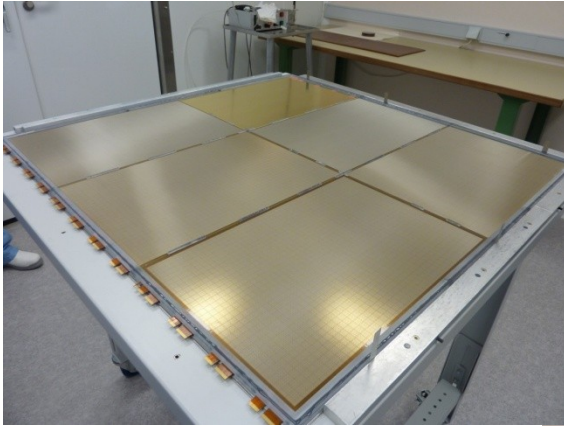
DIF

Test Bench and test procedure



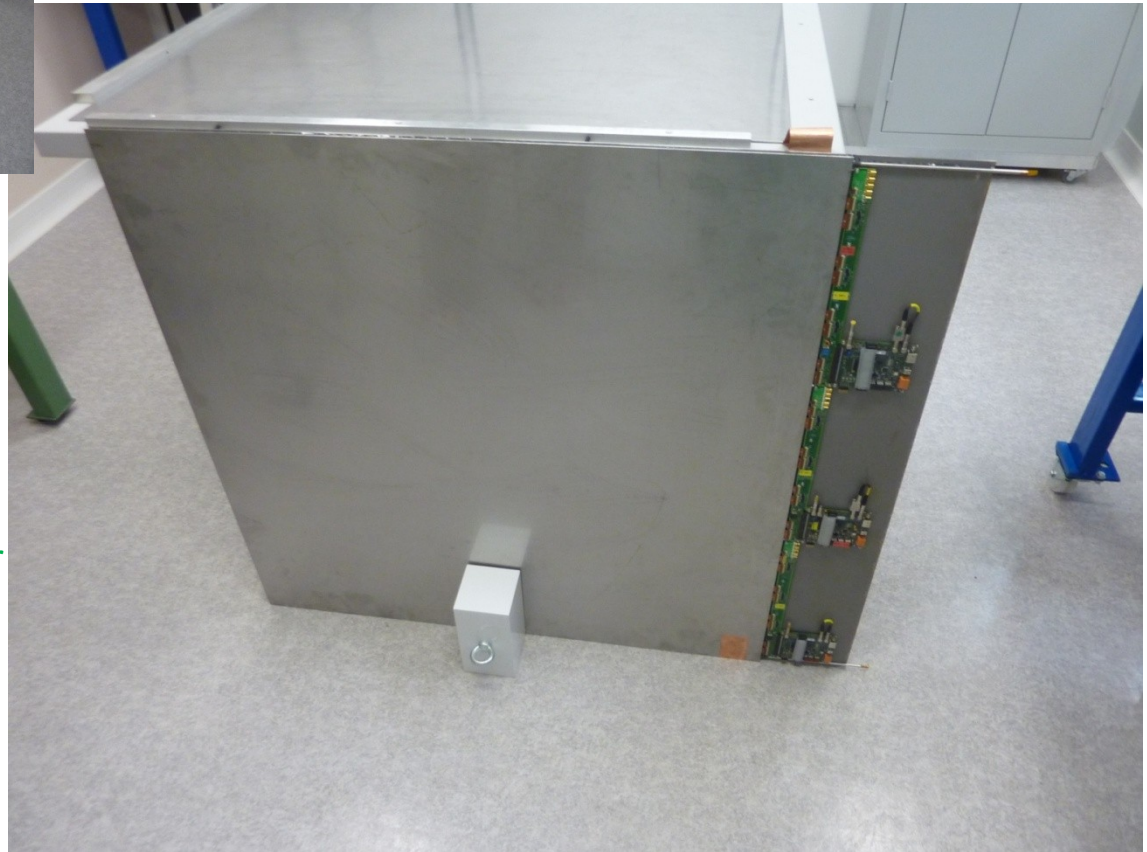
DHCAL Square Meter Assembly

MICROMEGAS Square Meter
With Hardroc2 & Hardroc2b



Inside the square meter

MICROMEGAS square meter structure



*See several physician's talk for
results on 2010 Beam Test*

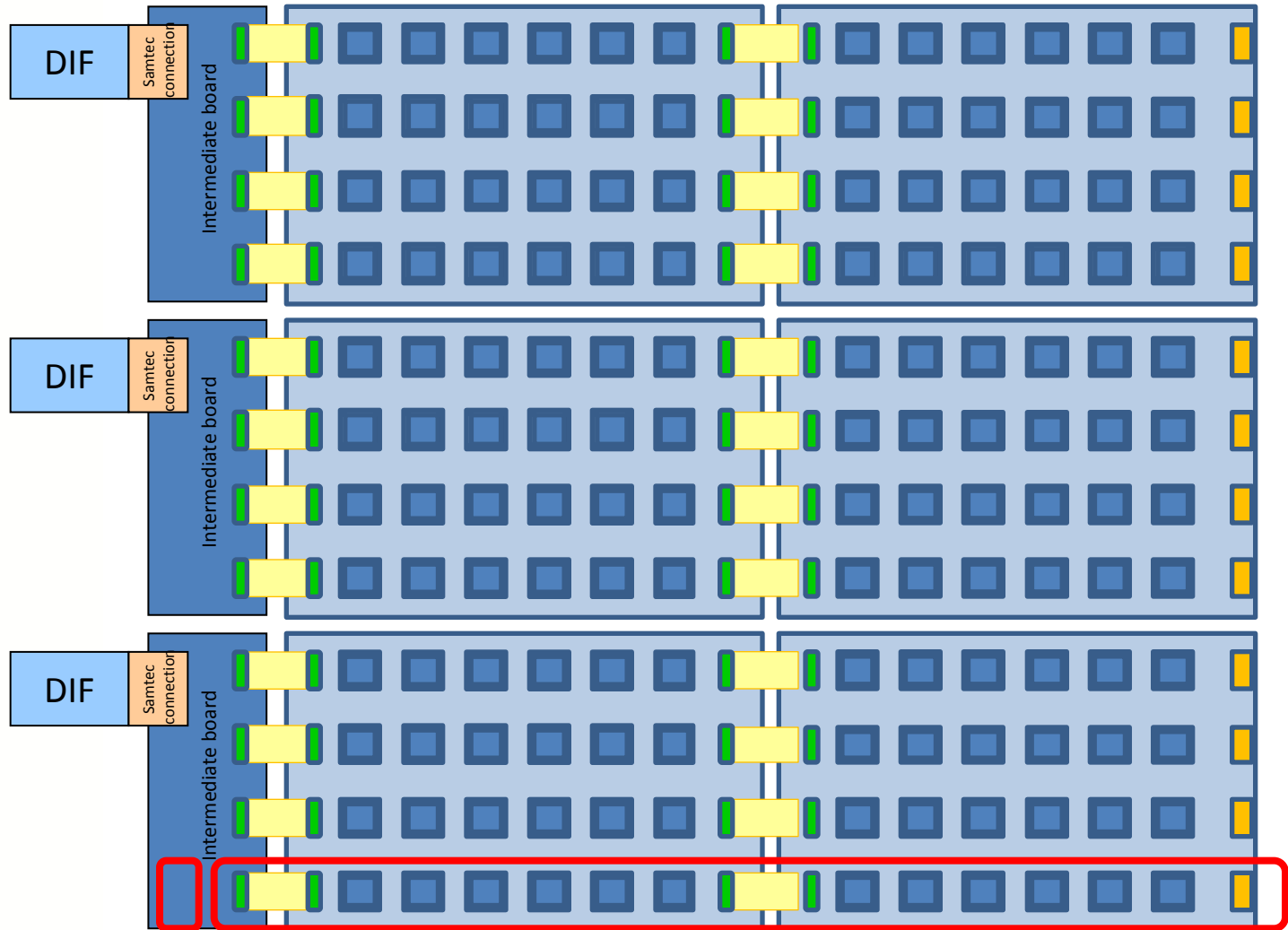
Micromegas DHCAL SLAB with Hardroc2/Microroc

1. Result in 2010

2. Works for 2011:

Microroc ASU – SLAB – M² detector

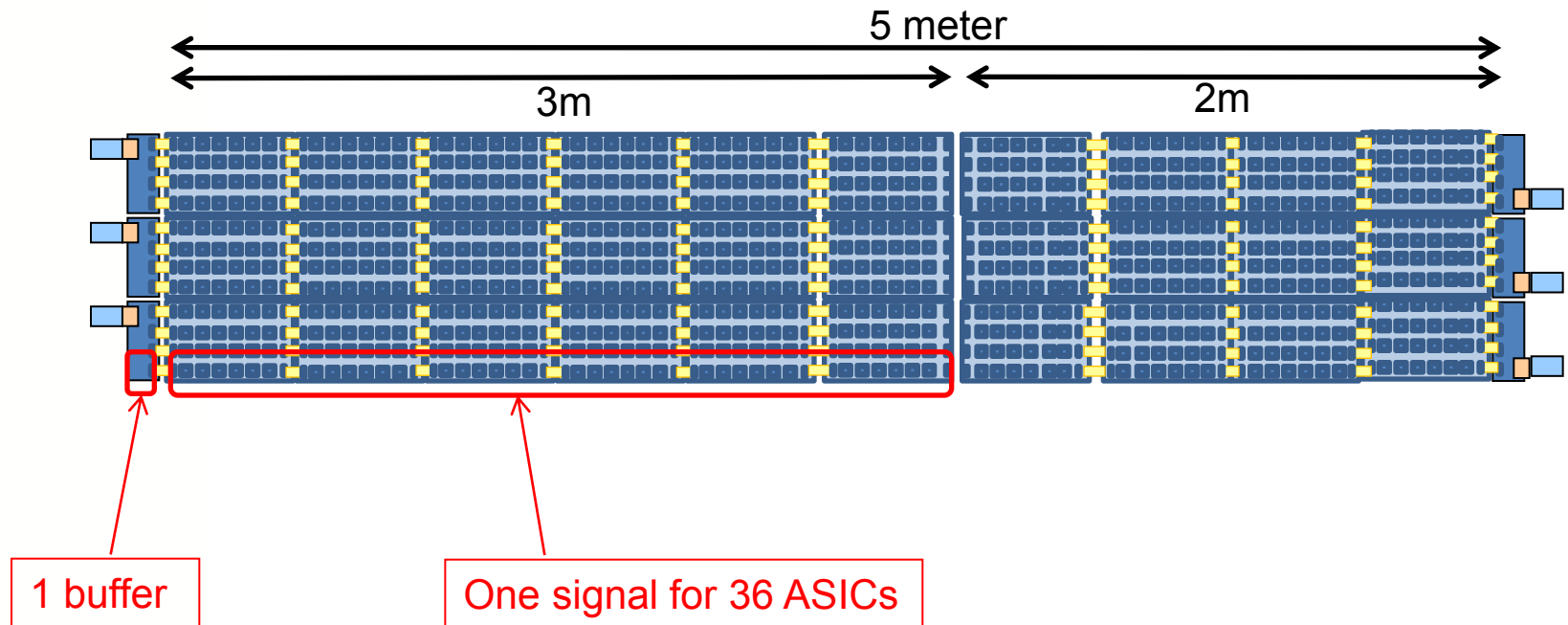
LAPP M²: Main principle



Buffer line

Independante line

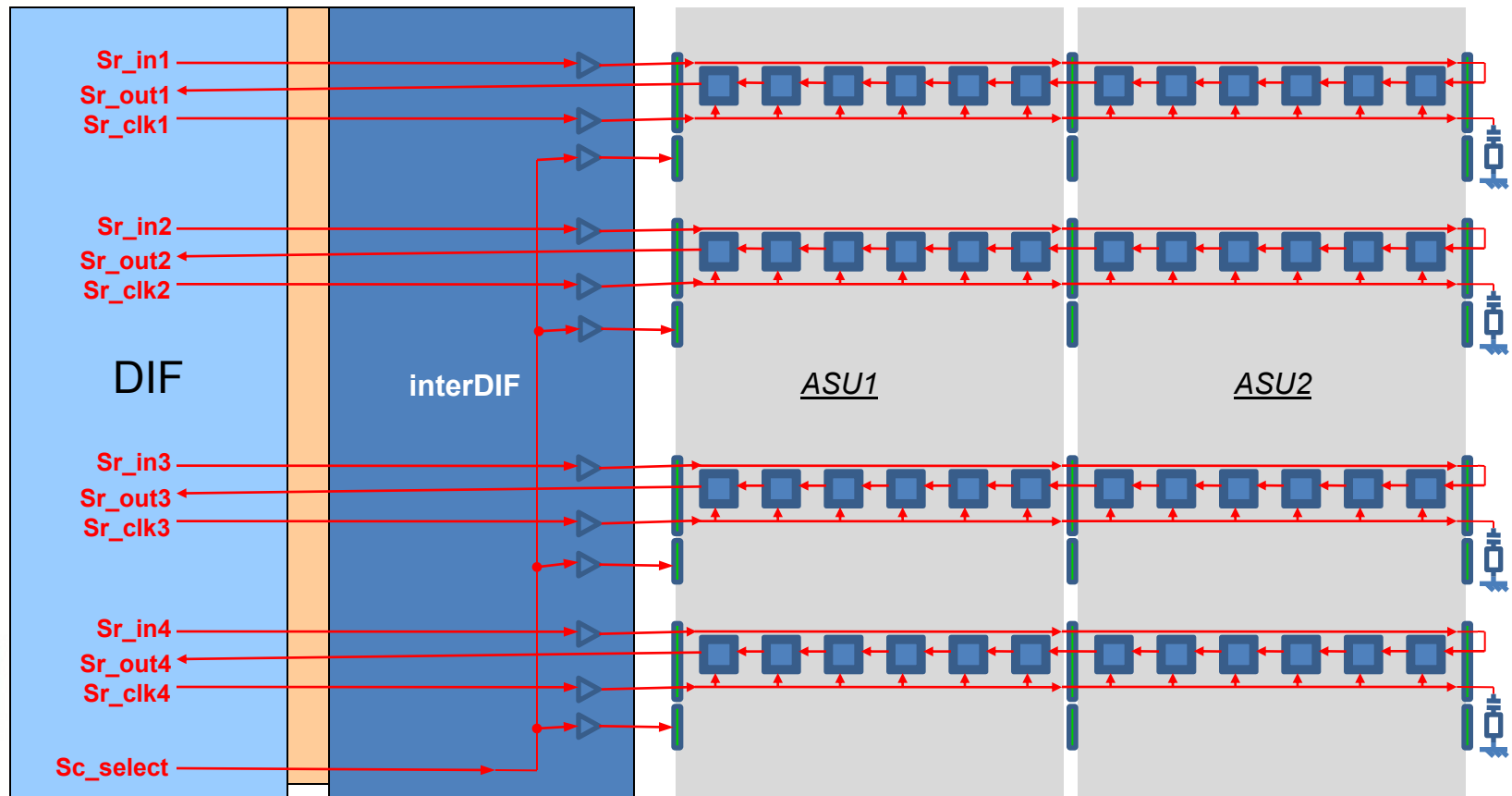
SLAB 3m and 2m



Driving line realistic

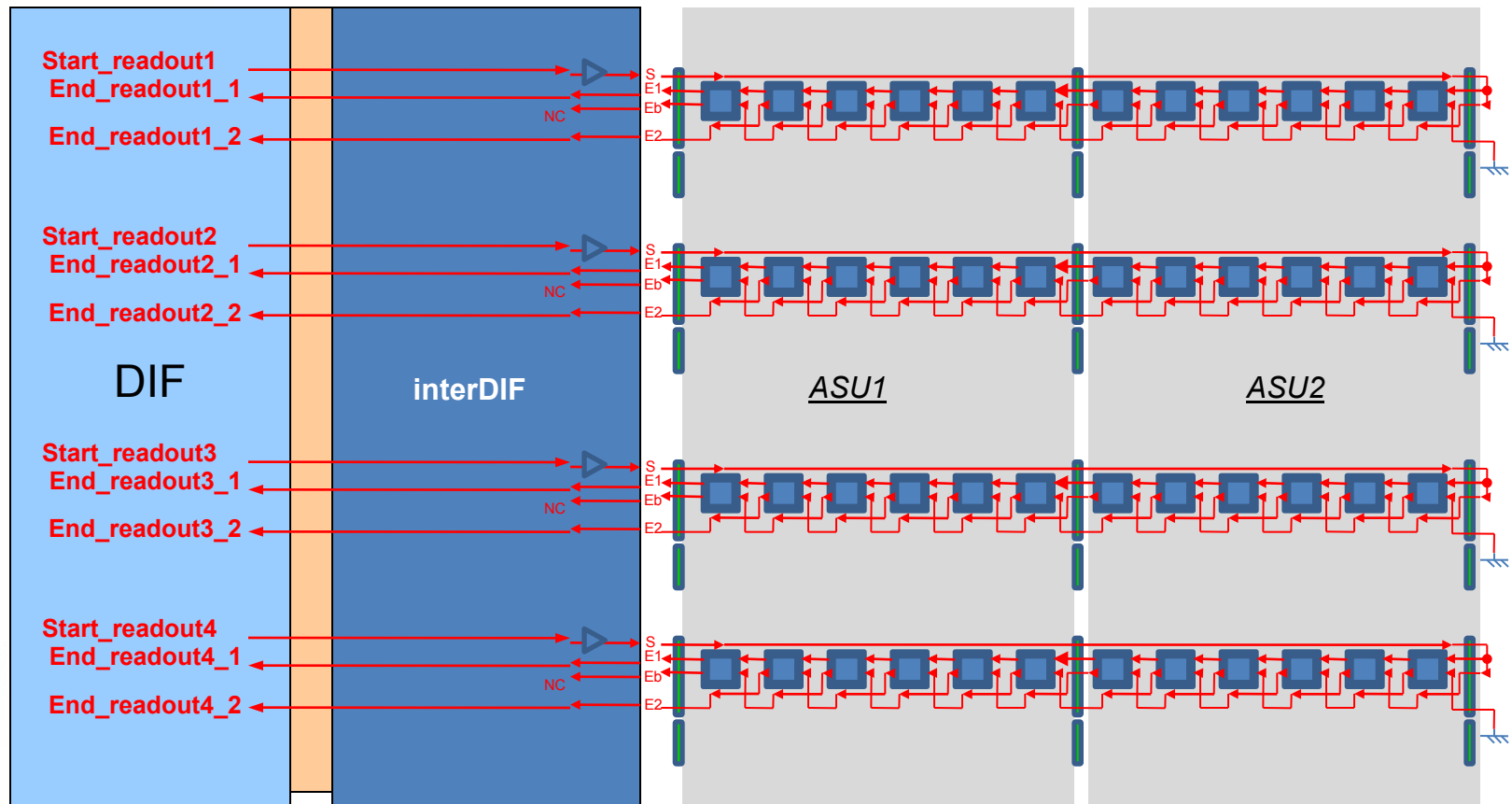
Chainage Slow-Control (et registre pour sortie analogique)

Liaison avec le FPGA de la DIF



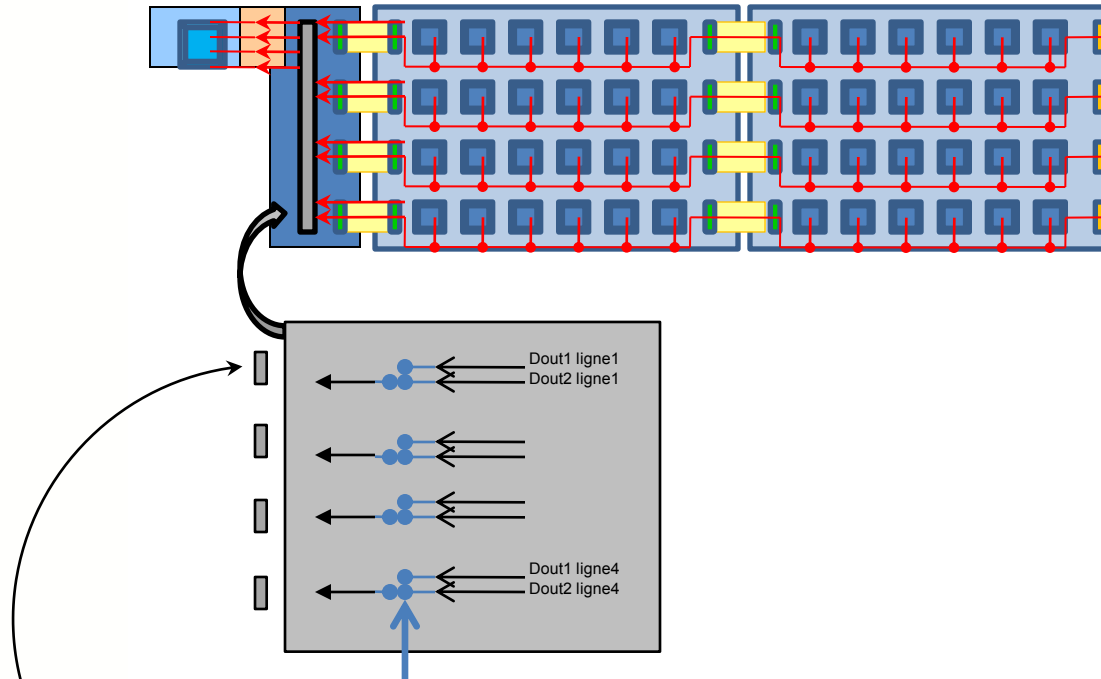
Double Chainage jeton readout

Liaison avec le FPGA de la DIF



Sortie « Dout »

Chaque ASIC à 2 sorties Dout disponible (au cas ou une sortie est en panne)
Une ligne de 12 ASIC sort 2 signaux Dout (au cas ou un est en défaut)

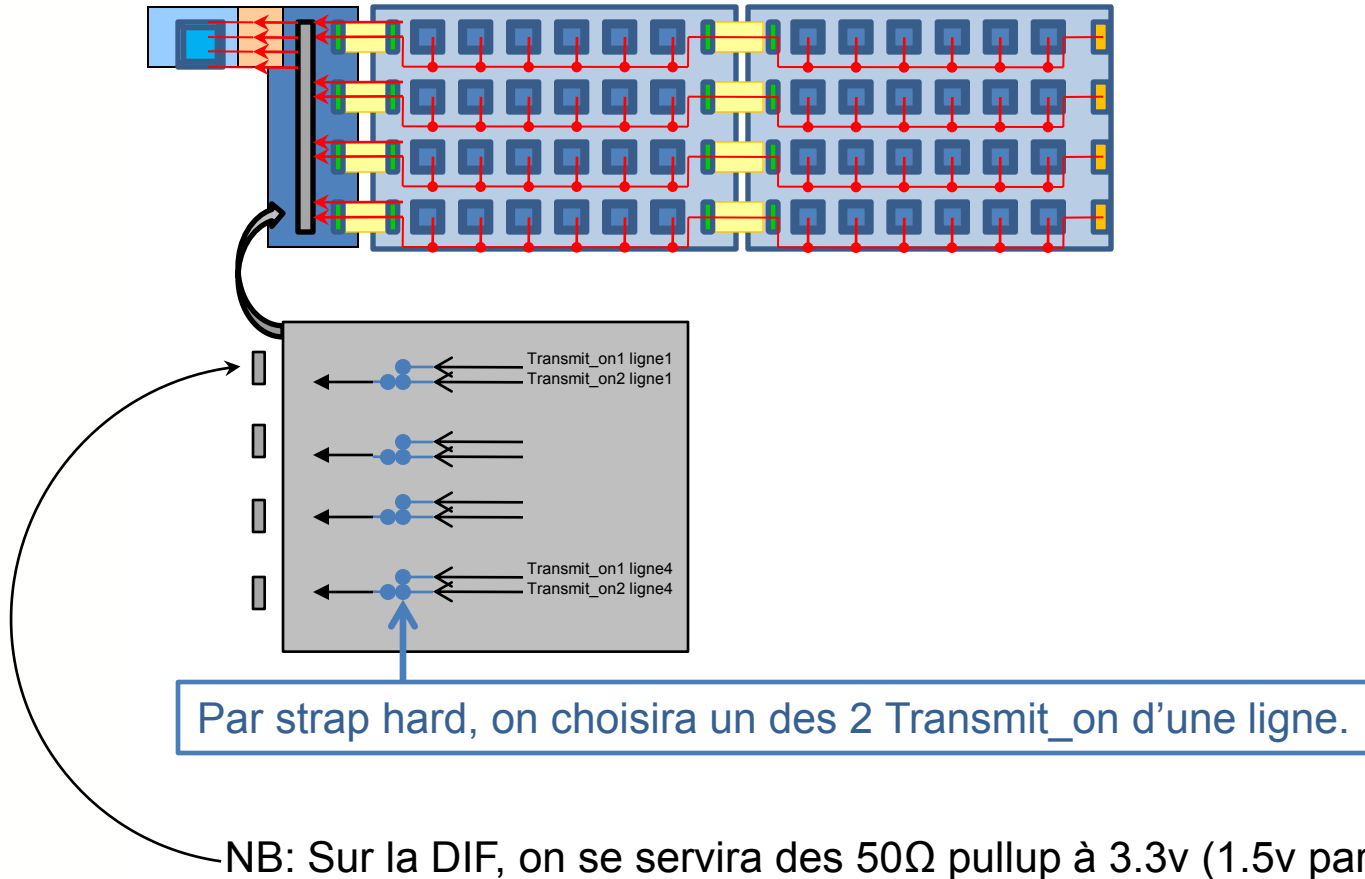


Par strap hard, on choisira un des 2 Dout d'une ligne.

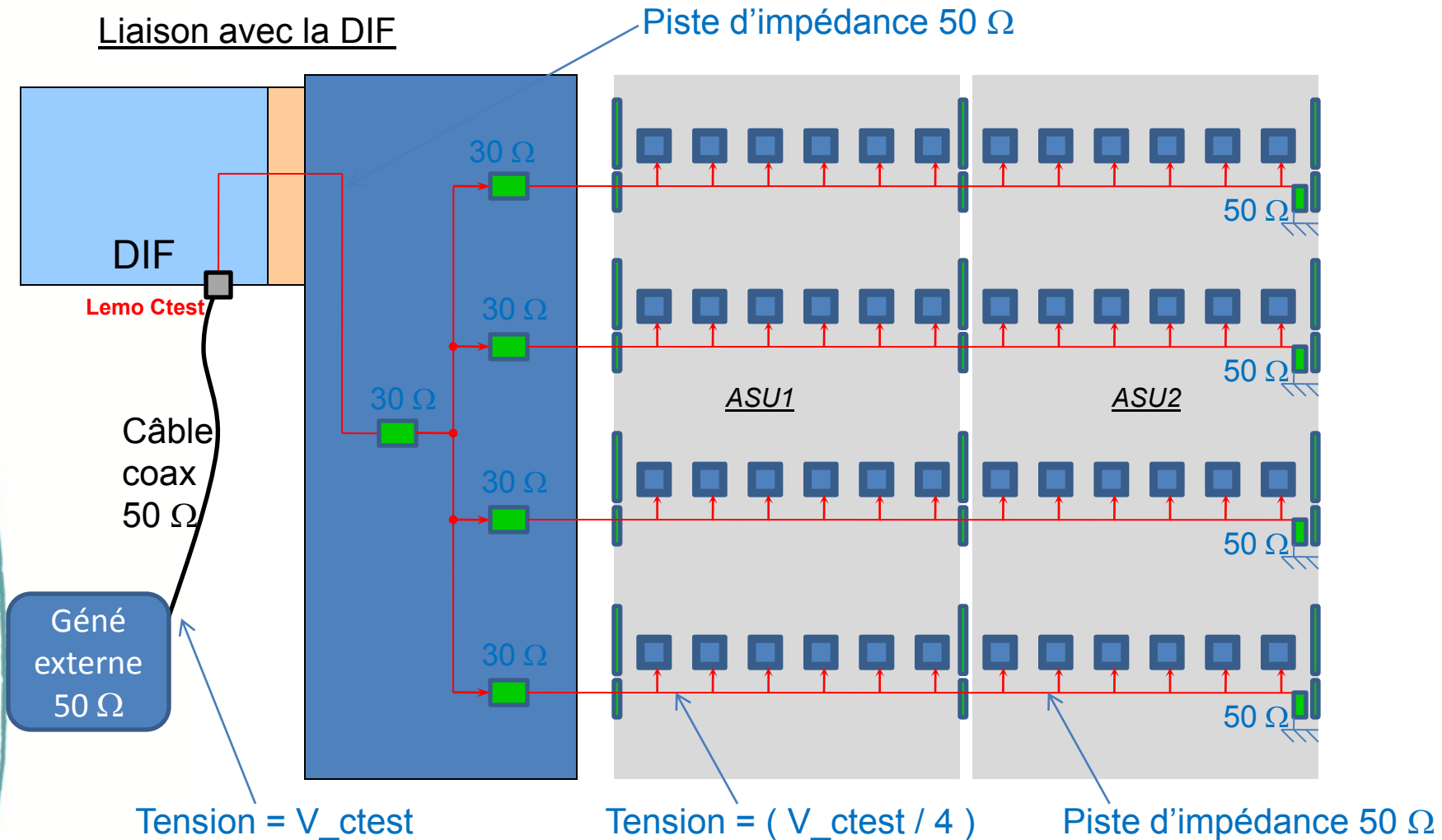
NB: Sur la DIF, on se servira des 50Ω pullup à 3.3v (1.5v par la suite)

Sortie « Transmit_on »

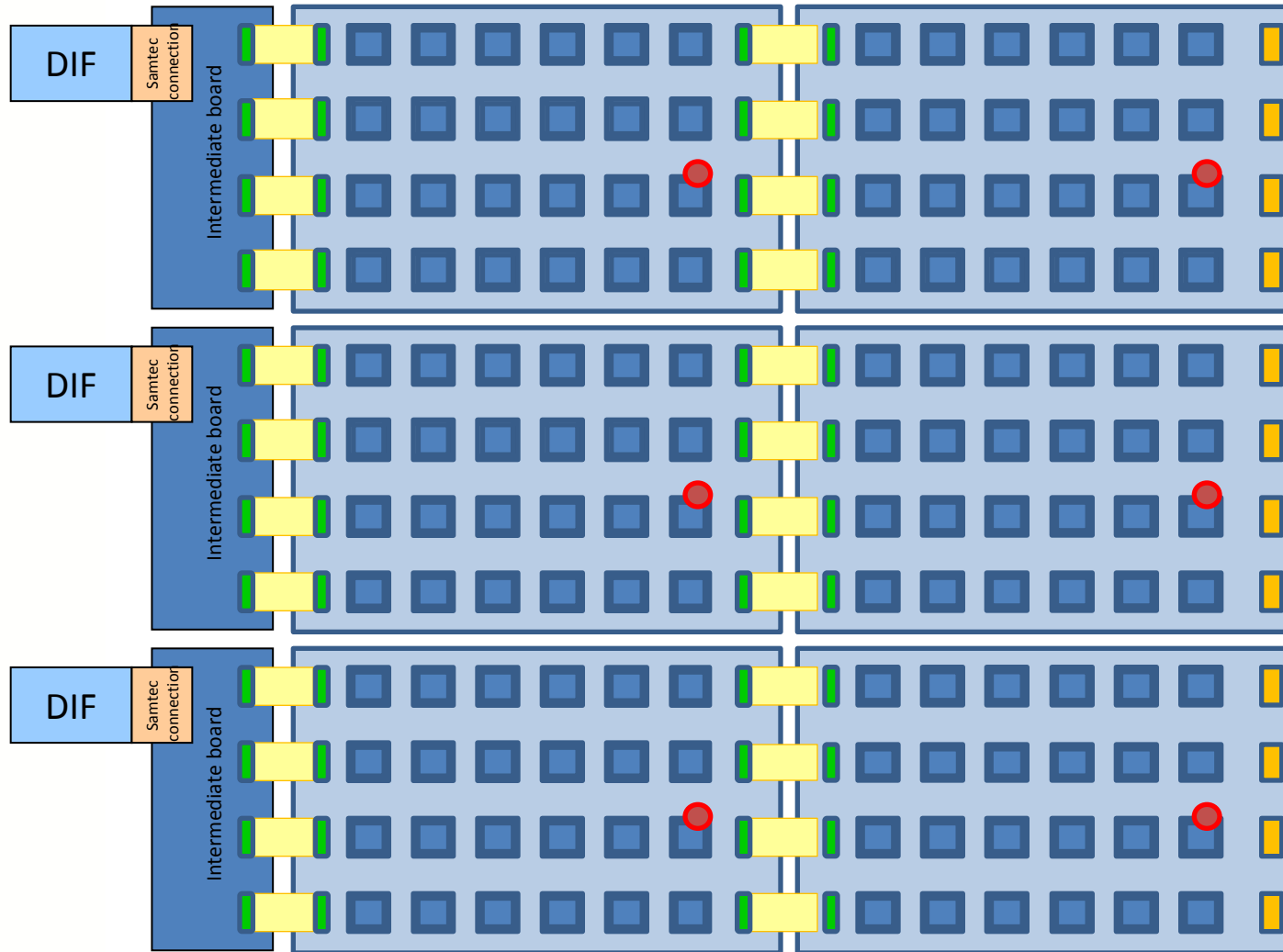
Chaque ASIC à 2 sorties Transmit_on disponible (au cas ou une sortie est en panne)
Une ligne de 12 ASIC sort 2 signaux Transmit_on (au cas ou un est en défaut)



Injection signal Ctest

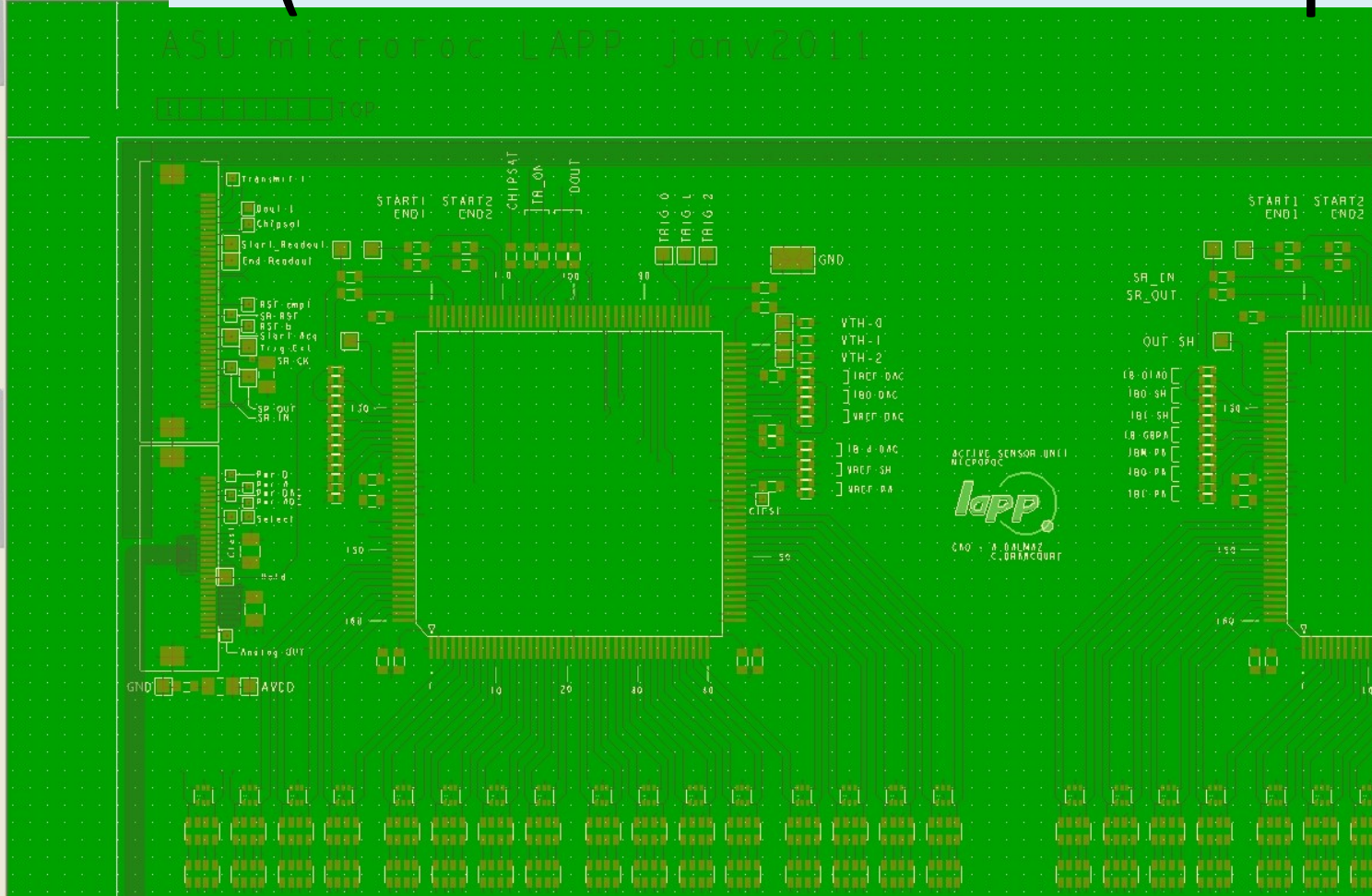


Sondes de Temperature



● *Emplacement des sondes de temperature*

PCB Layout Design (2 hierarchical level kept)



Views: [dropdown]

Layer	Etch	Via	Pin	Drill	All
Conductors	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Planes	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Top	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Gnd1	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Signal	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Alim	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Gnd2	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Analog	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Gnd3	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Bottom	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
All	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Options

Active Class and Subclass:

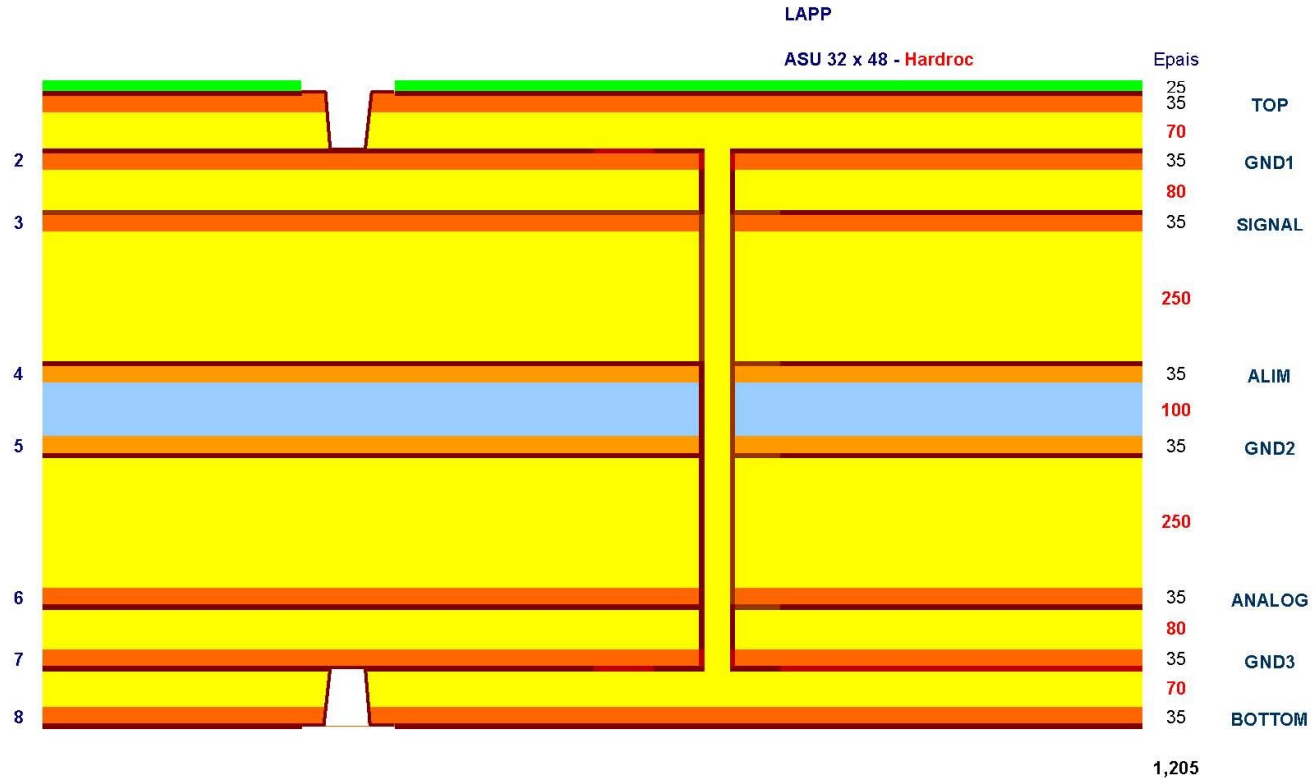
Board Geometry [dropdown]

Soldermask_Top [dropdown]

x Pick 1st corner of the new window.
last pick: -9.971 336.312
Pick to complete the window.
last pick: 61.259 253.925
Grids are drawn 1.600, 1.600 apart for enhanced viewability.
Command >

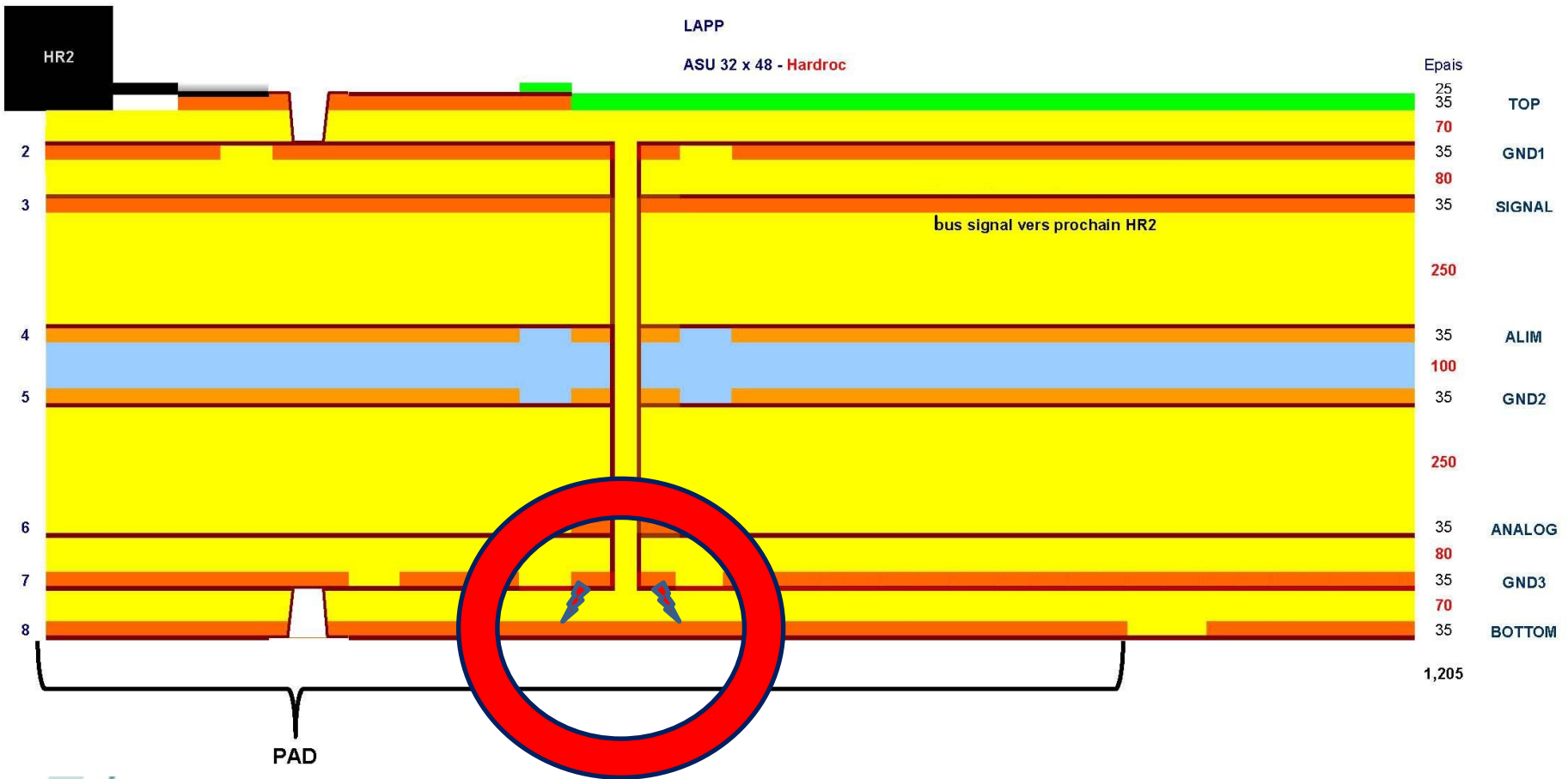


Stack Up ASU Hardroc (2009/2010)

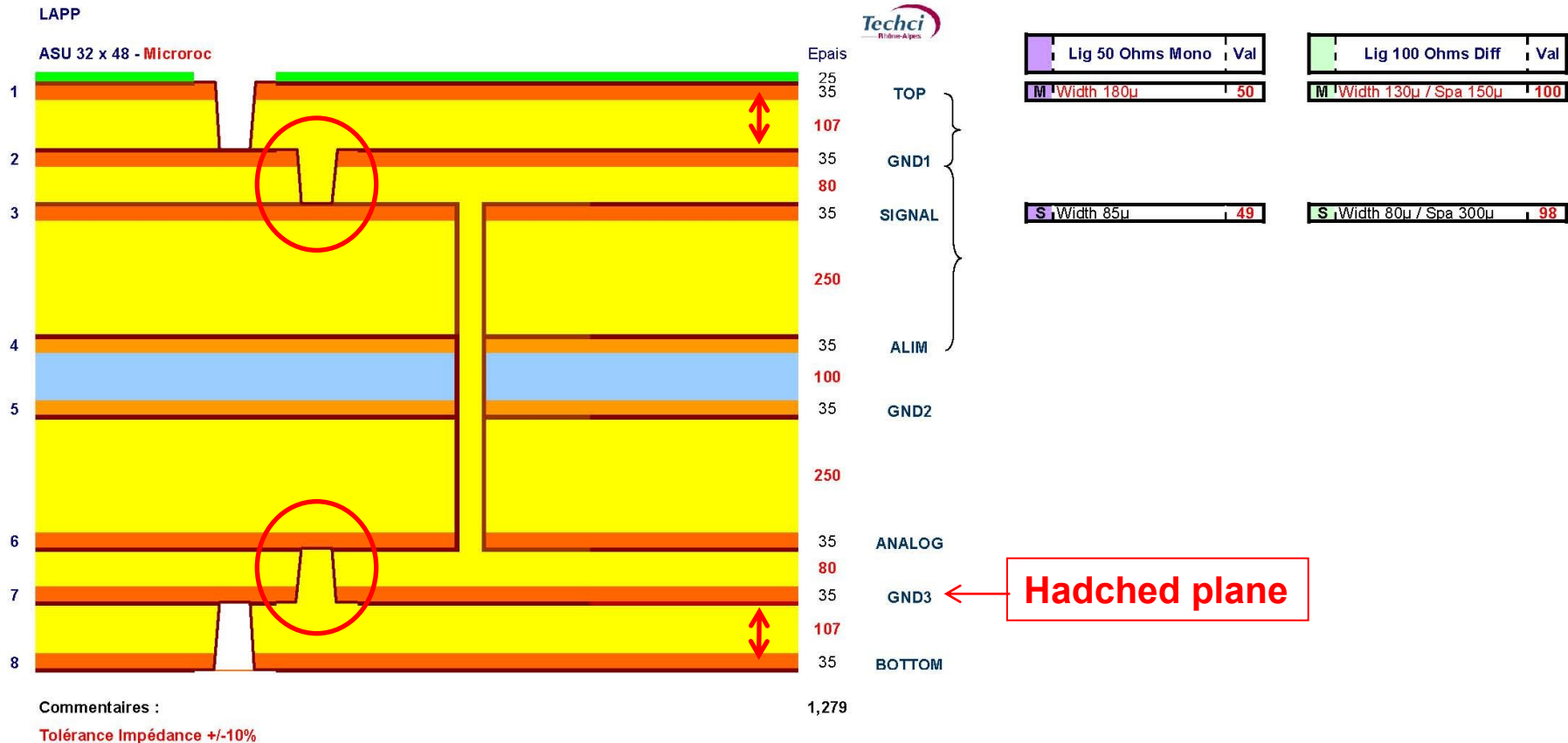


StackUp ASU Hardroc (2009/2010)

Cross talk



Stack Up ASU Microroc (2011)



Old Layout ASU MR routage PAD (july)

The image shows a screenshot of a PCB layout software interface. The main workspace displays a routing grid with green traces and vias. The interface includes a toolbar on the left, a command window at the bottom left, and several panels on the right.

Command Window:

```
x last pick: 29.400 8.600
+ Waiting for the destination pick.
+ last pick: 29.400 9.200
+ No DRC errors detected.
+ Pick another element to slide.
+ Command >
```

Right Panel - Active etch subclass:

- Analog

Right Panel - Net:

- Net: Null Net
- Corners: 45
- Max 45 len: 99999.00
- Bubble: Shove preferred
- Shove vias: Off
- Clip dangling clines
- Smooth: Off

Right Panel - Find:

Design Object Find Filter

All On All Off

- Groups
- Comps
- Symbols
- Functions
- Nets
- Pins
- Clines
- Lines
- Shapes
- Voids
- Cline Segs
- Other Segs
- Figures
- DRC errors
- Text
- Ratsnests
- Rat Ts

Right Panel - Visibility:

Views: [Dropdown]

Layer	Etch	Via	Pin	Drc	All
Conductors	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Planes	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Top	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
Gnd1	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
Signal	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
Aim	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
Gnd2	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
Analog	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Gnd3	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Bottom	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
All	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>

Bottom Status Bar:

ANALOG 43.300, 5.400 [P] [A] GEN [DRC]

Upgrade resume

1. **ASIC: Hardroc > Microroc** *to match with sensibility of micromegas*
2. **Diode: BAV99 > NUP 4114** *to perform the protection discharge*
3. **Link: 4 // readout chain on a DIF** *to increase the readout speed*
4. **Link: 4 // Configuration chain** *to increase the robustness*
5. **Link: Analog readout** *facility performance analyse and debug*
6. **Ctest: Passive Distribution on interdif** *to replace OP.AMP*
7. **Driver: no buffer on ASU** , *only on interDIF*
8. **Added function: Temperature Sensor (I2C)** *increase monitoring*
9. **PCB: added stage μ via** *to cancel Crosstalk*
10. **PCB: Hadched ground plane** *to decrease Pad Capacitor*
11. **PCB: height dielectric** *to decrease Pad Capacitor*

Mois: Janv. février mars avril mai juin juillet

Semaine: 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29

