

# AHCAL Electronics.

## DAQ and SPIROC2b integration issues

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Electronics and DAQ meeting  
Orsay  
Feb. 9th, 2011



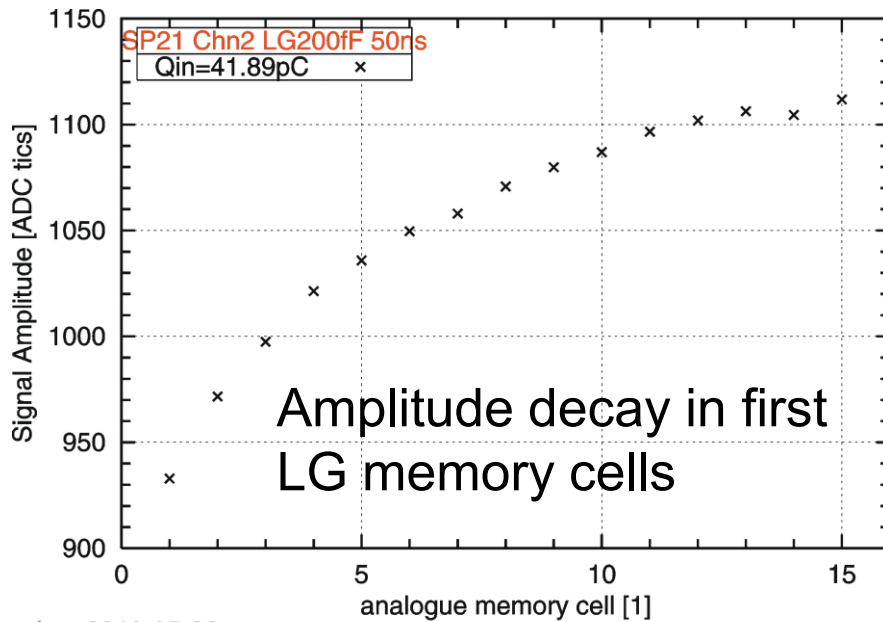
- > Electronics: Open Issues
  - open points during tests
  - SPIROC2b integration
- > DAQ Integration
  - Status Labview DAQ
  - Status Redesigns Boards (DESY)

**This is mainly the status from November 2010  
with few updates wherever possible.**

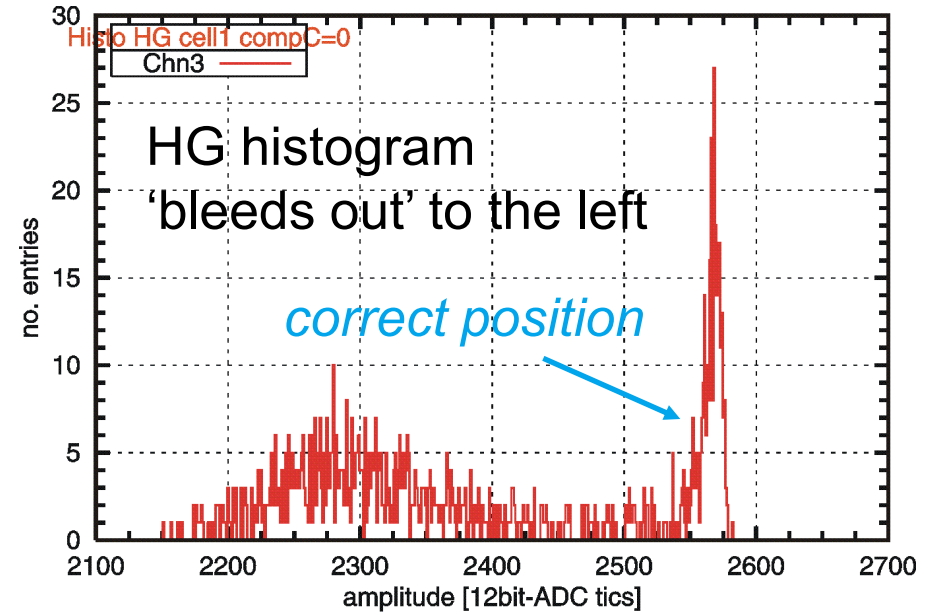


# SPIROC2 open issues : Reduced amplitude

## Problem: Cell dependent amplitude



date 2010-05-28



date 2010-09-10

Effect cannot be eliminated as at LAL  
by a high blocking-cap on VDDD2 (R. Honda)

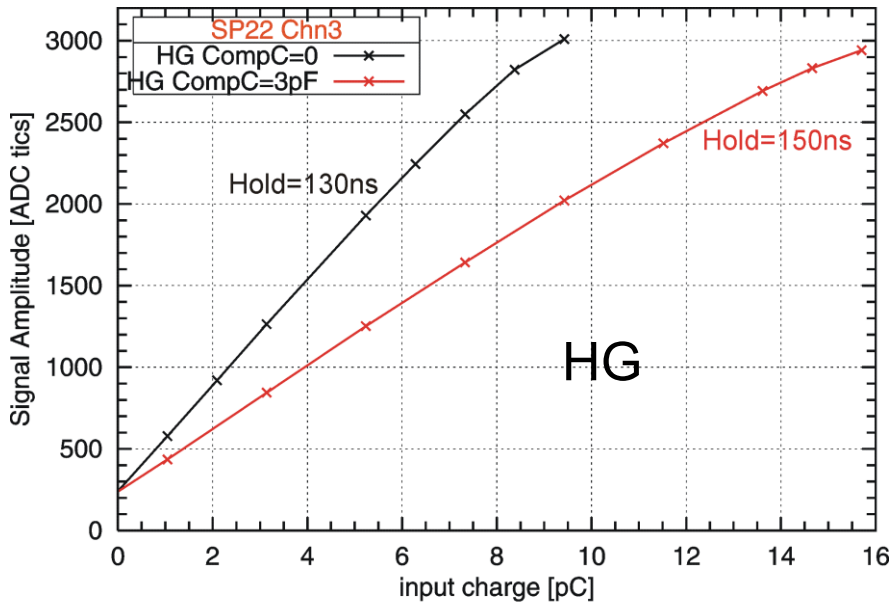
Effect =  $f(\text{amplitude, input signal shape, PA comp. caps})$   
Effect  $\neq f(\text{trigger rate, block-caps}@100\mu\text{F})$

HG PA=100fF, LG PA=200fF  
50 ns shaping, ext. Hold/Trig.  
hold-time=95ns (LG), 130ns (HG)  
Charge Injection with 5ns risetime.  
No PA compCs



# SPIROC2 open issues : Reduced amplitude

## Dynamic Range HG and LG



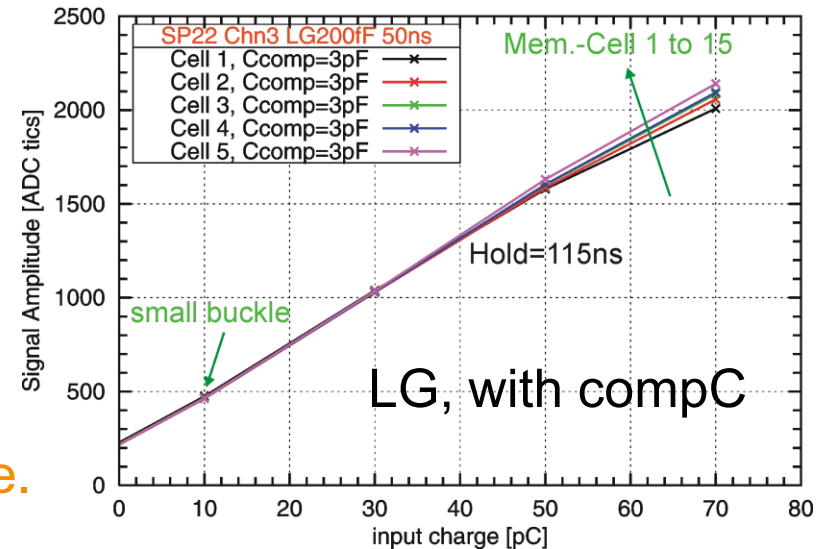
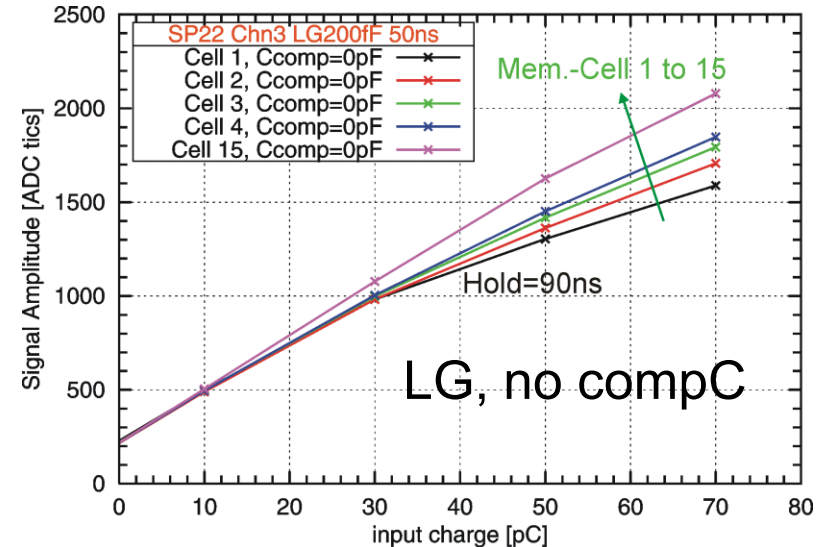
date 2010-09-10

CompCs improve severely cell uniformity,  
CompCs increase HG dynamic range,  
CompC=3pF still not large enough  
for very fast signals

⇒ Input signal shape changes amplitude.

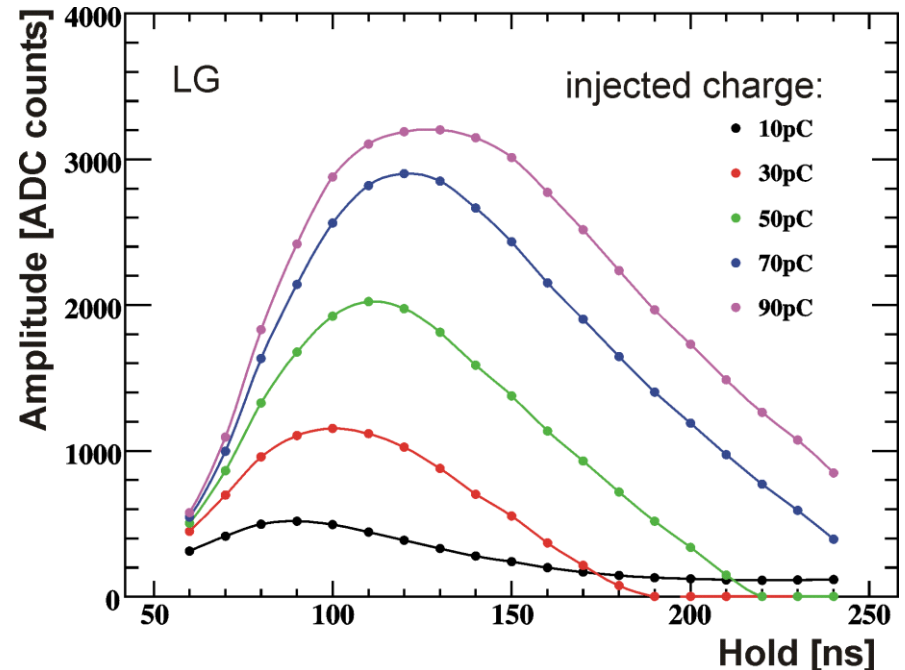
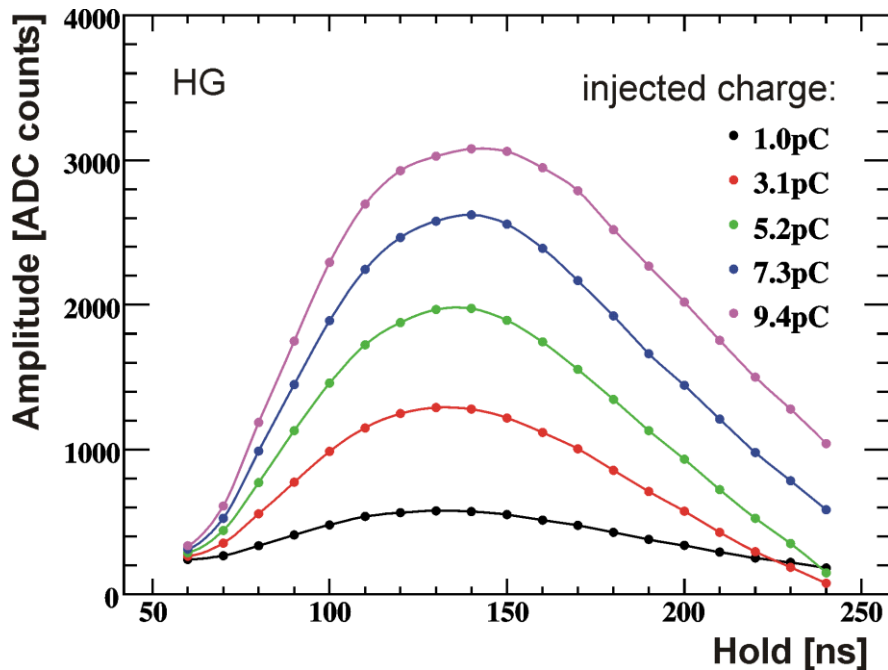
⇒ Bad linearity.

HG PA=100fF, LG PA=200fF  
50 ns shaping, ext. Hold/Trig.  
Charge Injection with 2ns risetime.



# SPIROC2 open issues : Holdscans

**Problem: Position of Hold-Maximum depends on signal amplitude.  
Position is different for HG and LG**



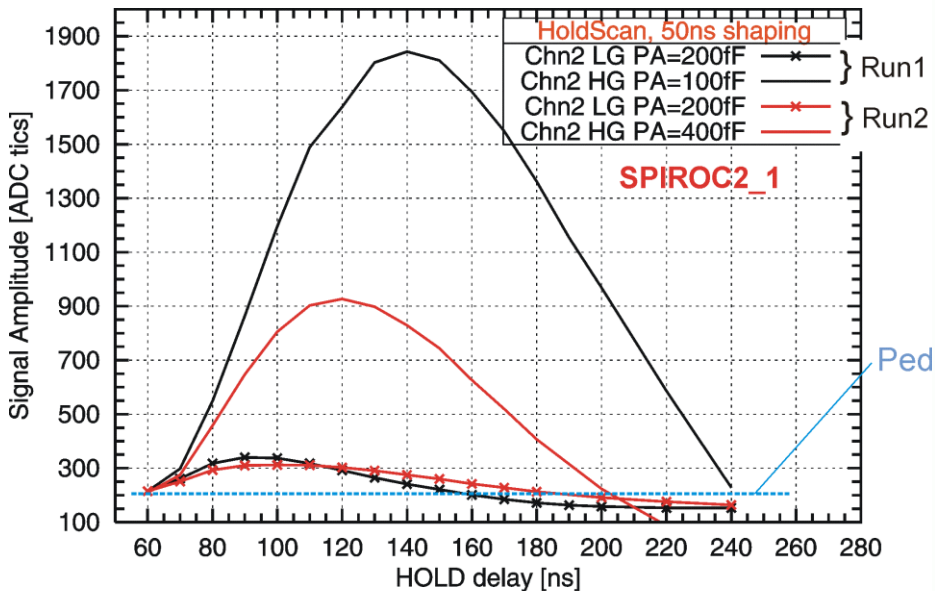
Compensation capacitors do not improve this behaviour.

HG PA=100fF, LG PA=200fF  
50 ns shaping, ext. Hold/Trig.  
Charge Injection with 2ns risetime.  
No PA compCs

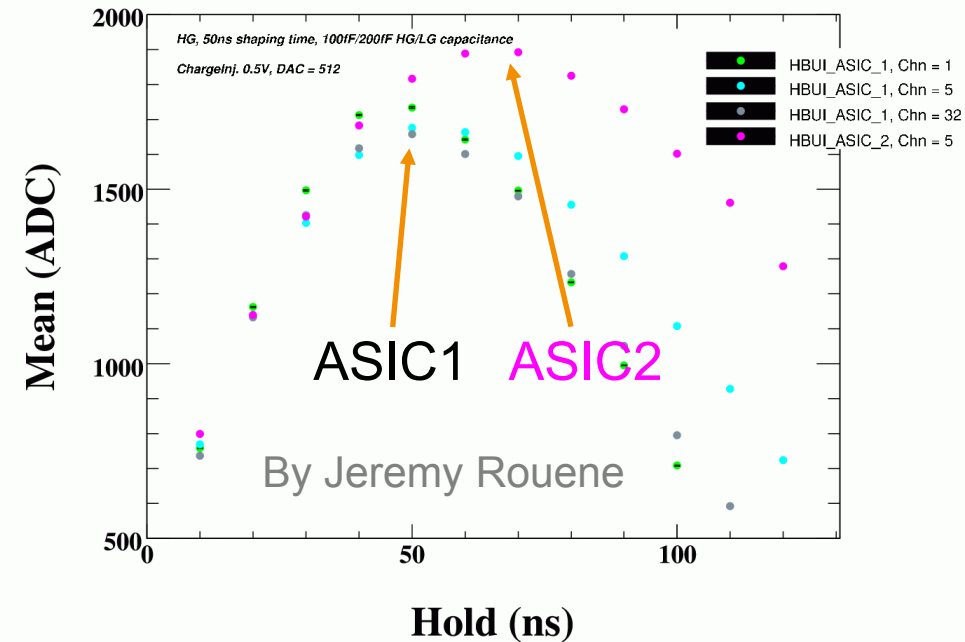


# SPIROC2 open issues : Holdscans

**Problem: Position of Hold-Maximum depends on preamp. setting (left) and varies from ASIC to ASIC (right)**



date 2010-05-25

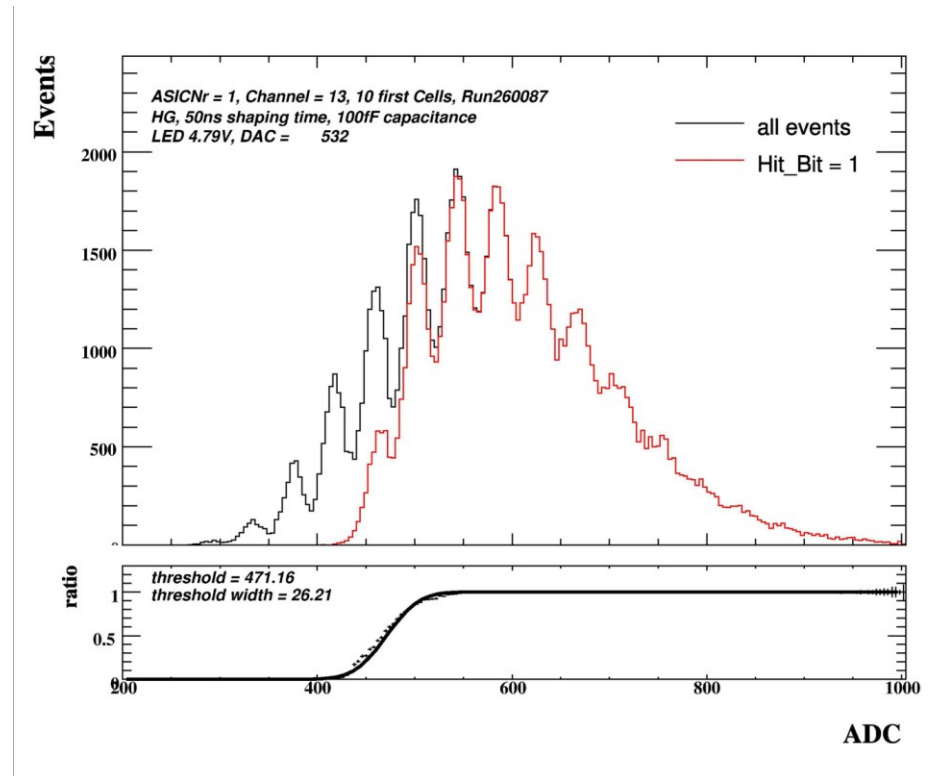
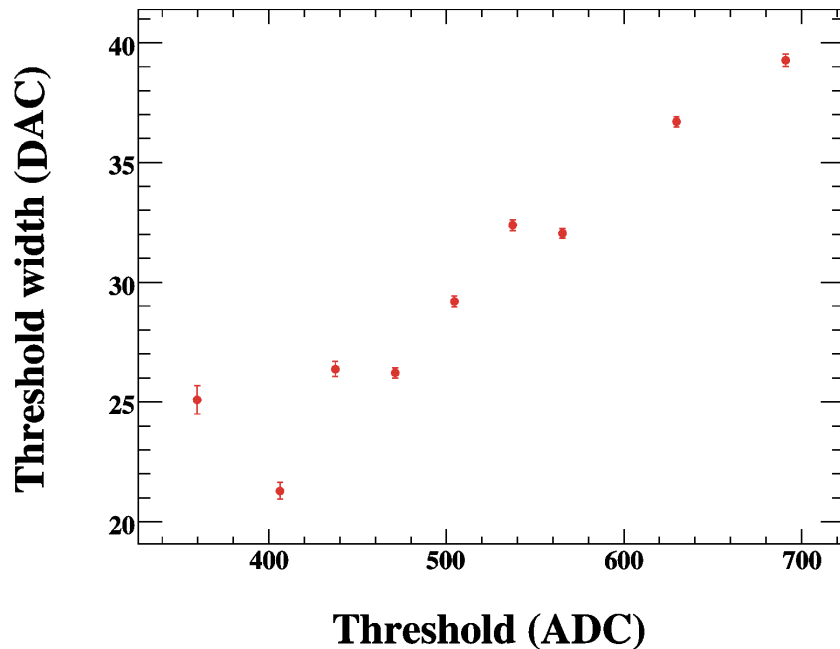


Charge Injection with 5ns risetime.  
50ns shaping, ext. Hold/Trig  
No PA compCs



# SPIROC2 open issues : Autotrigger

**Problem: Autotrigger threshold width depends on amplitude and is rather broad at  $\frac{1}{2}$ -MIP ( $\sim 20$  DAC tics)**

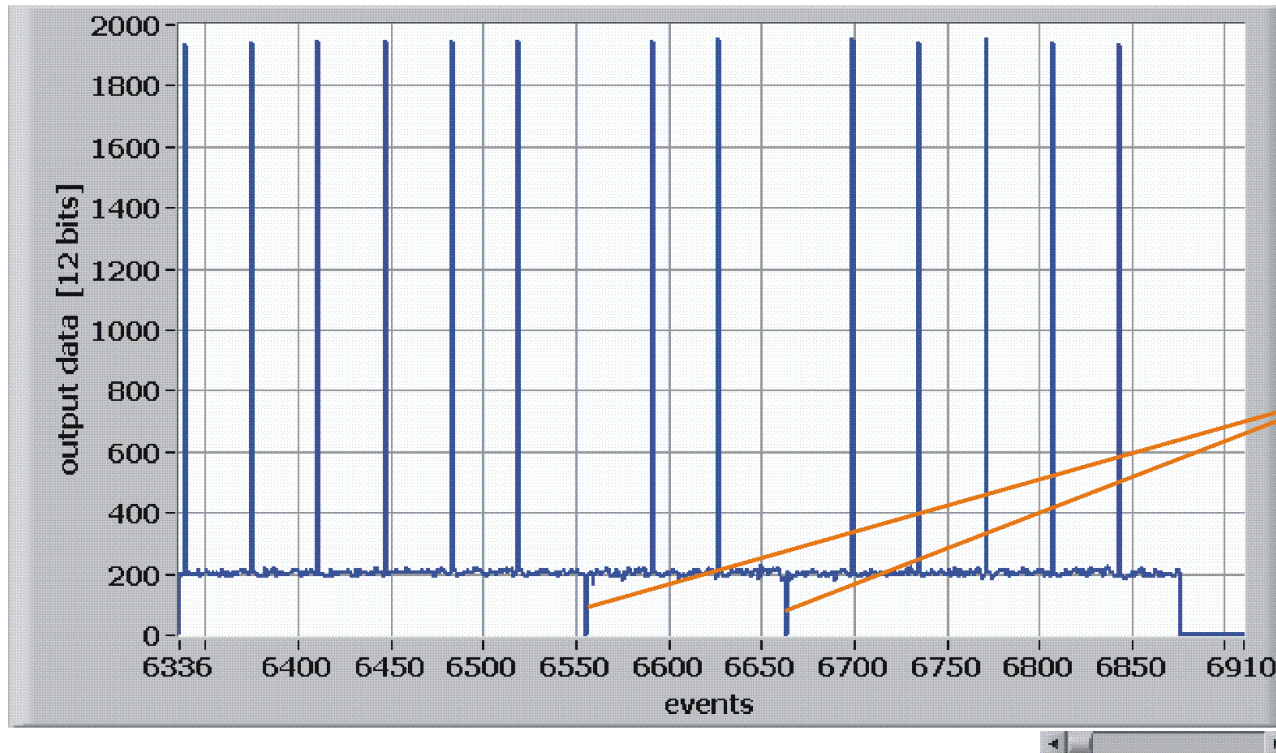


Effect of Hit-Bit? Could be verified in simulation?

**Autogain, e.g. @20MIP: Width and dynamic range of threshold?**



# SPIROC2 open issues : Arbitrary zero events



All channels show sometimes single events with 'zero' as output (no pedestal value but '0').

No dependence of this effect observed so far.





# SPIROC2b integration

- > Initial Plan : SPIROC2b on HBU2 (see timeline new boards)
- > SPIROC2b to current HBU (verify OMEGA results)
  - one HBU equipped with 2 SPIROC2b. But no time up to now to test...
- > SPIROC2b on current HBU:
  - Labview is ready,
  - DIF firmware needs adaption (sc-data), 2 weeks needed,
  - hardware needs changes (trigger/hold setup) on CALIB board.
- > Power pulsing is only possible with SPIROC2b.



# AHCAL DAQ – Status

- > Full operation with Labview/USB DAQ now.
- > CALICE DAQ modules arrived at DESY, still waiting for some new modules suggested by LLR (e.g. network adapter).
- > CALICE DAQ integration foreseen for new electronics generation
  - we start with a copy of LLR setup as soon as the analogue tests allow it.
  - Python-based control at first. How do we dive into XDAQ (no experience/knowledge so far at DESY-FE).
- > DIF firmware structure/block definition within DIF task force
  - command set defined
  - exchange of VHDL blocks via svn repository
  - proposal for DIF firmware block structure and –intercommunication (LLR). Needs to be changed for AHCAL DIF firmware (1 month).
  - **A lot of work done by LLR and LAPP – THANKS A LOT!!!!**

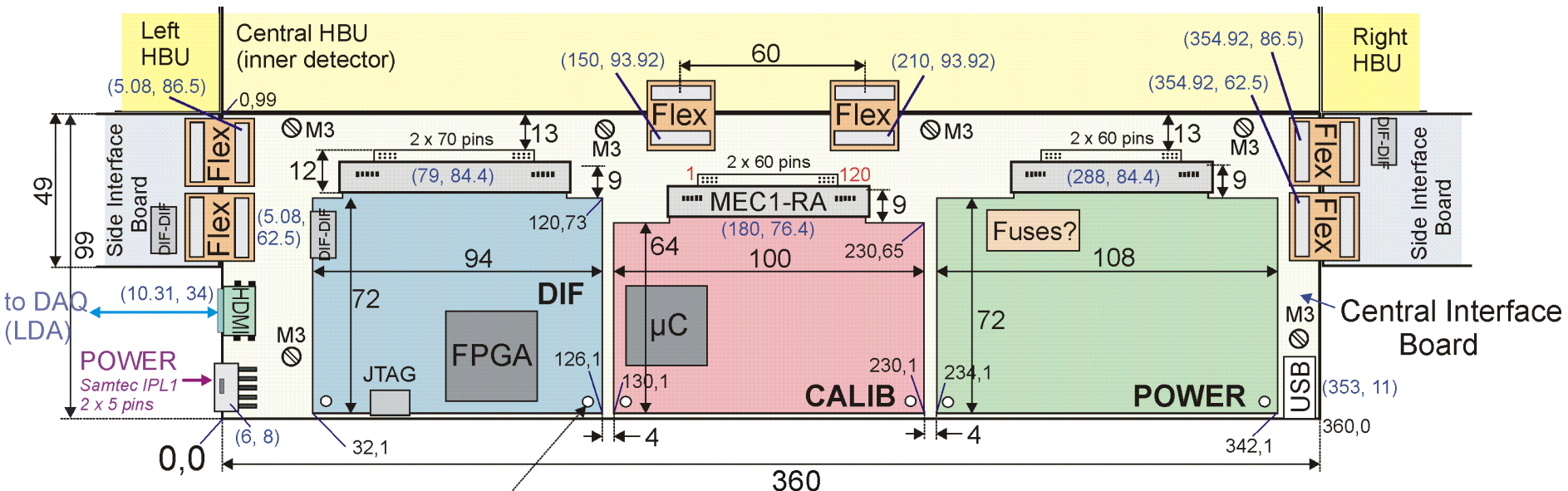


# AHCAL DAQ – Received Hardware from UK

- LDA (with all mezzanines?) + power adapter: 8x
  - Clock&Control card 2x
  - ODR 1x
  - Power Supplies (metal box, 220V, for C&C?) 2x
  - HDMI cables (non halogen free) 10x (8x: 2m)
  - optical cables (ODR-LDA) 8x
  - DAQ PC 1x
- 
- Ordered hardware to copy LLR setup: Copper-SFP (arrived), network adapter card (STILL not there).

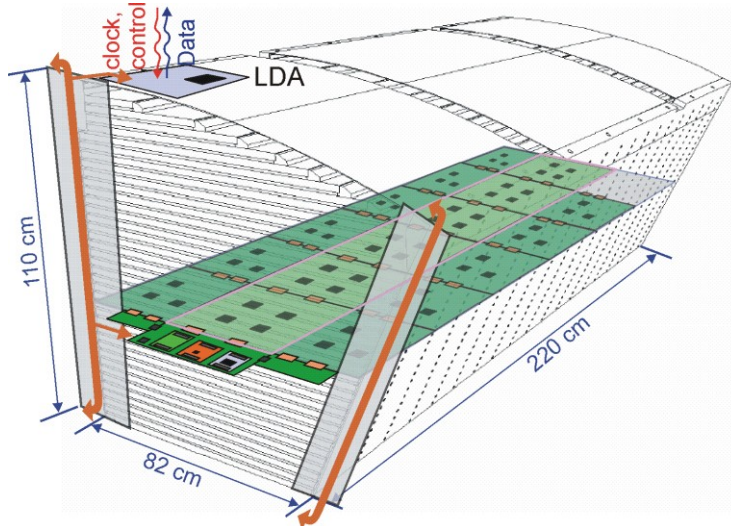
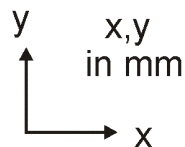


# New generation's modules



**(x, y): Connector Origin**

- USB: CONN000163
- IPL1: CONN001758
- HDMI: CONN001224
- Flex: CONN001123
- MEC1 (140pin): CONN001706
- MEC1 (120pin): CONN001776



Designs to be done:  
 CIB, SIB, DIF, CALIB2, POWER2,  
 HBU2, (Flexleads)



# Status Redesigns

	DIF	CALIB2	POWER2	HBU2	CIB	SIB	Flexleads
concept dev., circuit design							
schematic entry	NIU 						
Layout	NIU 						
Production	NIU 						

done

in preparation

not started yet

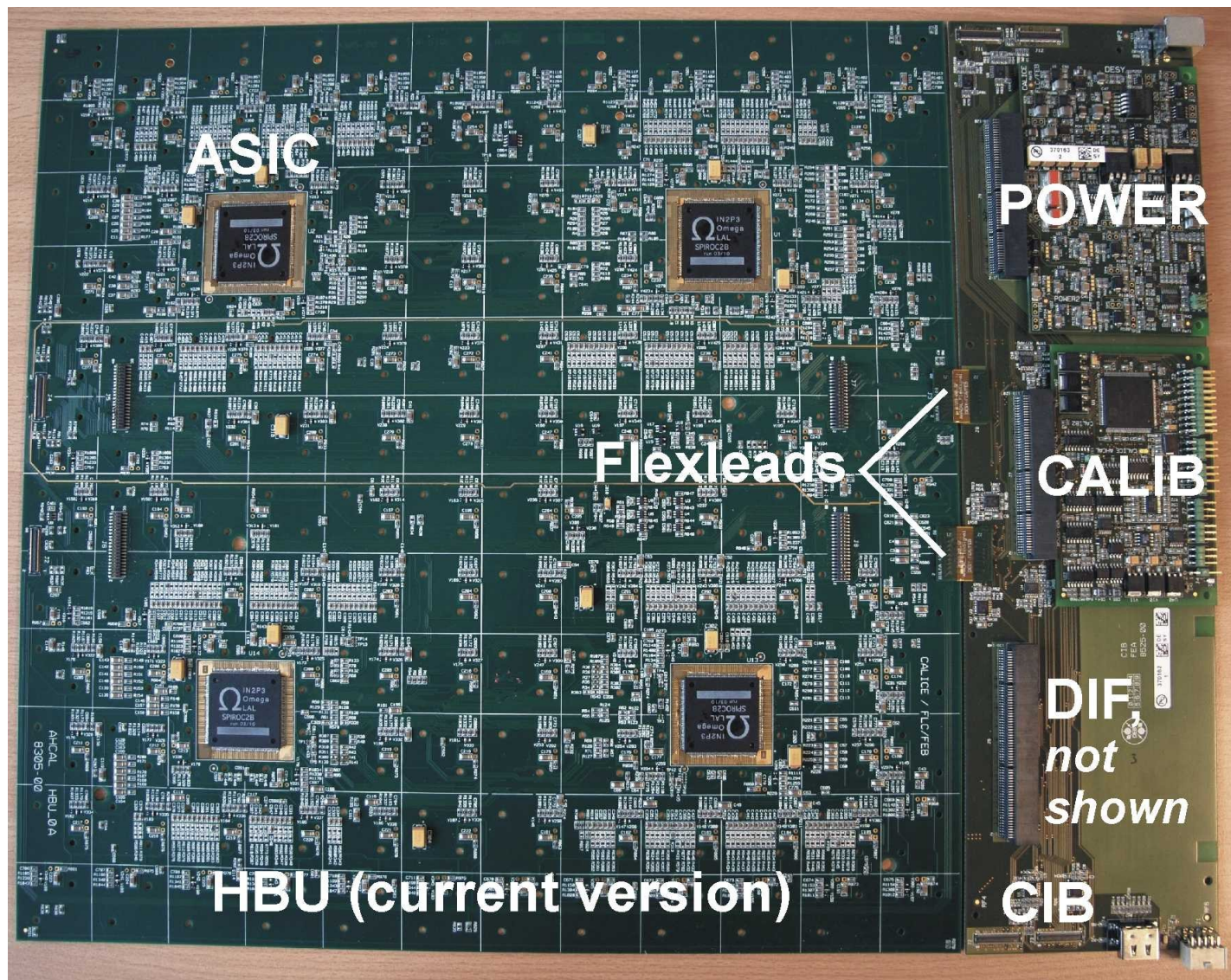
- > Most critical part: HBU2. **Stopped due to LED circuit problems.** Expected end March 2011. **HBU2 can carry SPIROC2, 2a or 2b.**
- > SIB is not needed for layer module => delayed.
- > DIF design taken over by NIU – thank you!!

new electronics ready end March. 2011, with basic testing end Apr. 2011.  
=> **DAQ integration Feb 2011 (duplication LLR setup)**





# AHCAL: Current Electronics



HBU (current version)

