

## ILD vertex detector powering

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$x$ Detector specifications
$x$ CMOS sensor VXD
$x$ Power integration strategy
$x$ Details on each area
$x$ Summary

## ILD vertex detector specifications

- Goal=impact parameter resolution
x Intrinsic sensor spatial resolution
$\rightarrow$ high granularity: single point resolution $3 \mu \mathrm{~m}$
- $10^{8}(\mathrm{CMOS})$ to $10^{10}(\mathrm{FPCCD})$ pixels
x Multiple scattering


Require 0-suppression
$\rightarrow$ power
$\rightarrow$ Low material budget for the whole system

- few $0.1 \%$ X0 range per layer


## Environment

$x \quad$ Large beam background hits
$\rightarrow$ Dominates the data throughput, whatever the technology


- O(20) Mbits / train
x Inner region
$\rightarrow$ Not much space
$\rightarrow$ "adiabatic" operation important / thermal budget
$\rightarrow$ Light structure important / material budget

The CMOS sensor-based VXD

Two geometries
x 3 double-sided layers $=$ baseline
$\rightarrow$ Double-sided $=$ one support equipped with sensors on both sides
x 5 single-sided layers
x Same envelope
$\rightarrow$ Radius coverage
$\rightarrow$ Ladder-end support

| layer | radius (mm) | width (mm) | length (mm) | \# ladders | \# sensors* |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathbf{1}$ | $16 / 18$ | 11 | 125 | 14 | 168 |
| $\mathbf{2}$ | $37 / 39$ | 22 | 250 | 26 | 312 |
| $\mathbf{3}$ | $58 / 60$ | 22 | 250 | 40 | 480 |
| total |  |  |  | $\mathbf{8 0}$ | $\mathbf{9 6 0}$ |

* Numbers corresponding to current CMOS technology ( $0.35 \mu \mathrm{~m}$ ) prototypes
$\qquad$


## CMOS sensors for the VXD

## Embedded functionalities

x In-pixel: pre-amplification pedestal suppression
$x$ periphery: digitization + zero-suppression
$x \quad$ Readout strategy $=$ rolling-shutter
$\rightarrow$ Only during train
$\rightarrow \mathrm{t}_{\text {integration }}=\mathrm{t}_{\text {read-out }}$
$x$ Existing prototype:
$\rightarrow 2 \mathrm{~cm}^{2}, 0.6$ Mpixels, $\mathrm{t}=100 \mu \mathrm{~s}$ in CMOS $0.35 \mu \mathrm{~m}$
$\rightarrow$ Development IPHC \& IRFU
$\rightarrow$ Evolution toward CMOS $0.18 \mu \mathrm{~m}$


- Optimization / layer
x Inner layer: face large beam background
$\rightarrow$ shortest readout-time $\sim 25 \mu s$
$\rightarrow$ pixel pitch $16 \times 16 \mu \mathrm{~m}^{2}$
x Outer layers: optimize power
$\rightarrow$ larger pitch ( $35 \mu \mathrm{~m}$ )
$\rightarrow$ Keep resolution with 4 bits ADC
$\rightarrow$ Detailed discussion in
Marc Winter's talk, tomorrow


## Power pulsing sensor

## Pulsing strategy

$x$ Activity period $\sim 2$ to 4 ms over the 200 ms train
$\rightarrow$ Estimated duty cycle range: $1 / 50$ to $1 / 100$
$x$ For stability reasons, not all element switchable
$\rightarrow$ Test started for the analog part
$\rightarrow$ To be done for the digital circuitry


| Assuming: $0.18 \mu \mathrm{~m}$ techno <br> \& 1.8 V voltage <br> \& continuous operatio |  |  |  |  | 2-sided ladder <br> switch. not-swi. total |  |  | whole detector switch. not-swi. total |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| inner layer | power (V) | 1,575 | 025 | 1,6 | 18,9 | 0,3 | 19,2 | 8 W | 2 W | W |
|  | current (A) | 0,875 | 0,014 | 0,89 | 10,5 | 0,1 | 10,6 |  |  |  |
| ter | power (W) | 0,490 | 0,010 | 0,5 | 88 | 0,1 | 6 | 382 A | A | 90 A |
| Layers | current (A) | 0,272 | 0,006 | 0,28 | 3,27 | 0,07 | 3,33 |  |  |  |

Average power (integrating pulsing) 20 to 30 W
$\rightarrow$ Air cooling probably good enough


## Area 1: sensor integration

## Cable structure

$x \quad 2$ metal layers in polyimide ( 1 to $2 \times 15 \mathrm{~cm}^{2}$ ) +6 sensors $\rightarrow$ weight $\leq 5 \mathrm{~g}$
$x$ Current $\leq 5 \mathrm{~A} /$ cable $\rightarrow$ typical section for each aluminum power trace: $10 \mu \mathrm{~m} x \geq 2 \mathrm{~mm}$
$\rightarrow$ limit the voltage drop to about 0.1 V over 15 cm
$\rightarrow$ ~ $5 \%$ additional power dissipated
x Parallel powering assumed so far
$\boldsymbol{x}$ Could include DC-DC converter chip at cable end \& regulators inside sensor
$\rightarrow$ Material budget and heat cost?

$\rightarrow$ Under
development within
the PLUME project:
DESY + IPHC +
U.Bristol + U.Oxford


This structure weight 0.6 \% of X0 (2010)

Target for 2011: 0.3\%

## Area 1: power pulsing

## Wire bonds

$x \quad$ Average current through powering wires $\sim 10 \mathrm{~mA}$
$\rightarrow$ Small residual force in $B=4 T$ but vibrations possible
x Monolithic sensors are easy to handle
$\rightarrow$ Possibility to embed in polyimide \& connect through metallization
$\rightarrow$ IMEC+CMST \& CERN projects

## Lorentz force on low mass cable

x Many "small" transverse traces
$\rightarrow$ Residual force could reach few $\mathrm{g} \approx$ cable mass!
$x \quad$ Double-sided structure could be used to counter-balance the effect
$\rightarrow$ Cable design with reverse current path on each side
$x \quad$ Switching sensors with some delay and not simultaneously $\rightarrow$ reduce current
$\rightarrow$ Require specific sensor functionalities

## Area 2: intermediate cables

## - Cables

$x$ Length $\leq 10 \mathrm{~cm}$
x Low mass still required to preserve forward region
$\rightarrow$ Metal = aluminum
$\rightarrow$ Metal thickness limited
x Current @ 1.8 V: 5 to 10 A / ladder
$\rightarrow$ One cable may serve several ladder, current >10 A ?
$\boldsymbol{\rightarrow} \leq 40$ such cables on each side of the VXD
$x$ Higher voltage transport highly desirable
$\rightarrow$ Require DC-DC converters at ladder end

## Lorentz force

$x \quad$ Several Amps at switching on, transverse to B
$\rightarrow$ Lateral forces
$x$ Run along beryllium disk support structure
$\rightarrow$ Cables could be fixed
x Material budget
$x \quad$ Power dissipated in cable
$x$ Voltage drop


## - Optimization to be done for conductor sizing

## Area 3: power transport cables

## Cable type

$x \quad$ Still inside the detector but not in fiducial volume $\rightarrow$ copper allowed
x Weighting against \& heating the beam pipe

- Nominal voltage power transport
$x$ At 1.8 V: current to transport in activity is $\sim 400 \mathrm{~A}$ (otherwise $\leq 10 \mathrm{~A}$ )
$x$ Requiring a voltage drop $<0.1 \mathrm{~V} \rightarrow$ section of conductor $\sim 0.8 \mathrm{~cm}^{2}$
$x$ Total weight $\sim 7 \mathrm{~kg}$
$x \quad$ Power dissipated in conductors 40 W (with duty cycle 1/100 to 1/50)
$\rightarrow$ Small compared to 700 W
- Higher voltage power transport
$x$ Both weight and power dissipated decrease linearly with voltage
- Pulsing
$x$ Longitudinal cable / B field $\rightarrow$ no Lorentz force
$x$ How fast can we switch on/off many Amps on 4 meters?

Technical solutions still to investigate:

- power supplies
- cables with high rise time if no DC-DC converters


## Summary

- The CMOS sensor based ILD vertex detector
$x$ is a 1000 sensors detector
$x$ dissipates $\sim 700 \mathrm{~W}(\sim 400 \mathrm{~A})$ during train
$x$ dissipates 20 to 30 W in average with power pulsing
- Power distribution
$x$ studied on the ladder through dedicated R\&D (PLUME project)
$x$ will benefit from DC-DC converters but not quantitatively estimated yet
x No safety/failure analysis yet
- Power pulsing
x Absolutely necessary for material budget (through cooling)
$x \quad$ Largely not yet experimented with prototypes
$\rightarrow$ Starting with sensors
$\rightarrow$ Some material ready for low mass cabels
$x \quad$ Potential mechanical issues need setup with large B field

