CALICE calorimeters
Power Issues

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« Linear Collider Power Distribution and Pulsing workshop »

May 2011, LAL

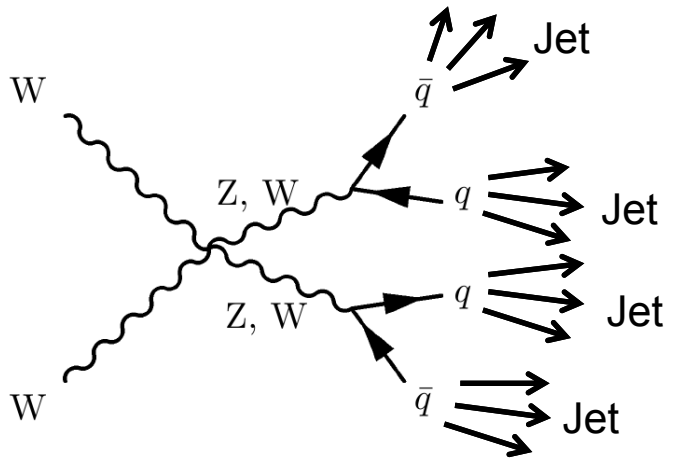
Outline

- Intro
- Calice calorimeters overview
- Power dissipation issues:
  - Power pulsing mechanism tested on SDHCAL
  - Active cooling test bench for Si-W ECAL
- Conclusion

Hadronic decay of W and Z bosons

Jet energy resolution will be a key feature in the analysis of multijet final state events:

Exemples:
→Trilinear Higgs self coupling measurement
→WW scattering measurement in absence of Higgs

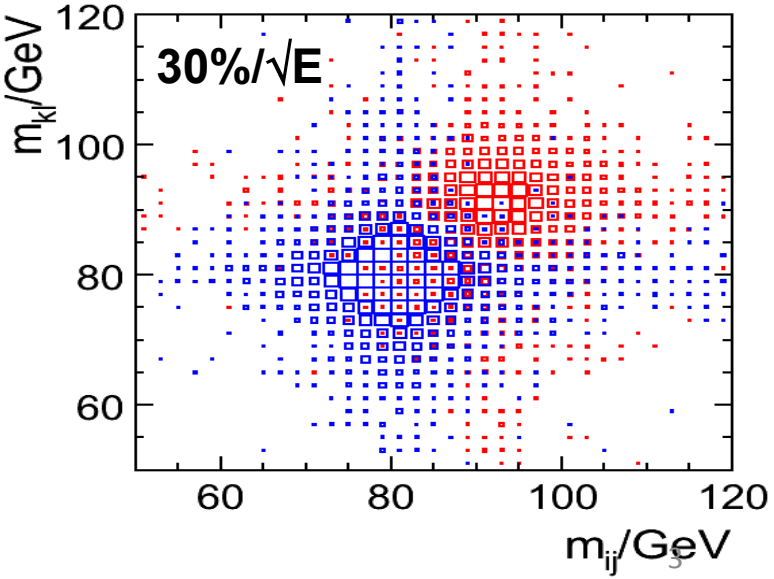


The separation capability of W and Z is mainly driven by the energy resolution.

$$\frac{\sigma_E}{E} = \frac{21}{\sqrt{E}} \oplus 0.7 \oplus 0.004E \oplus 2.1 \left(\frac{E}{100}\right)^{+0.3} \%$$

Resolution | Tracking | Leakage | Confusion

Remember: M_Z-M_W ≈ 10 GeV



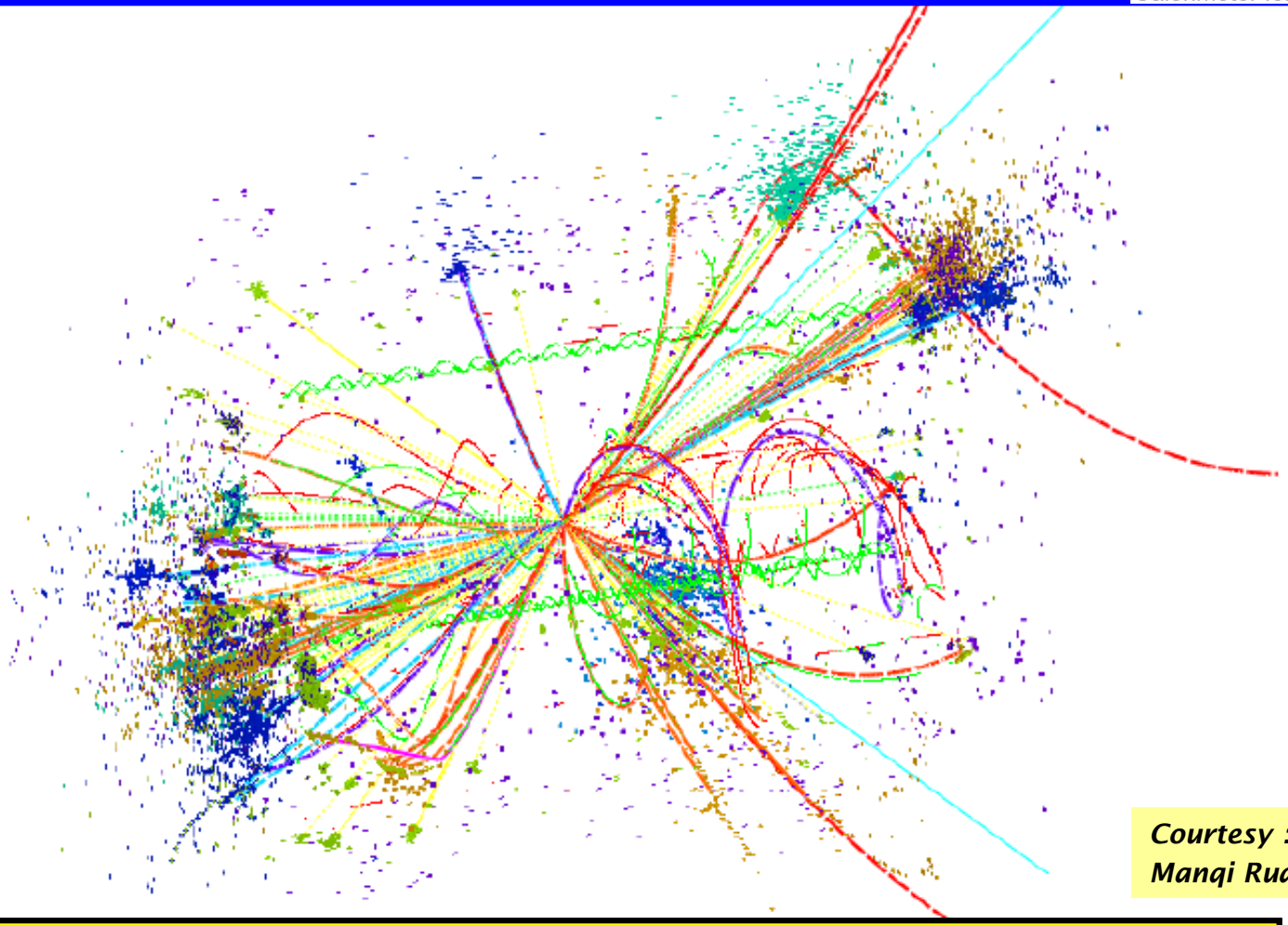
Calorimeter R&D for a future linear collider

Collaboration is:

More than 330 physicists/engineers from 57 institutes and 17 countries from 4 continents, working on different technologies of electromagnetic and hadronic calorimeters .

It aims at developing highly granular calorimeter to be used for future linear colliders but not only.

Highly granular calorimeters

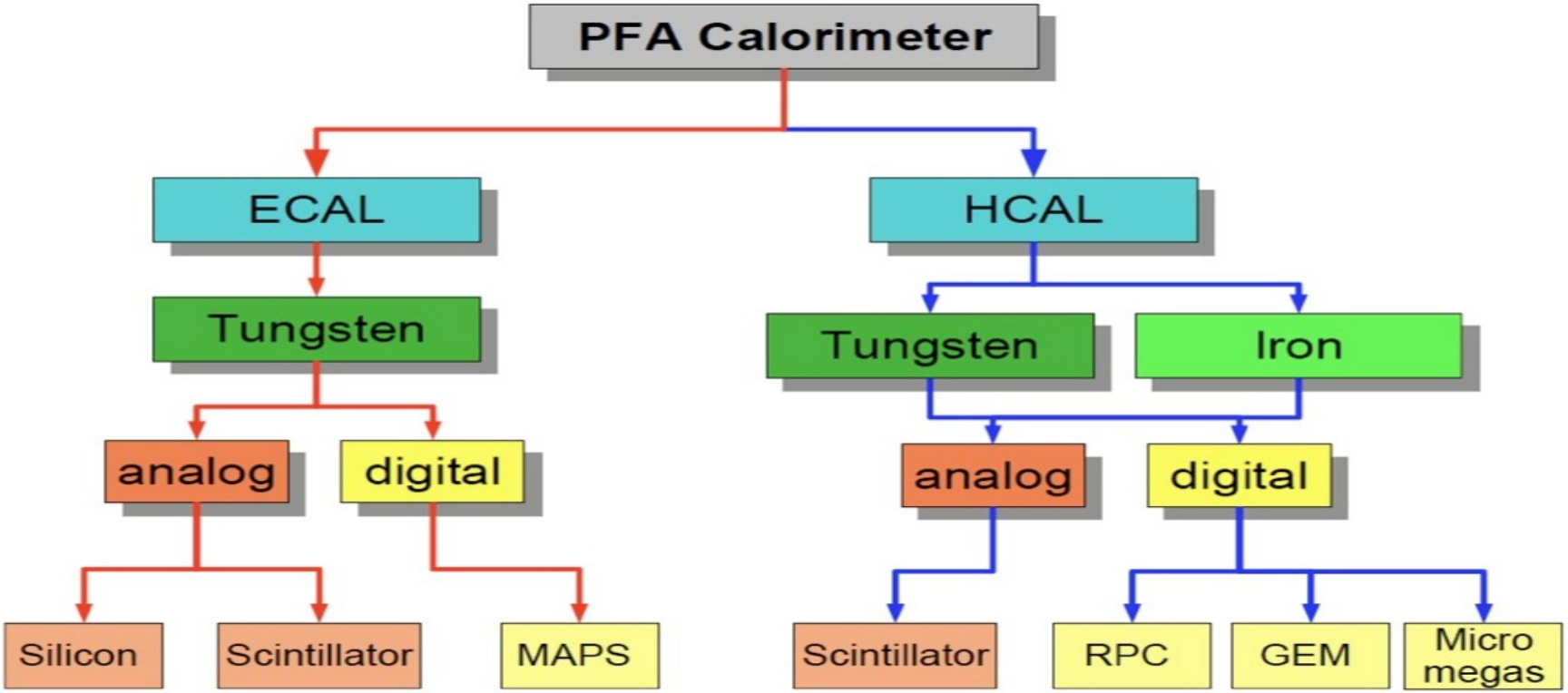


Courtesy :
Manqi Ruan LLR

ttbar event √s=500GeV on DRUID diplay

Calice calorimeters

All Calice calorimeters are designed in order to apply successfully particle flow analysis. Compactness, hermeticity, and high granularity are the key words of this development.

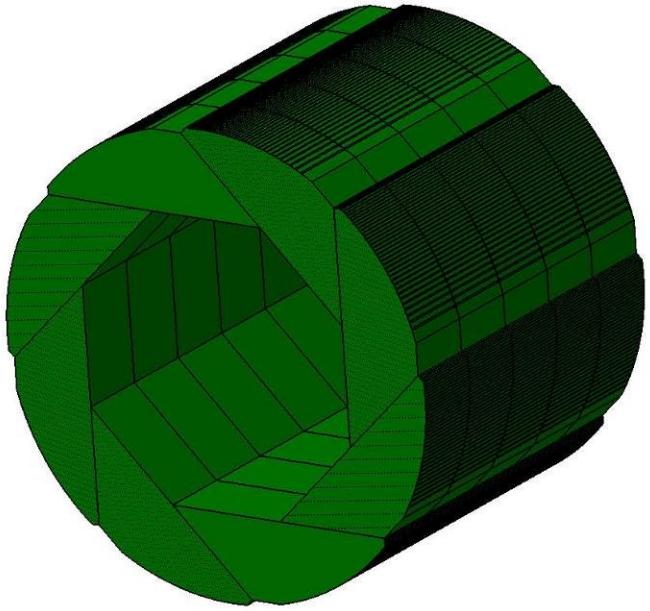


Calice calorimeters

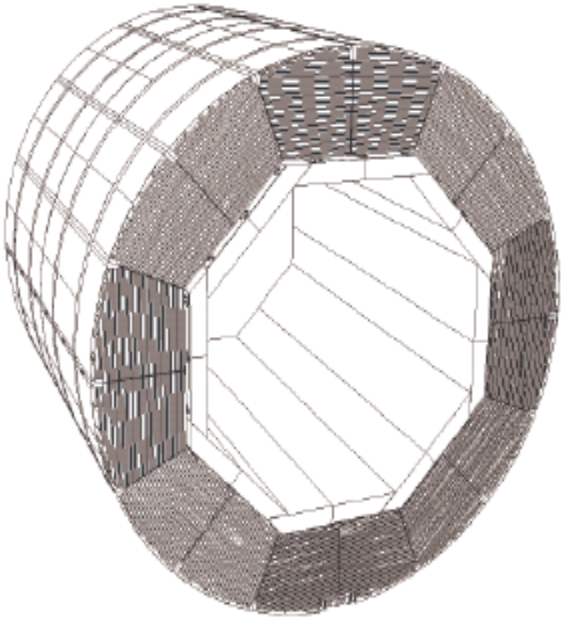
Calorimeter	Sensitive Medium	Absorber	Granularity	Number of Channels	Readout Chip	Consumption (PowerPulsed)
Si-W ECAL (ILD oriented)	Silicon Diodes	Tungsten	0.5x0.5 cm^2	≈100M	SKIROC	25µW/ch Tot: ≈2500W
Si-W ECAL (SiD oriented)	Silicon Diodes	Tungsten	0.13 cm^2	≈73M	KPiX	<20µW/ch Tot: <1460W
Scint-W ECAL (ILD oriented)	Scin. Tiles + SiPM	Tungsten	0.5 x 4.5 cm^2	≈11M	SPIROC	(25+7)µW/ch Tot: ≈352W
AHCAL	Scin. Tiles + SiPM	Iron	3x3 cm^2	≈8M	SPIROC	(25+15)µW/ch Tot: ≈320W
SDHCAL (ILD oriented)	GRPC or µMegas	Iron	1x1 cm^2	≈50M	HARDROC	7.5µW/ch Tot: ≈375W
DHCAL	GRPC	Iron	1x1 cm^2	≈50M	DCAL III	<4 mW/ch No Pow. Puls. Tot: <20kW

Geometry of HCALs

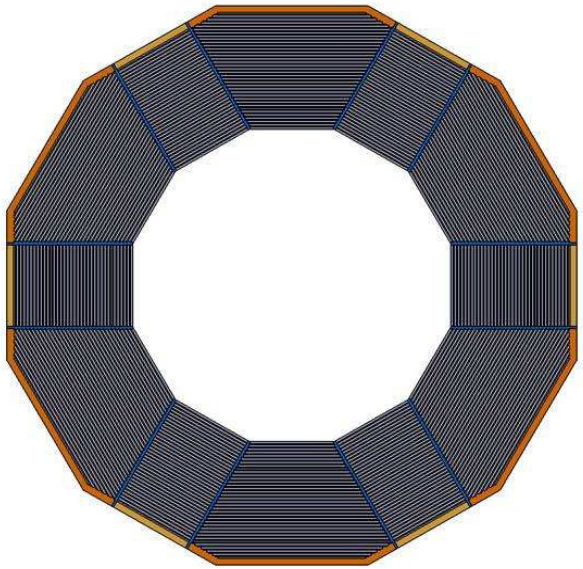
- Different geometries are under consideration to minimize cracks and improve HCALs' hermeticity .
- Absorbers are shaped to make a self-sustained structure.
- The space needed to connect each layer services is also a critical point:
  - Cabling: Power + data + detector interface (DIF)
  - Cooling: Pipes + radiator



ILD-Videau

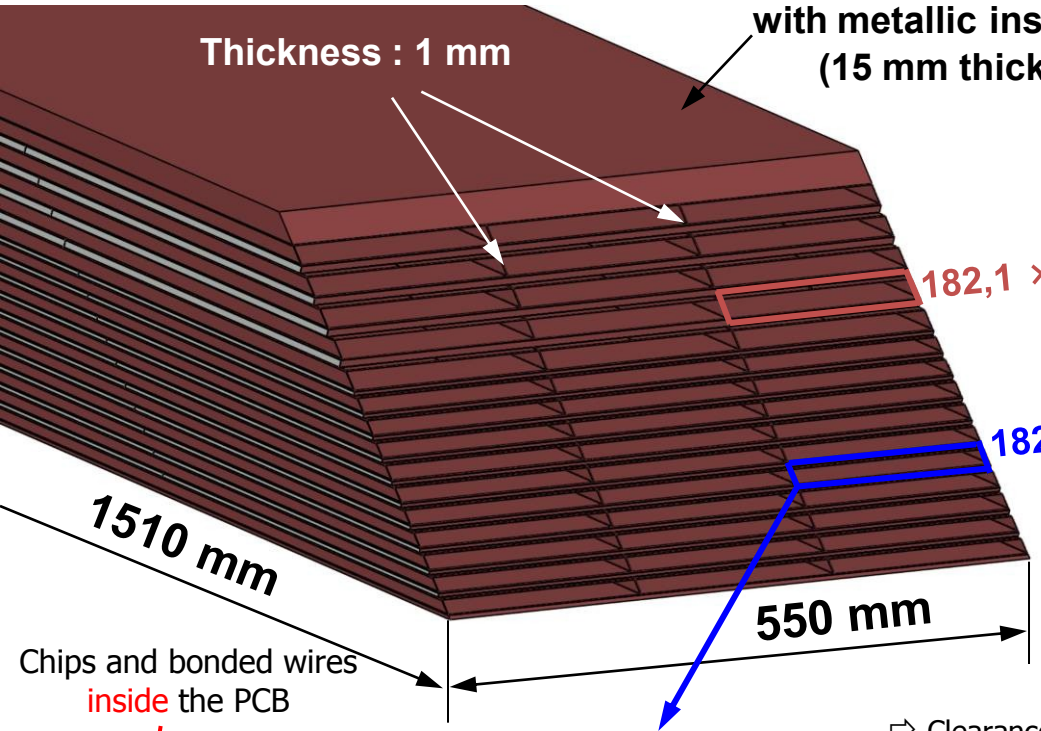


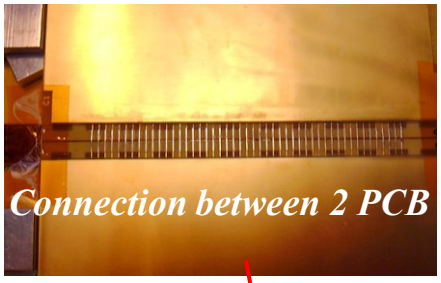
ILD-Baseline

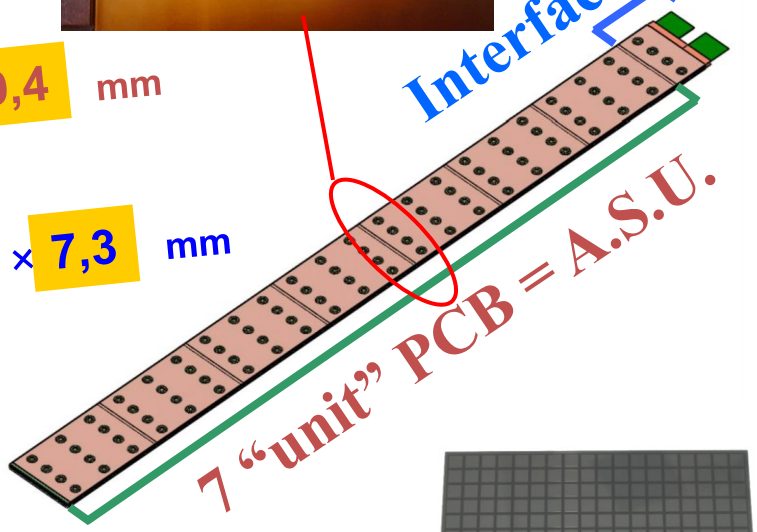


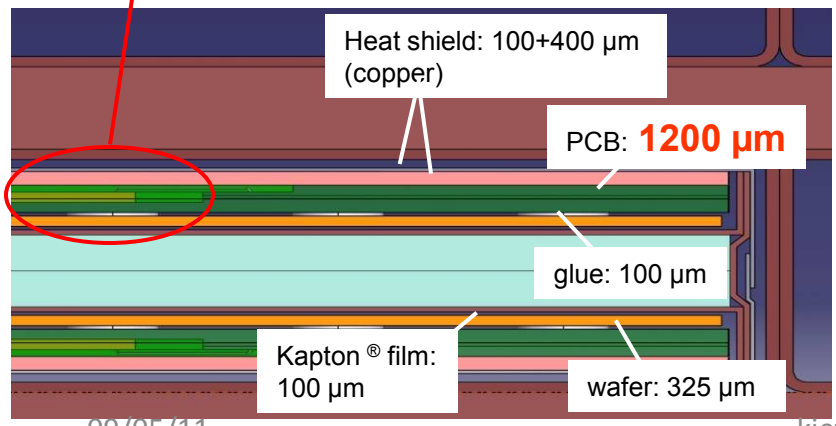
SiD-Baseline

Si-W ECAL (ILD oriented)

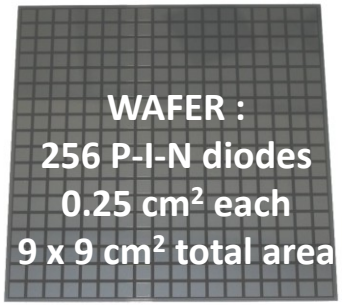








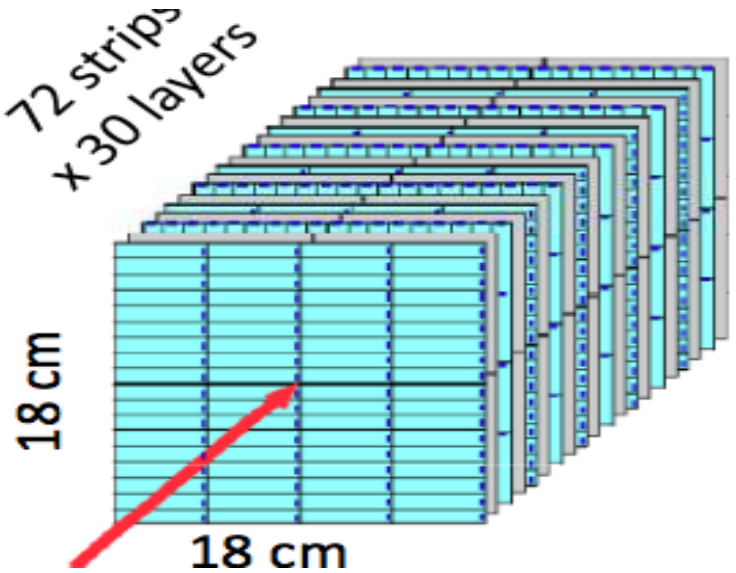
- ⇨ Clearance (slab integration) : 500 µm
- ⇨ Heat shield : **400 µm ?** →
- ⇨ PCB : **1200 µm ?** → design possibilities
- ⇨ Thickness of glue : 100 µm
- ⇨ Thickness of wafer : 325 µm
- ⇨ Kapton® film HV : **100 µm ?** → tests
- ⇨ Thickness of W : 2100/4200 µm (± 80 µm)

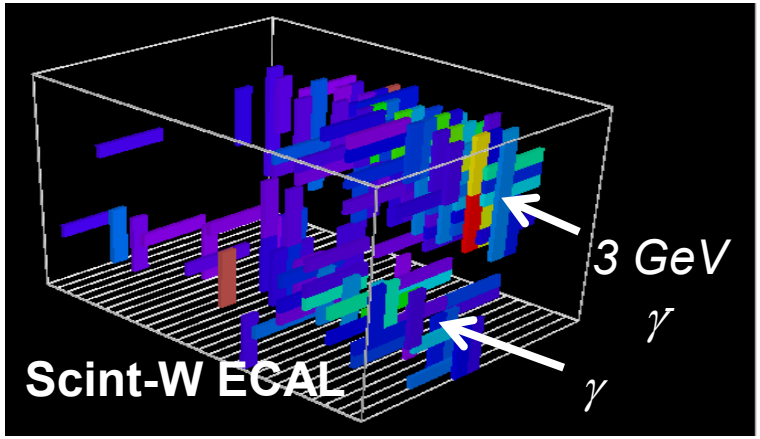


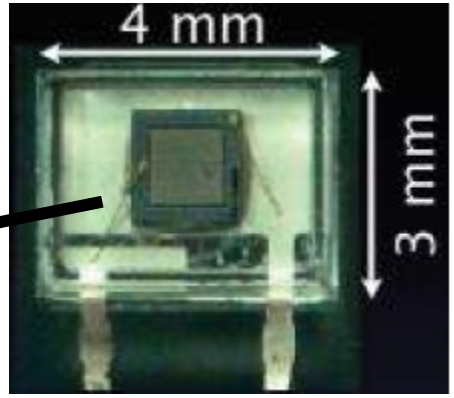
Courtesy :
Marc Anduze - LLR

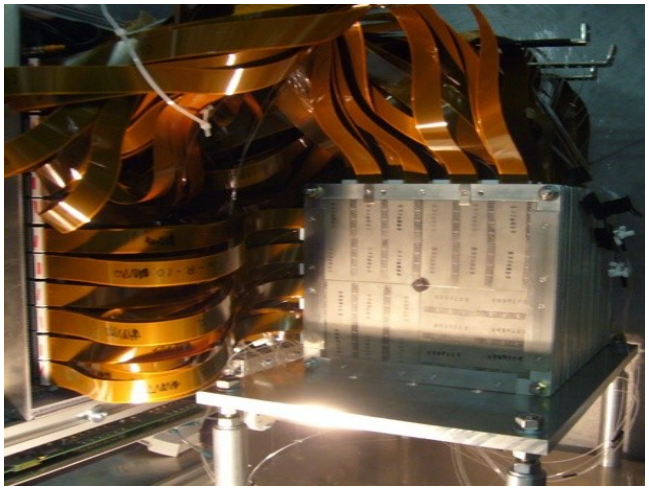
Scint-W ECAL (ILD oriented)

- Sandwich structure with scintillator-strips (3 mm) and tungsten layers (3.5 mm).
- Extruded scintillator with WLS fibers read with the MPPC.
- Strips are orthogonal in alternate layers (X-Y layers).
- 72 strips x 30 layers = 2160 channels



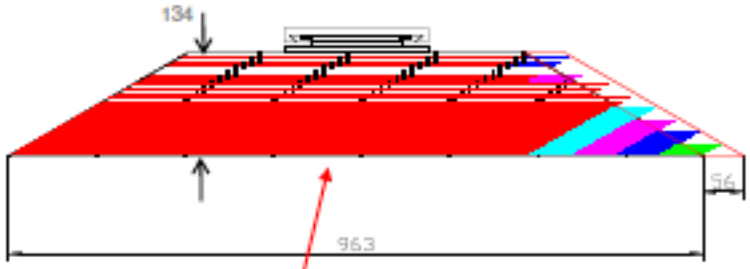


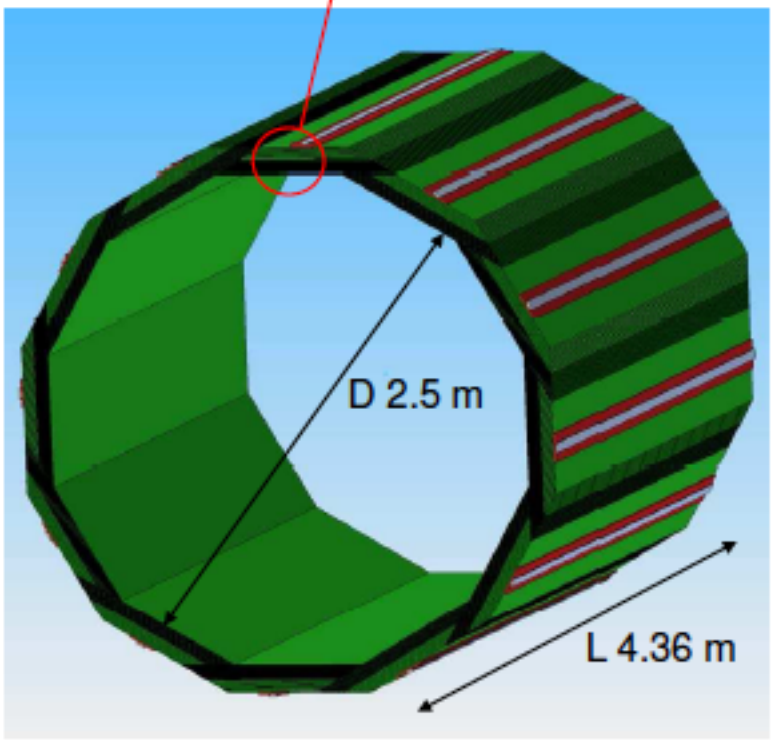


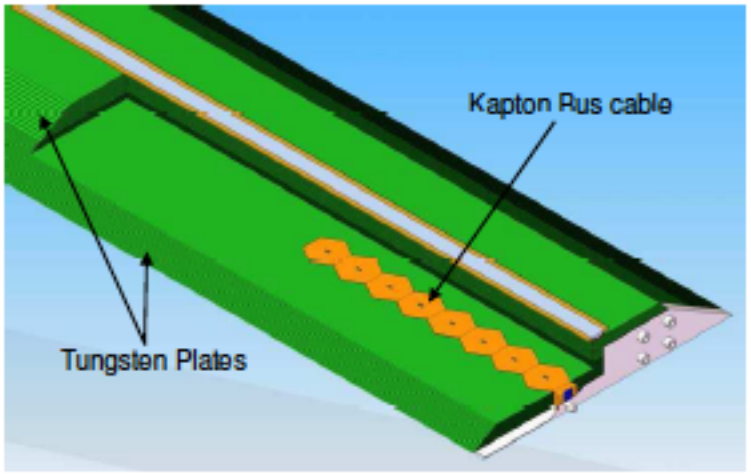


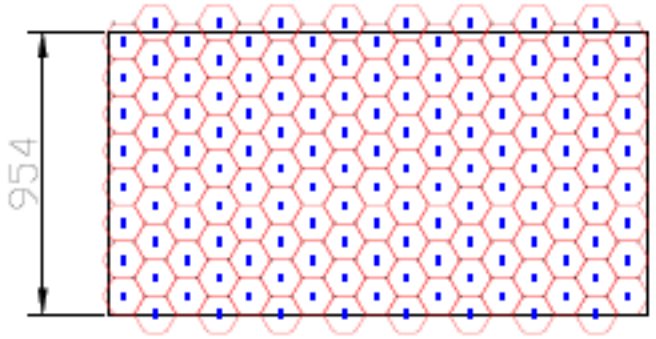
Scint: 4.5 x 1 x 0.2 cm

Si-W ECAL (SiD oriented)

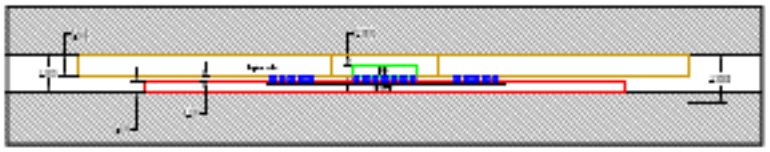






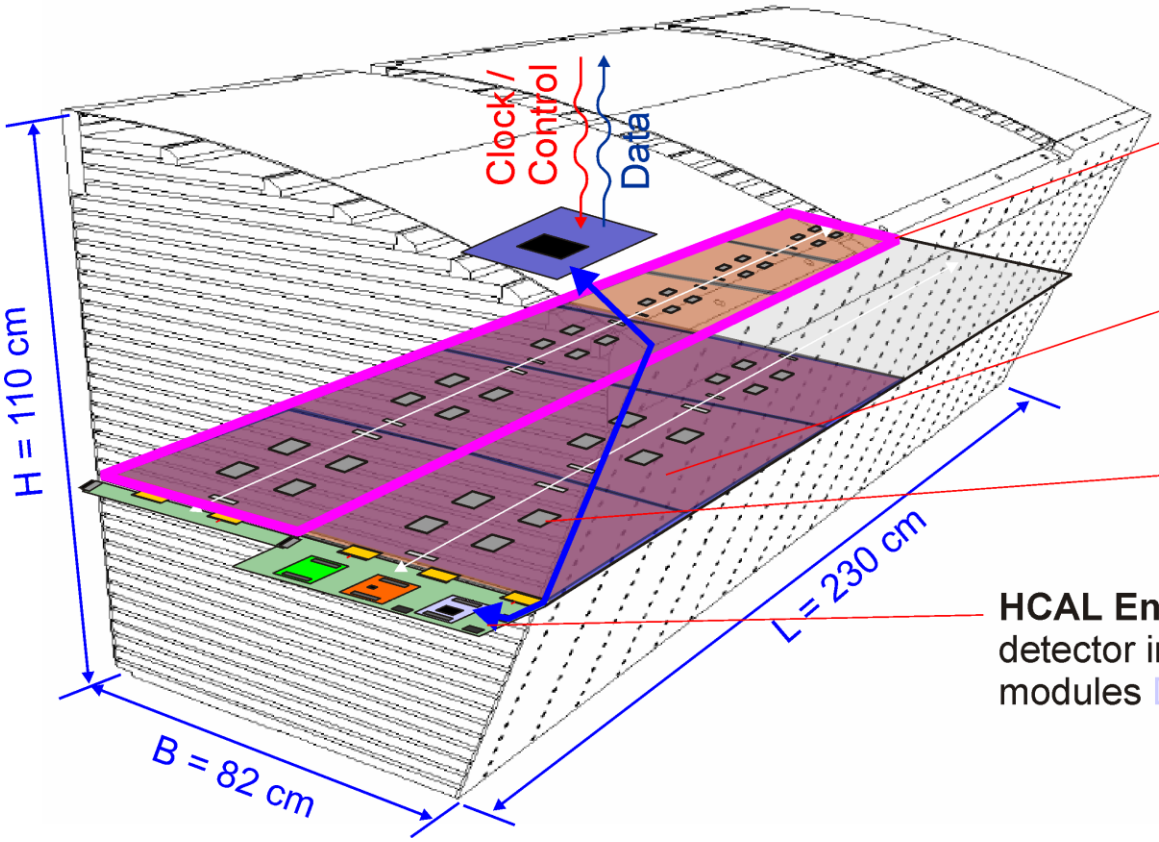


Hexagon sensors arrangement



detector module between tungsten plates

AHCAL (ILD oriented)

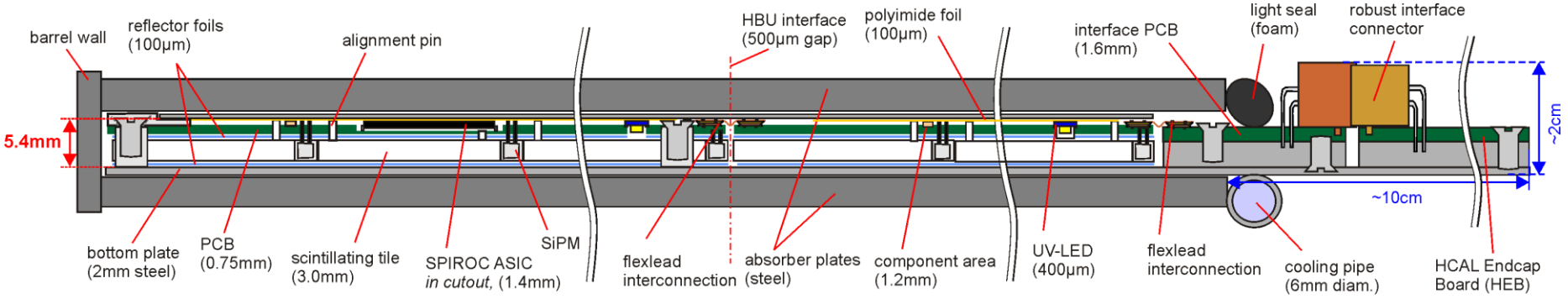


AHCAL slab
electronic layer unit
(6 HBUs in a row)

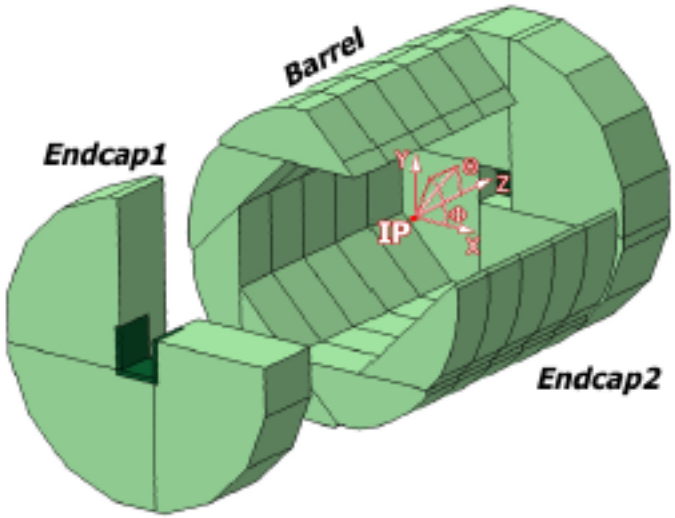
HCAL Base Unit (HBU)
144 detector channels,
4 SPIROCs (ASICs)

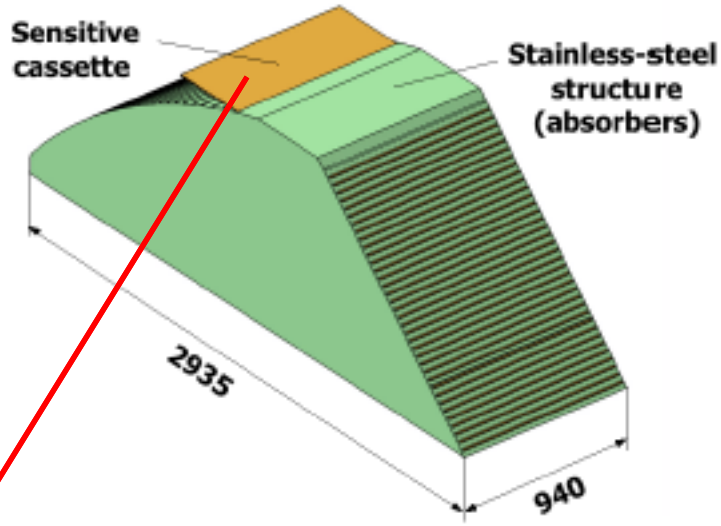
SPIROC (ASIC),
36 detector channels

HCAL Endcap Board (HEB),
detector interface electronics:
modules DIF, CALIB and POWER



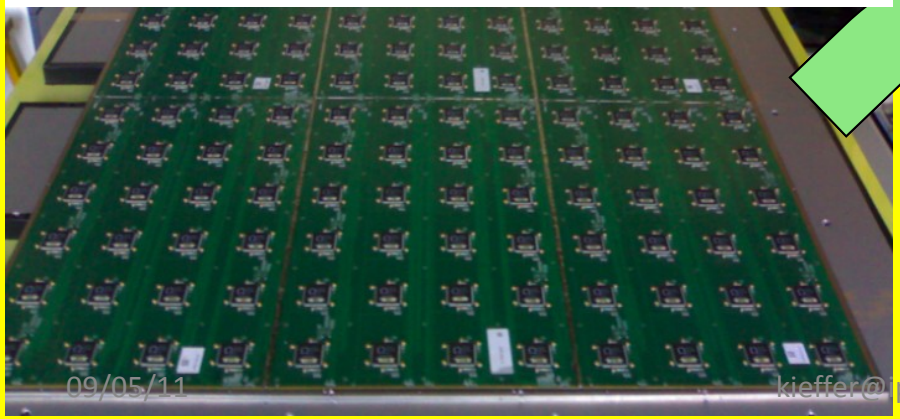
SDHCAL (ILD oriented)





Each **sensitive cassette** contains a **readout board** stick to a **GRPC**

1 m² semi-digital readout HARDROC



1 m² GRPC

DHCAL (SiD oriented)

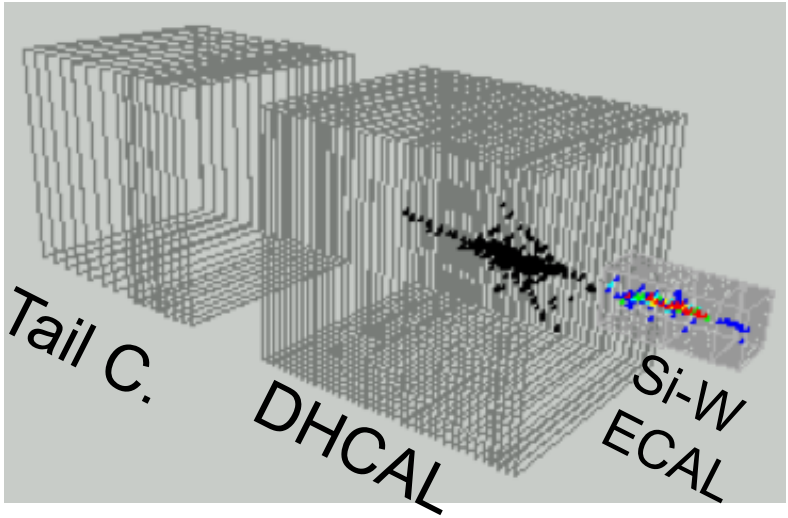
1m^3 physical prototype is currently in testbeam using the mechanical structure of the AHCAL prototype.

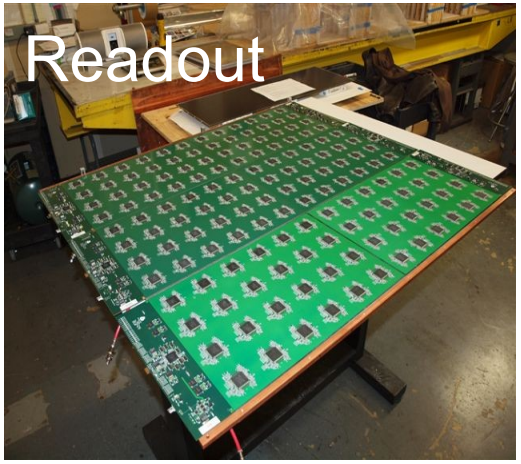
Si-W ECAL prototype is in front, and Tail Catcher on the back.

Detectors production

- 38 active layers each 1 x 1 m^2
  1x1 cm^2 readout pads
  ~10,000 pads per layer

- Embedded electronics
  ~350,000 readout channels in total





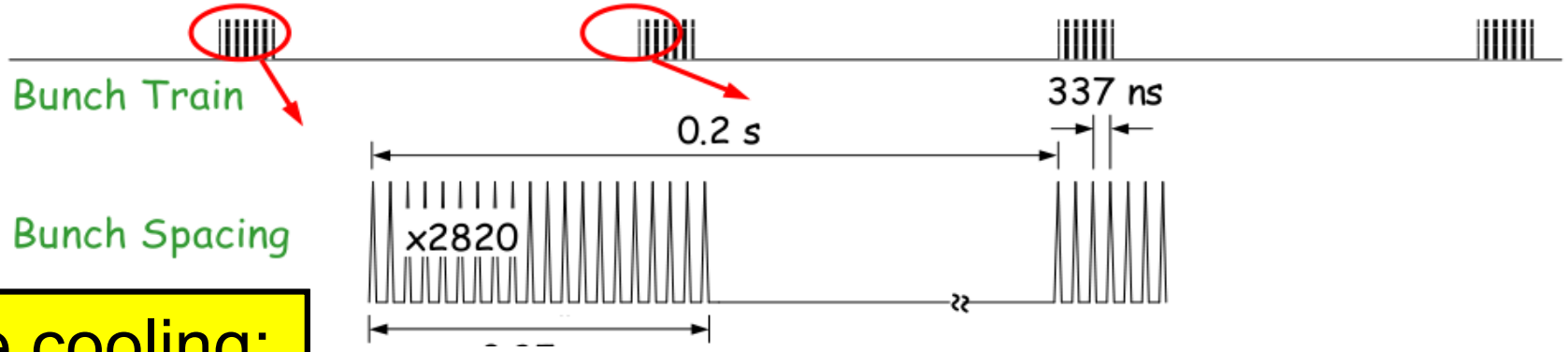
Power Issues

Power issues

Power Pulsing

Within Calice collaboration, most of our very front chip are designed to be powepulsed (see ROC family on N.Seguin-Moreau's talk).

Using this power mechanism in phase with the ILC beam structure, we can reduce the power dissipation by a factor >100.



Active cooling:

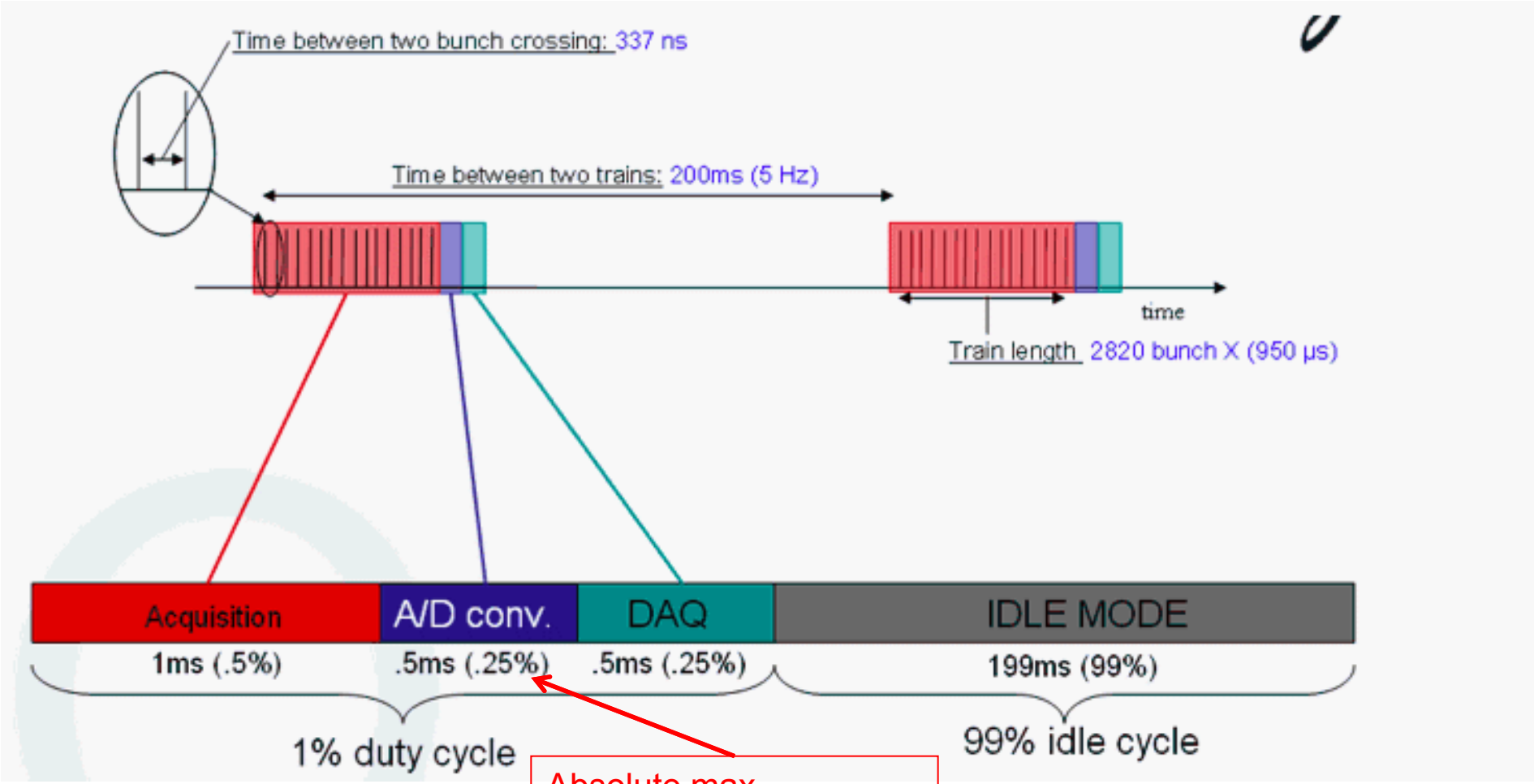
We intend to minimise the use of active cooling because of its impact on material budget.

- Nevertheless power pulsing decreases dissipated power but does not extract the remaining part!
- Intermediate cards (DIF+LDA+CCC) hosting FPGAs will also remain permanently powered.

=> A minimum active cooling will be needed.

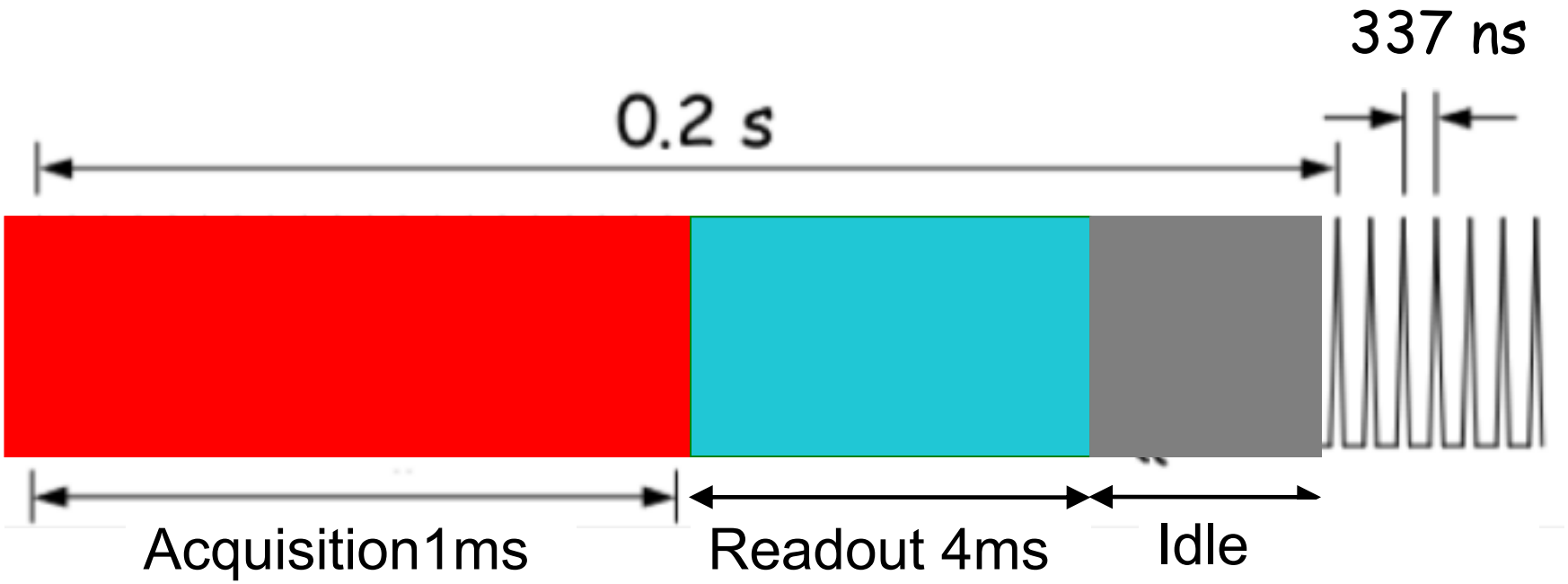
Power Pulsing scheme

The analog readout case: SPIROC & SKIROK



Power Pulsing scheme

The semi-digital readout case: HARDROC



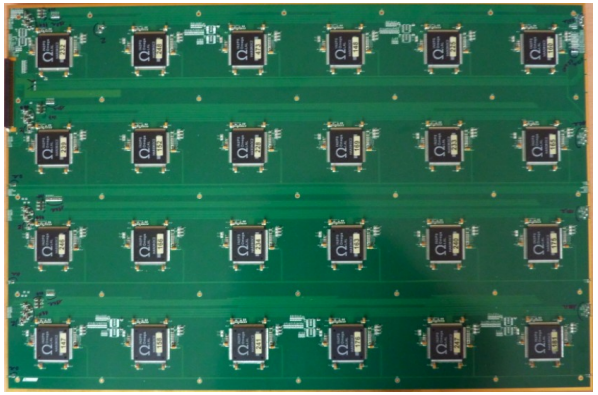
- Maximum readout duration: 4ms if the 127 memory slot of the chip are used.
  ⇒Most of the time shorter.

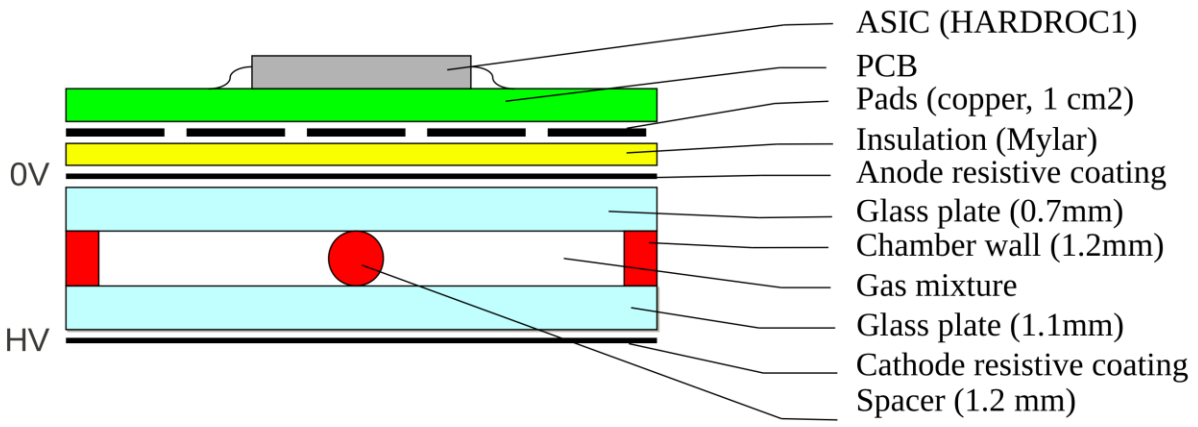
- No analog conversion needed (semi-digital =>3 thresholds).

SDHCAL power pulsing test

The active sensitive unit:

- An electronic board hosting 24 chips connected through a daisy chain scheme is fixed on a 50x33 cm^2 GRPC detector (1536 channels).





- A non-magnetic metallic cassette contains this assembly.

A testbeam under B field

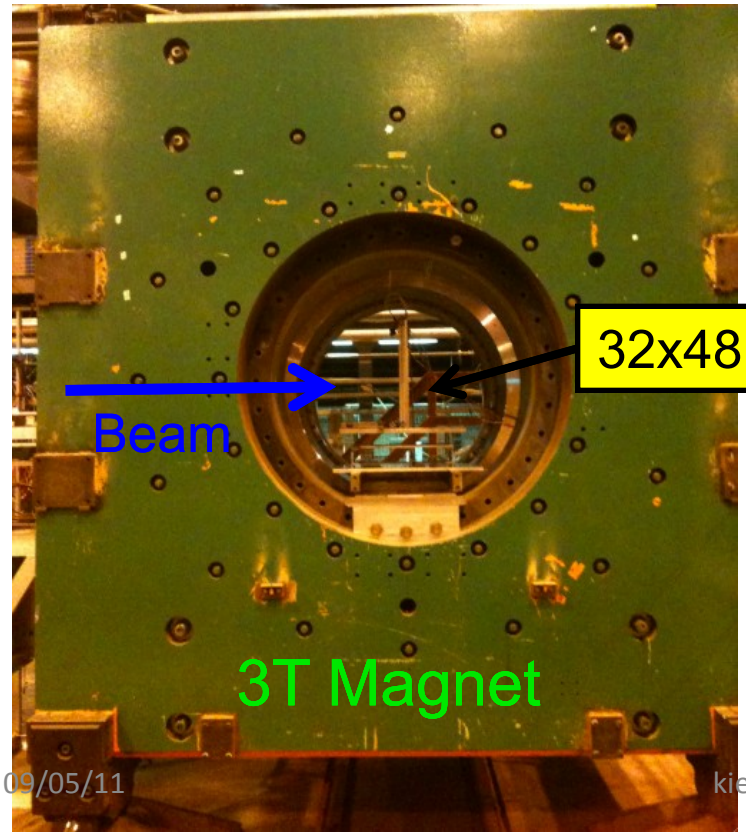
June 2010: 10 days, SPS H2, parasitic operation

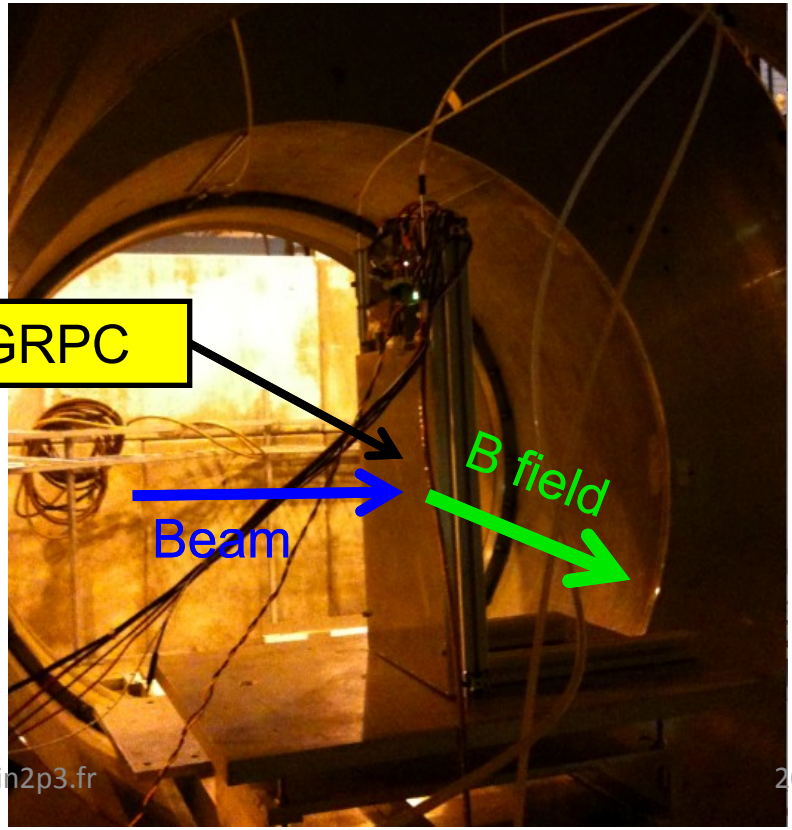
Beam conditions: 80GeV @ High Rate

Aim: PowerPulsing tests using B field.

PowerPulsed events: 42 kEvents

Non-PowerPulsed events: 74 kEvents





Data time structure

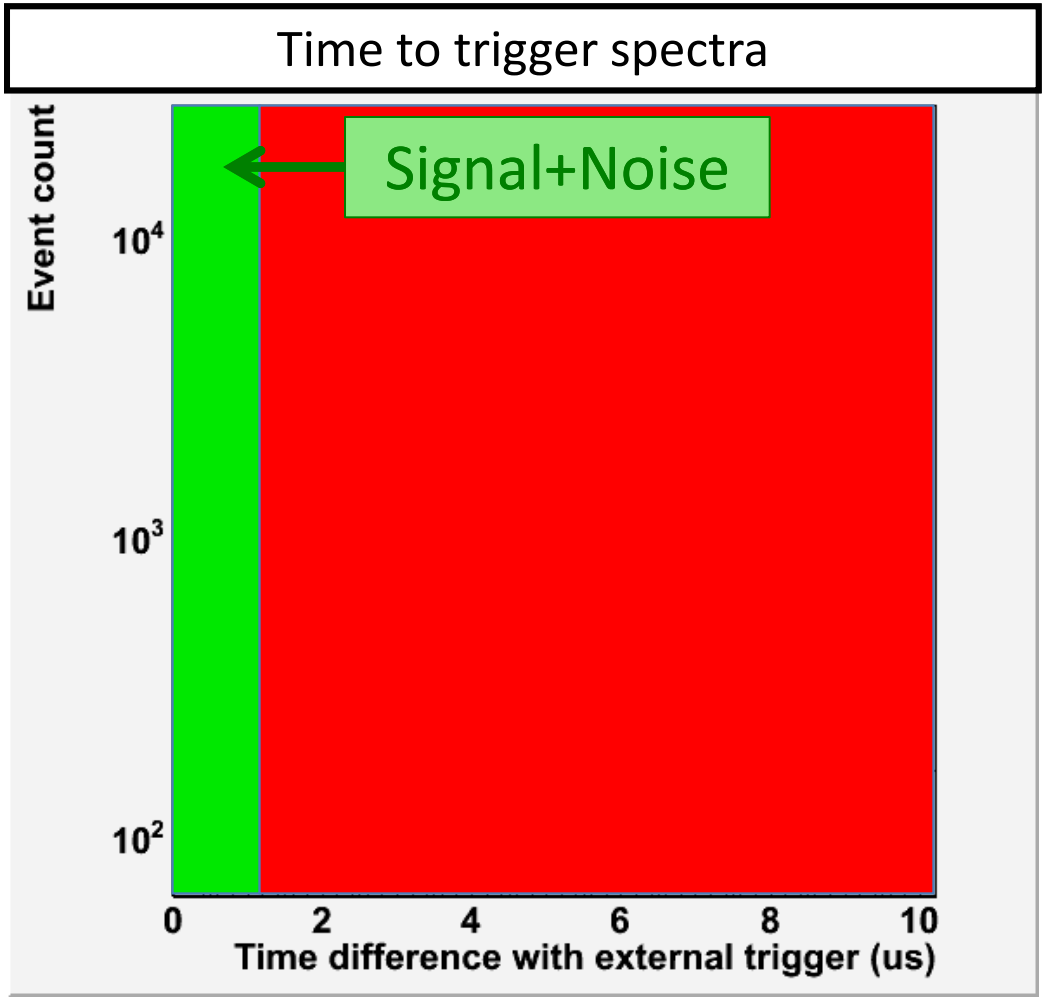
Clock period: 400ns

Time selection for triggered events:

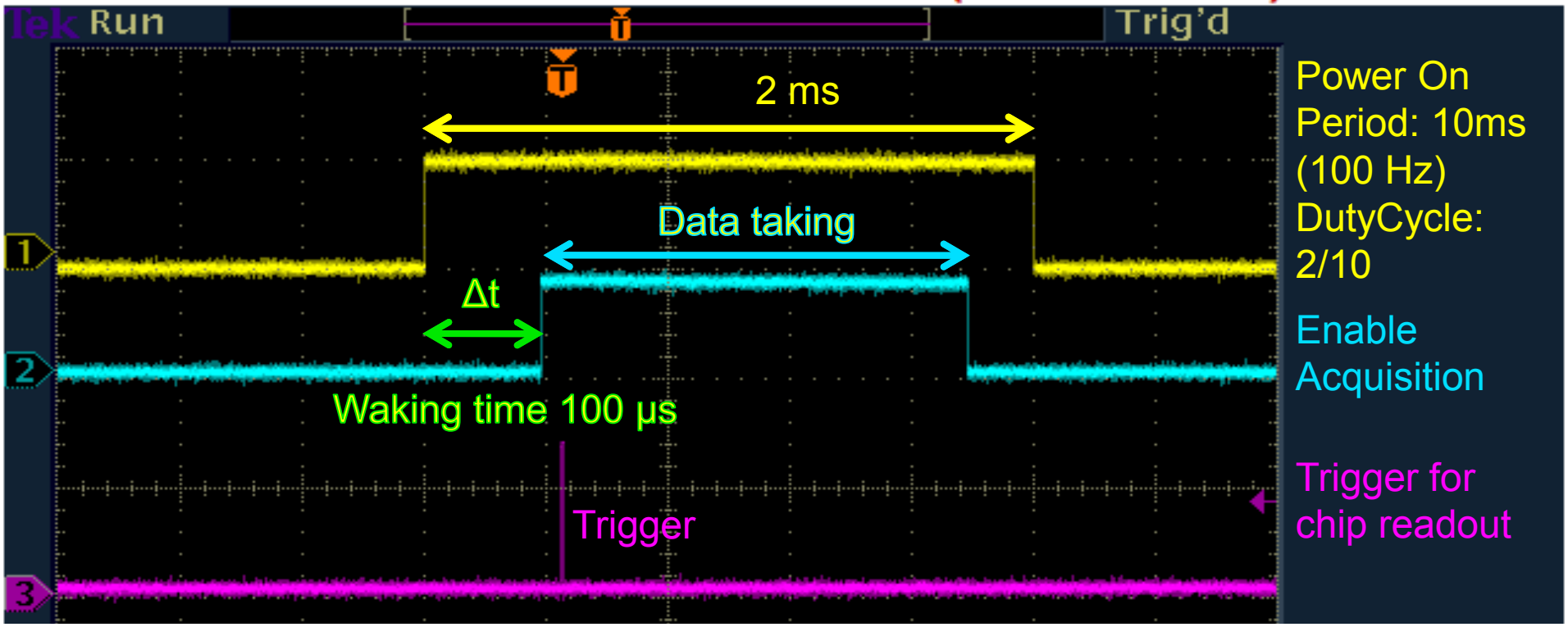
0<EvTime<1.2us

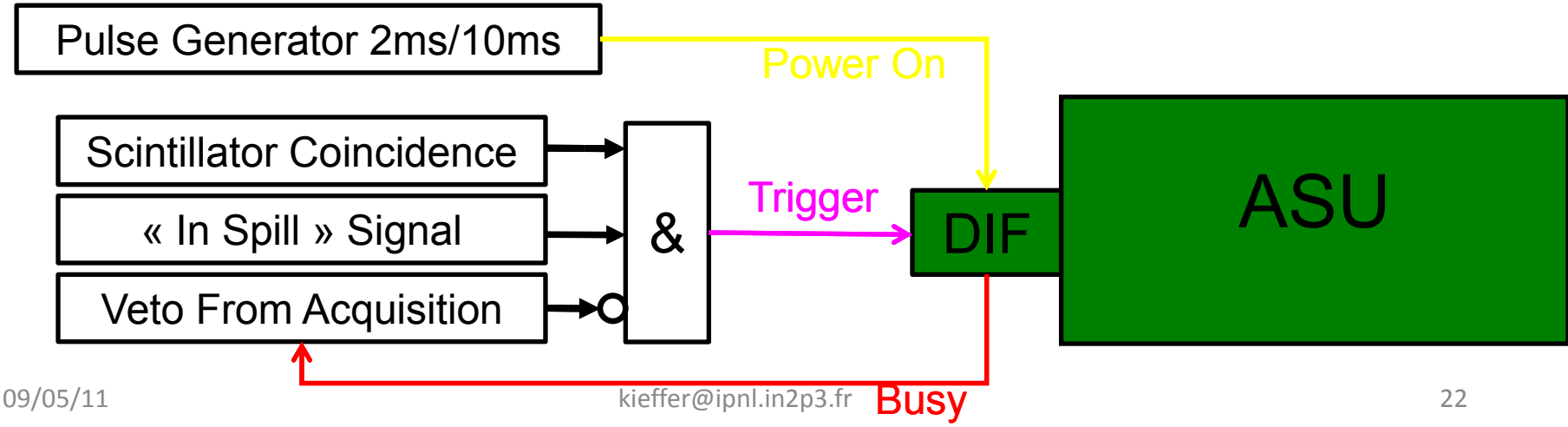
Noise contamination ratio:

1%



Power pulsing cycle



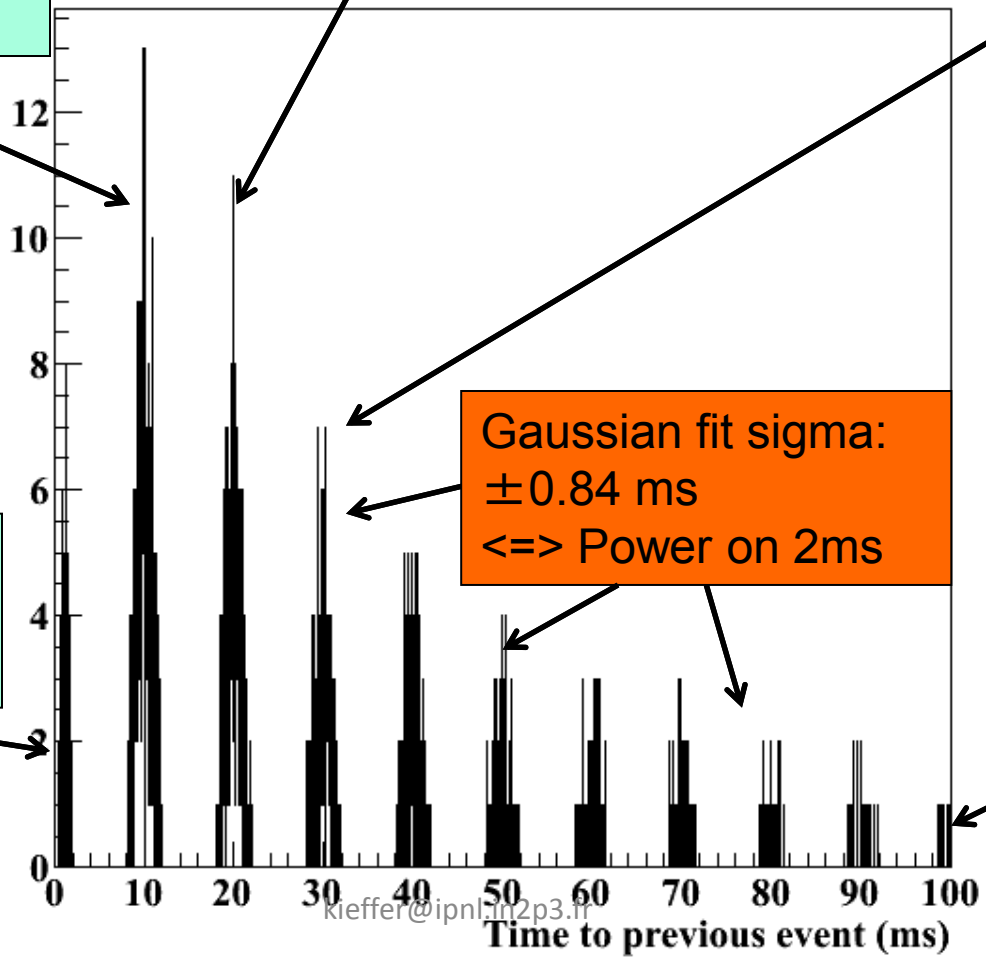


Timing of power cycle in the data

Trigger taken in two consecutive power-cycles (10ms)

One cycle without trigger (20ms)

Two cycles without trigger…

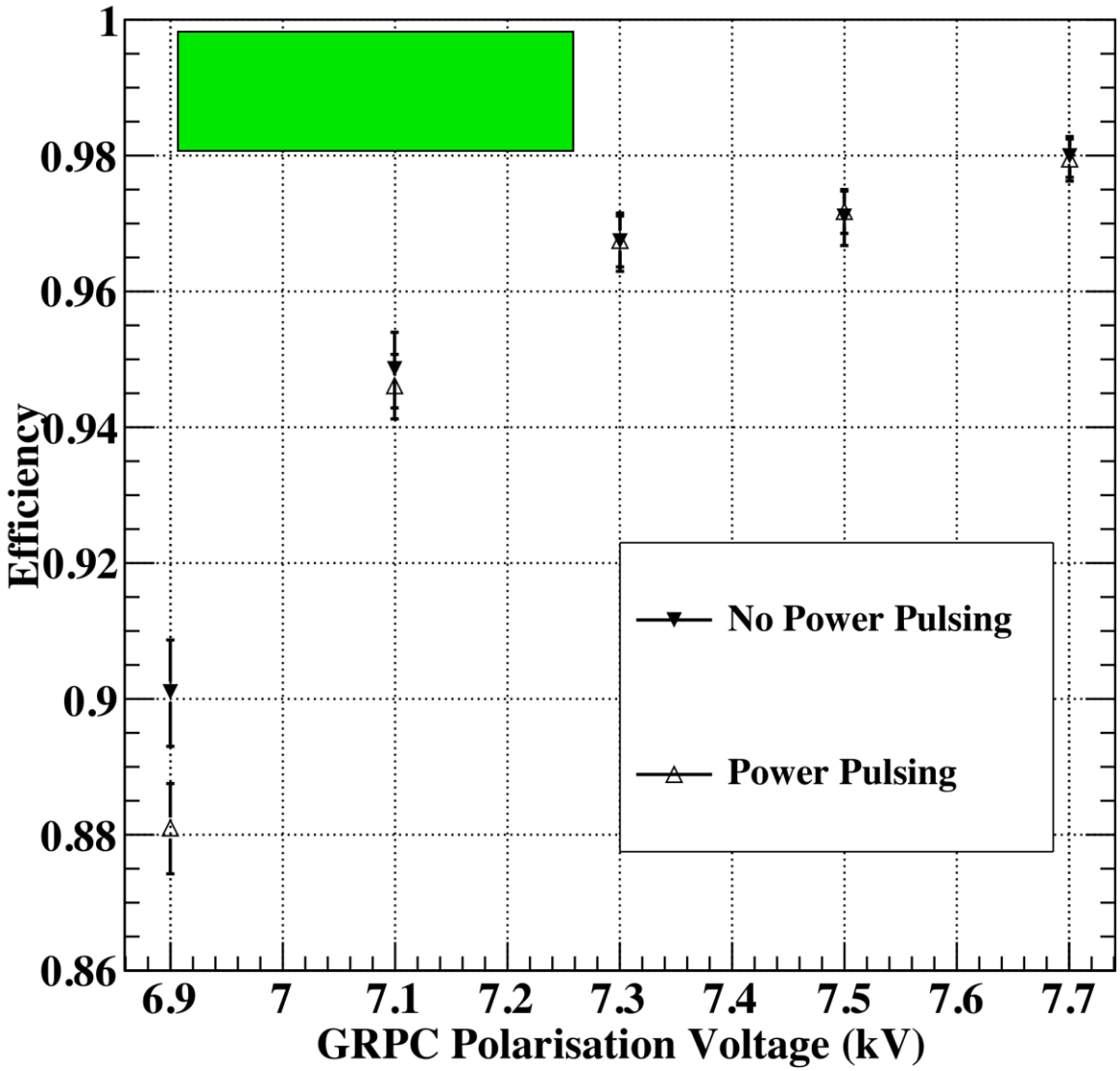


Gaussian fit sigma:
±0.84 ms
<=> Power on 2ms

Trigger taken in the same power-cycle (2ms)

Up to 11 power-cycles acquiring during a spill !!!

Efficiency using Power Pulsing

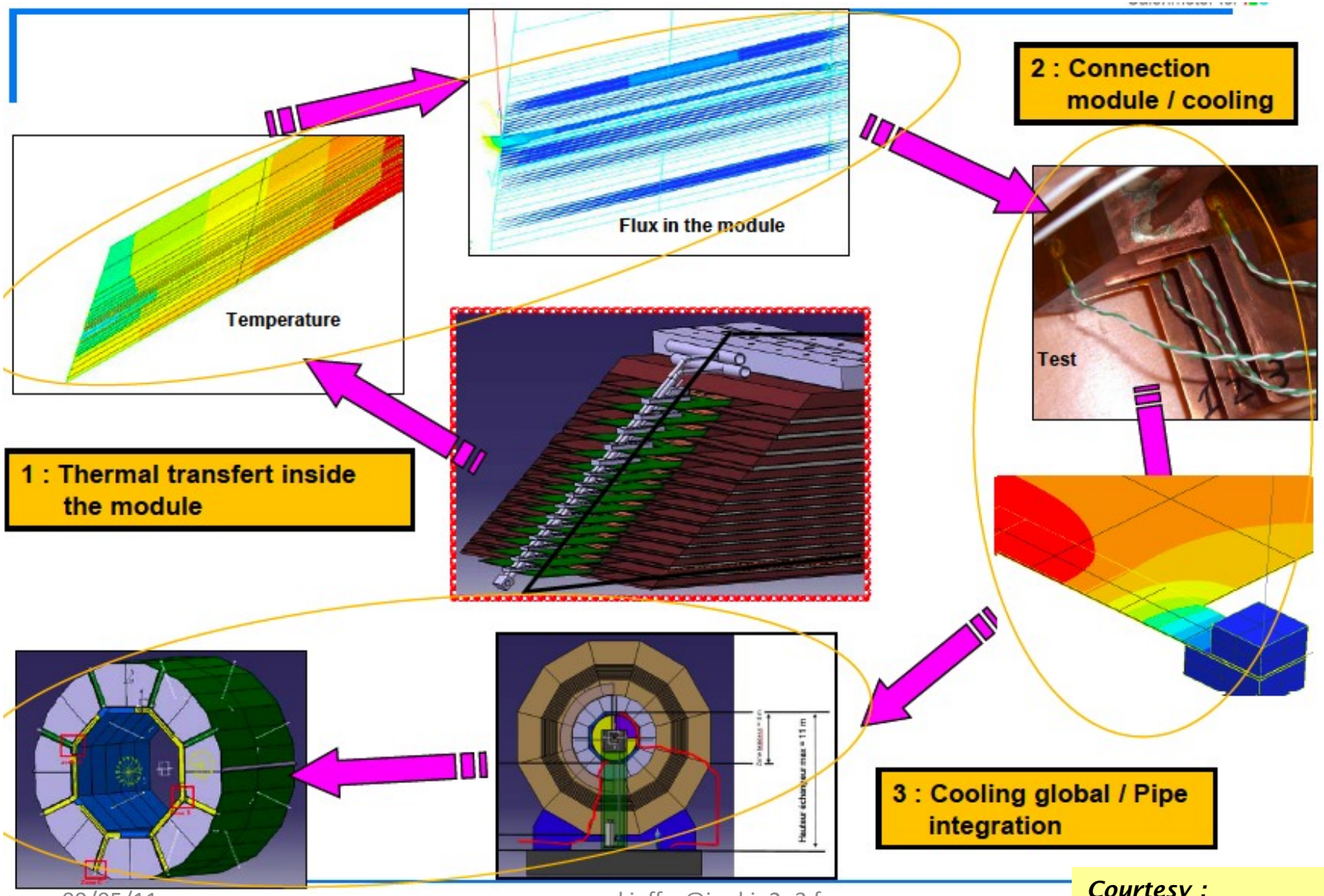


found runing under power pulsing.

Active cooling in Si-W ECAL

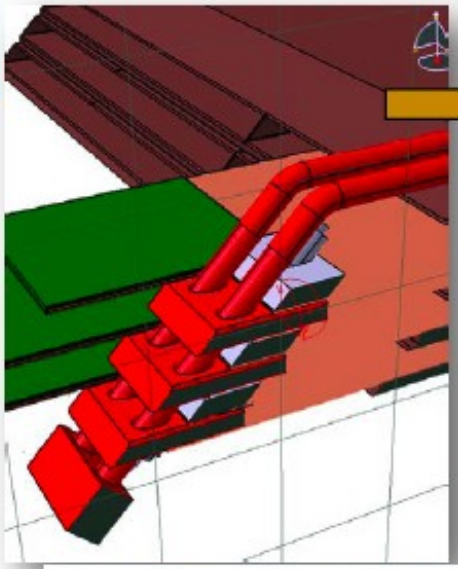
Active cooling in Si-W ECAL

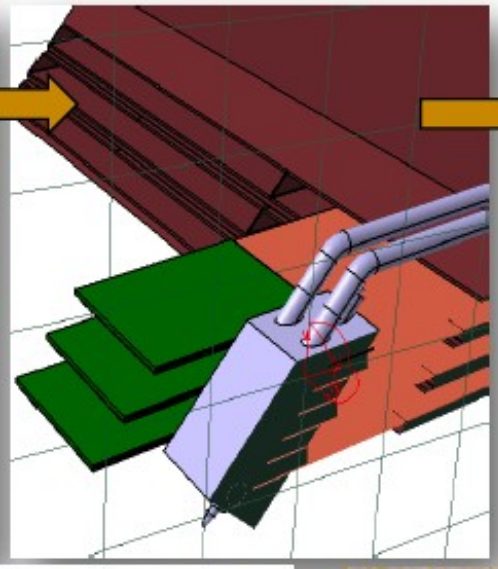
A bench test have been build at LPSC to develop active cooling.

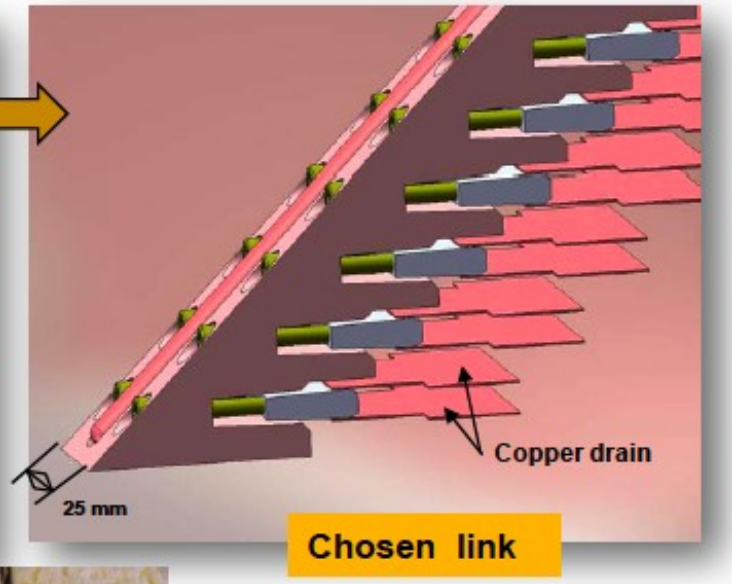


Courtesy : Julien Giraud- LLR

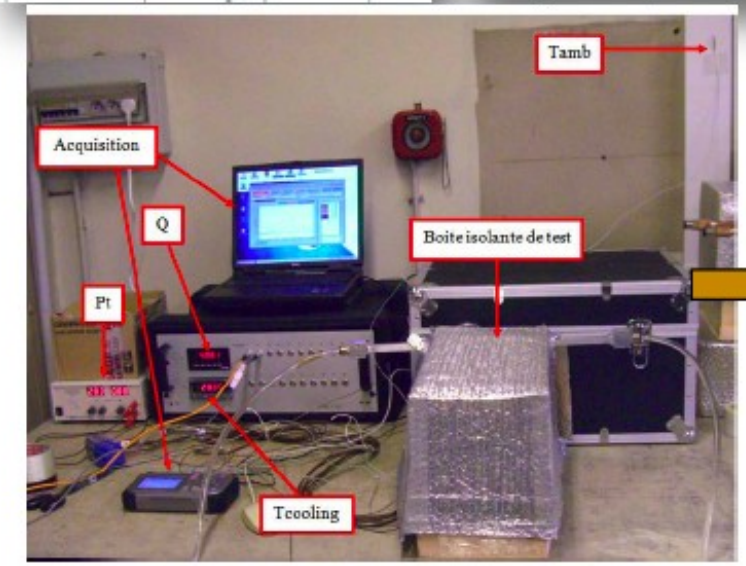
Active cooling in Si-W ECAL

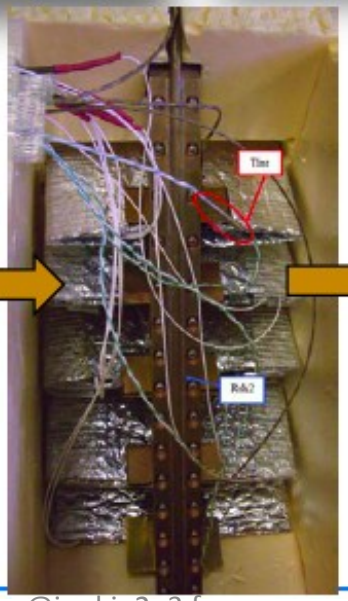




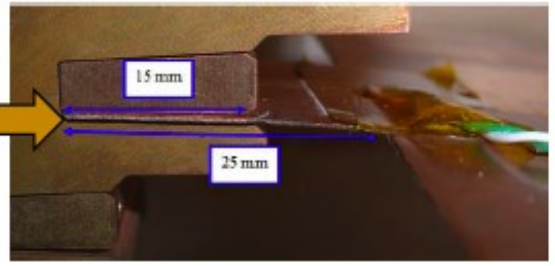


Chosen link





Confirmation: **25 mm** free opening in DIF for extraction of cooling system



Courtesy : Julien-Giraud LLR

Summary

Cooling issues:

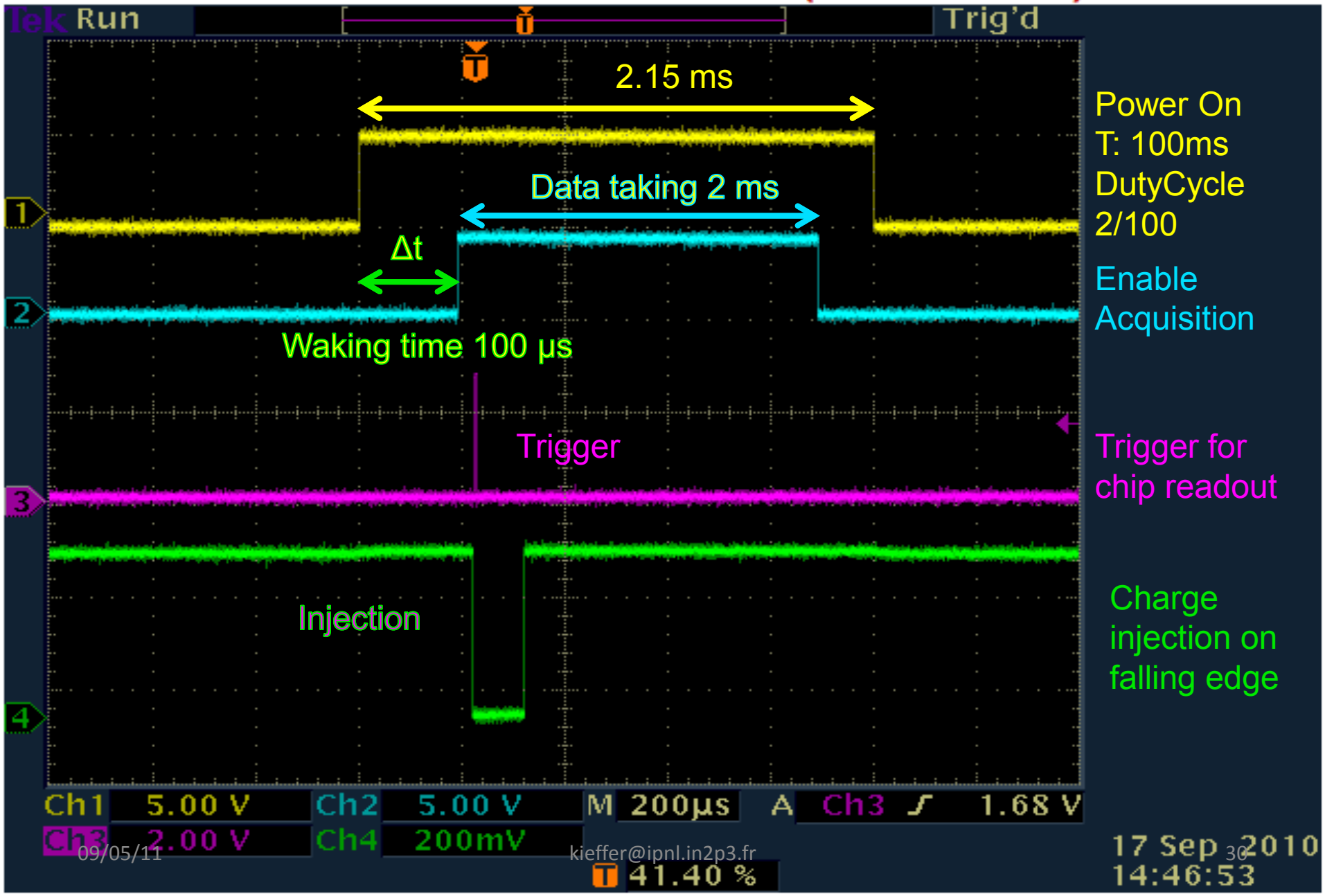
- ✓ Power pulsing scheme validated in testbeam with SDHCAL prototype.
- ✓ Power pulsing also validated on testboard for all ROC chips.
- ✓ Will be tested very soon for all other calorimeters prototypes.
- ✓ Cooling issues results are encouraging.

Calice prototypes' status:

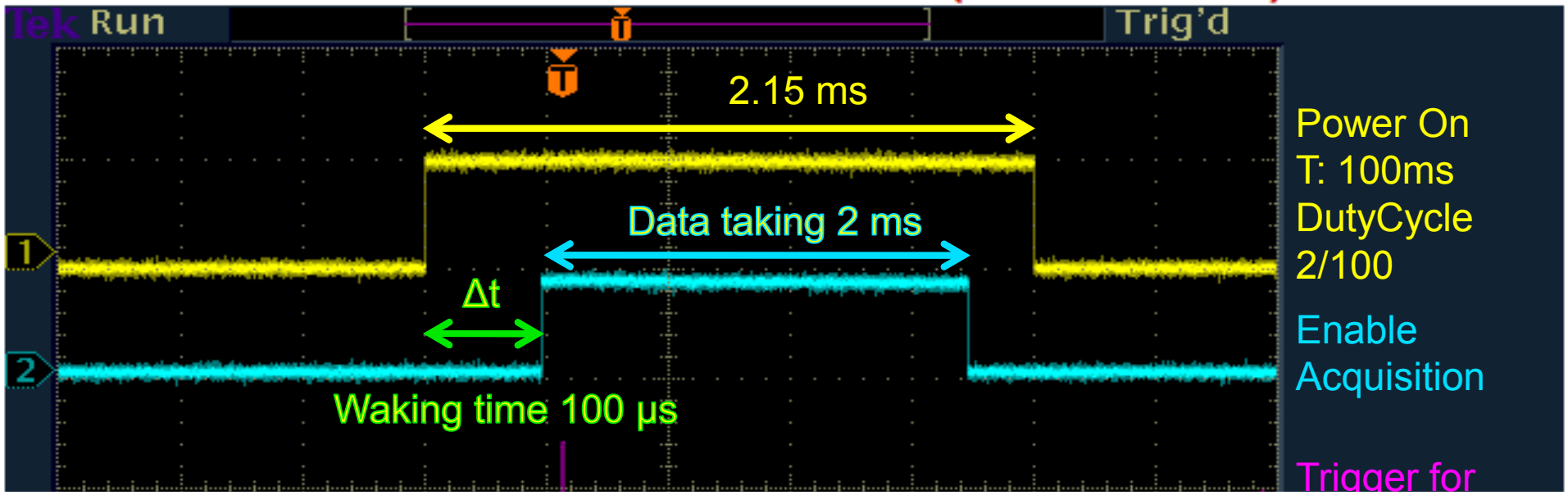
- ➢ French Si-ECAL technological prototype under construction.
- ➢ Analog HCAL : caracterised with Iron (tests with tungsten ongoing).
- ➢ SDHCAL under construction: testbeam scheduled June 2011
- ➢ DHCAL currently in testbeam at FNAL, together with the small Si-W ECAL prototype.

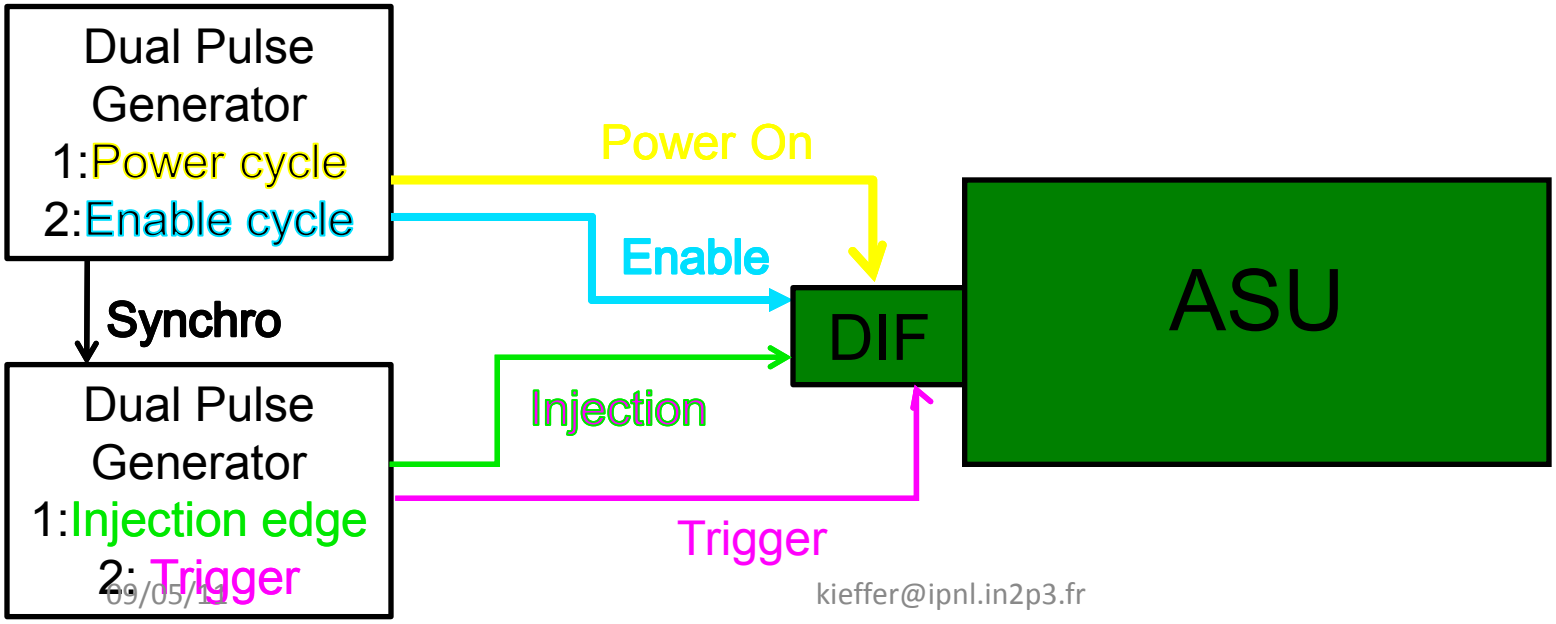
Backup slides

Injection with power pulsing

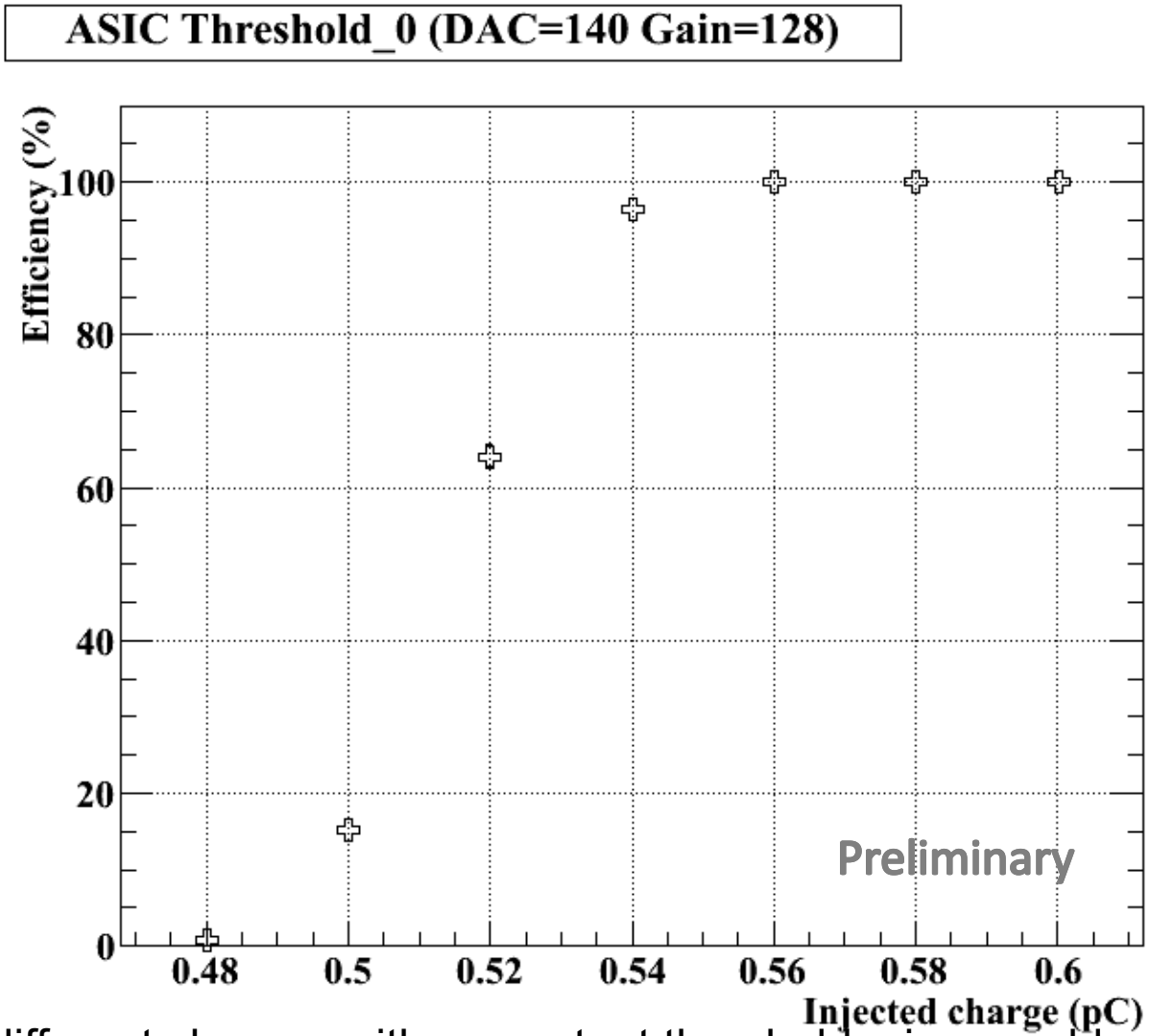


Injection with power pulsing



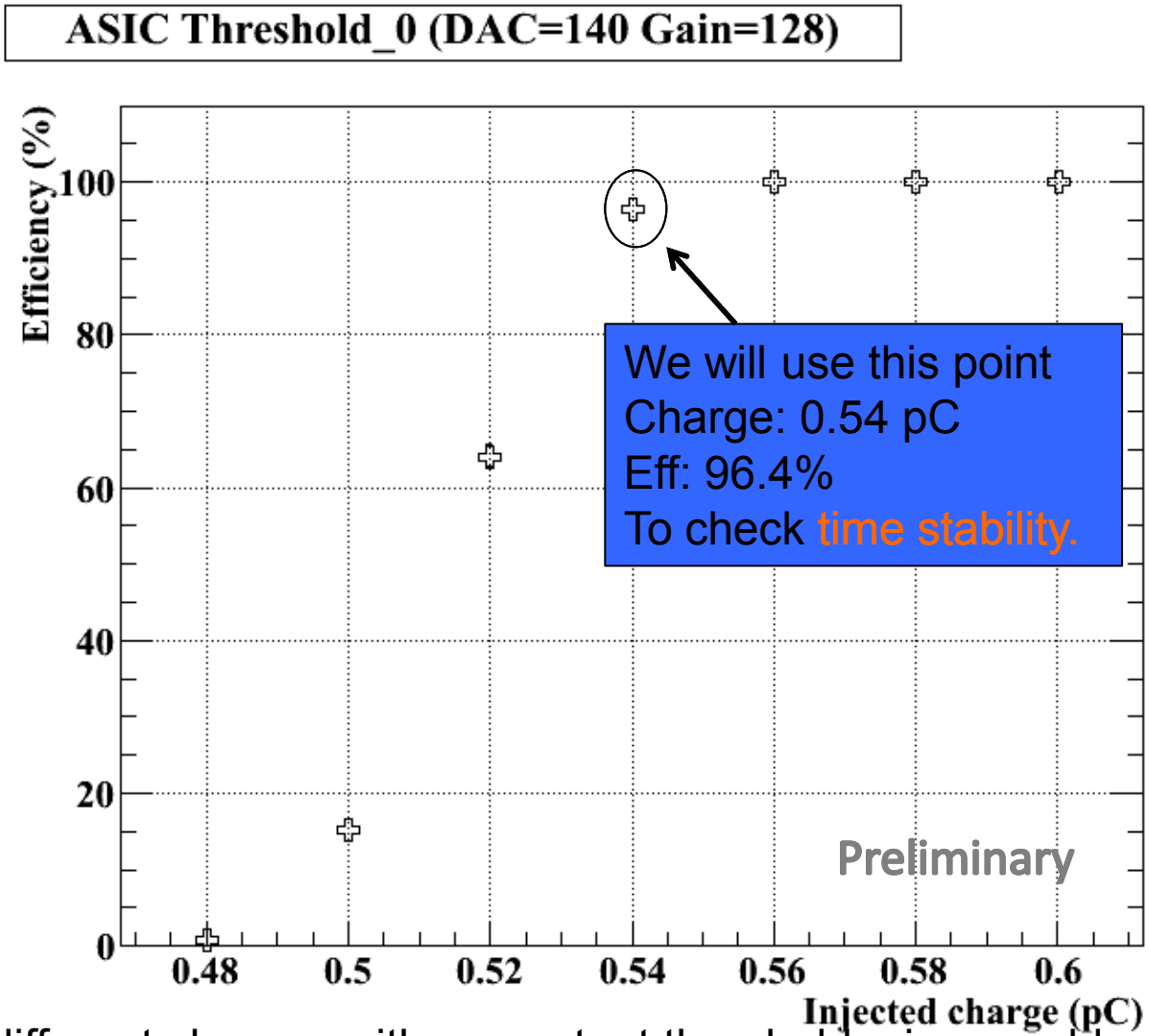


Injection with power pulsing



Injecting different charges with a constant threshold, give roughly a DAC/Charge value for HARDROC 2B. **=> 140 DAC ≈ 0.53 pC** (on Threshold_0)

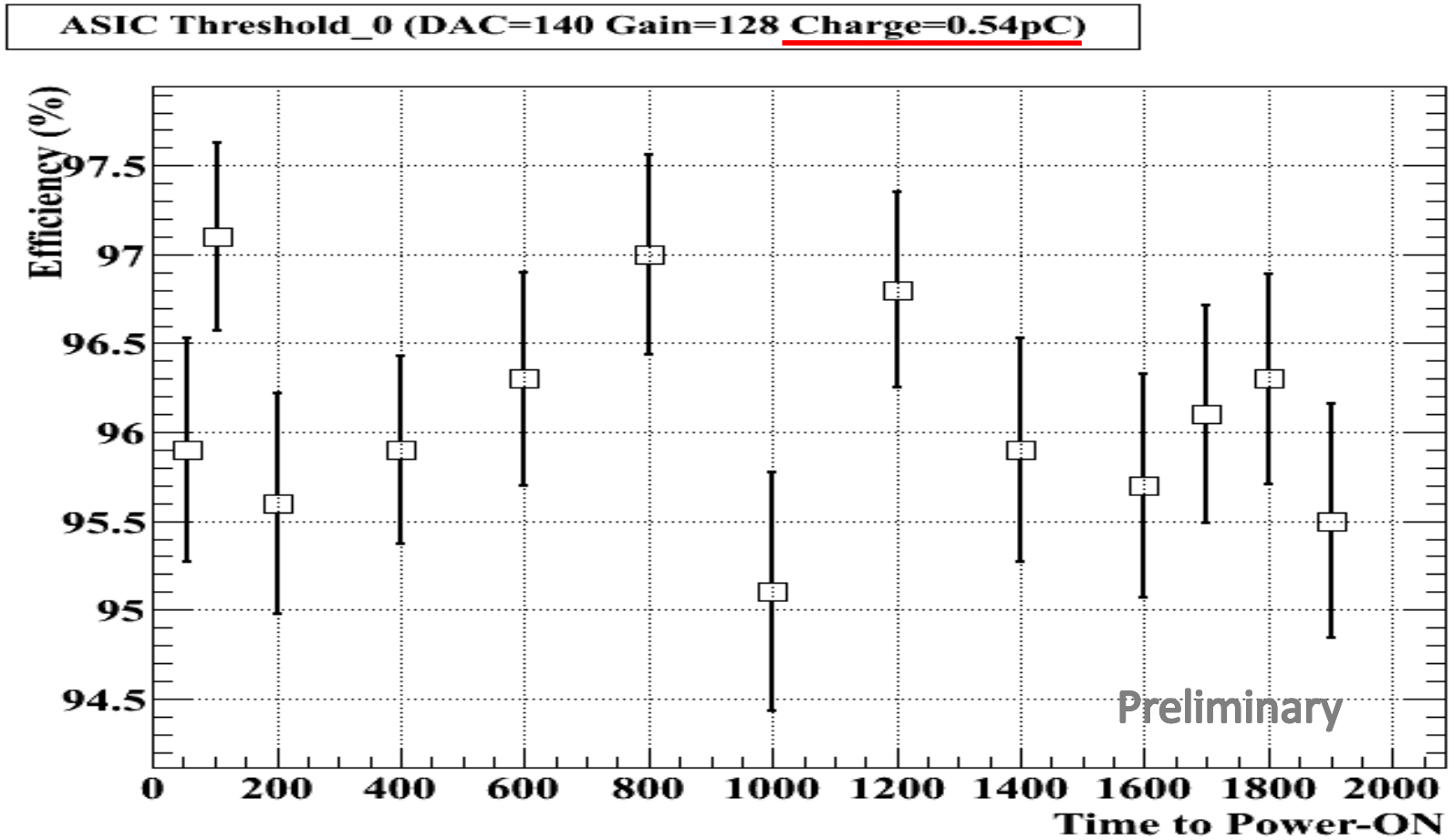
Injection with power pulsing



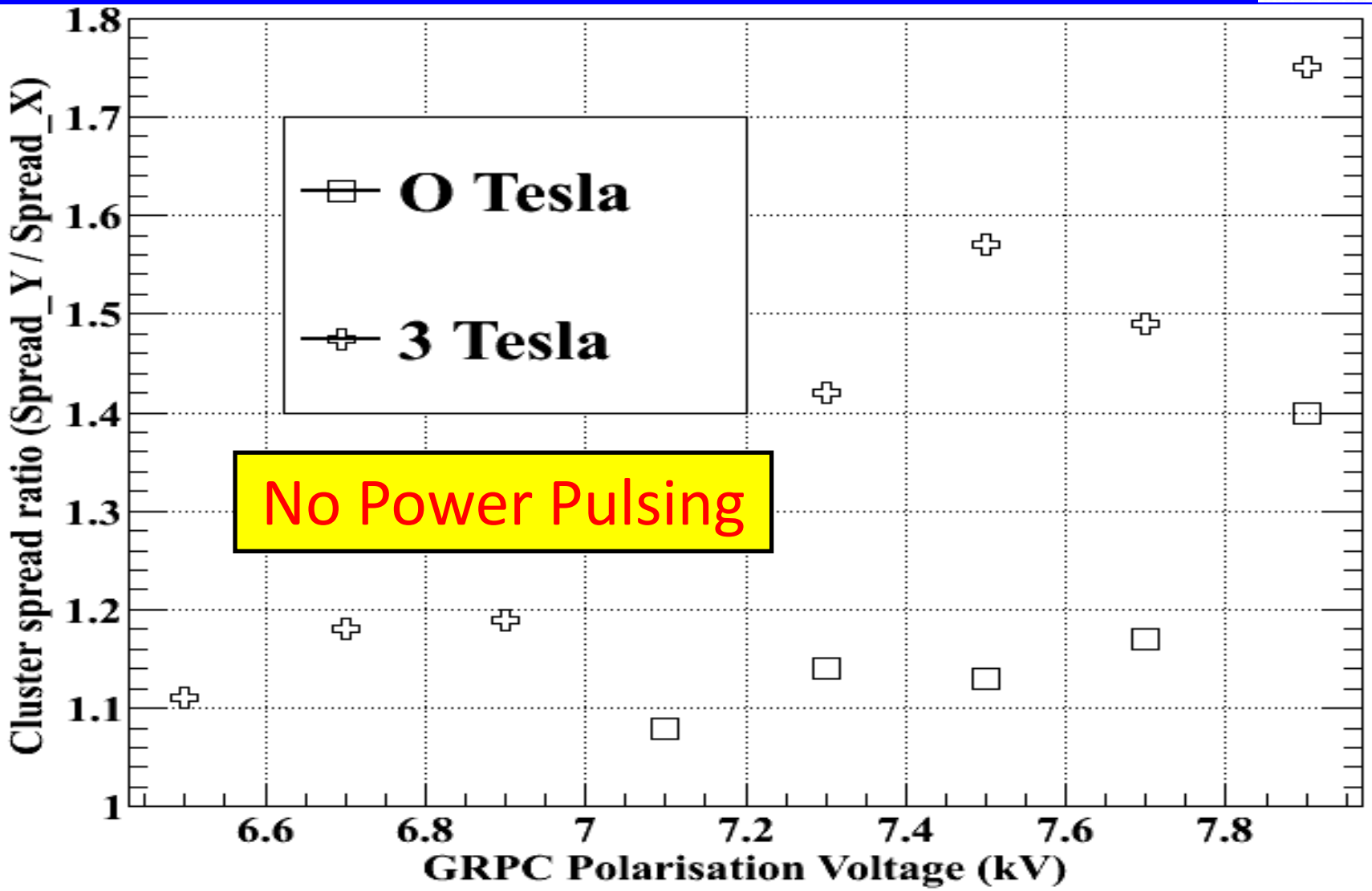
Injecting different charges with a constant threshold, give roughly a DAC/Charge value for HARDROC 2B. **=> 140 DAC ≈ 0.53 pC** (on Threshold_0)

Injection with power pulsing

Suspecting threshold stability, we injected charges with different delays from Power-ON edge. Efficiency is quite constant during the 2ms power cycle.
Work is still ongoing to understand efficiency loss recorded on beam data.

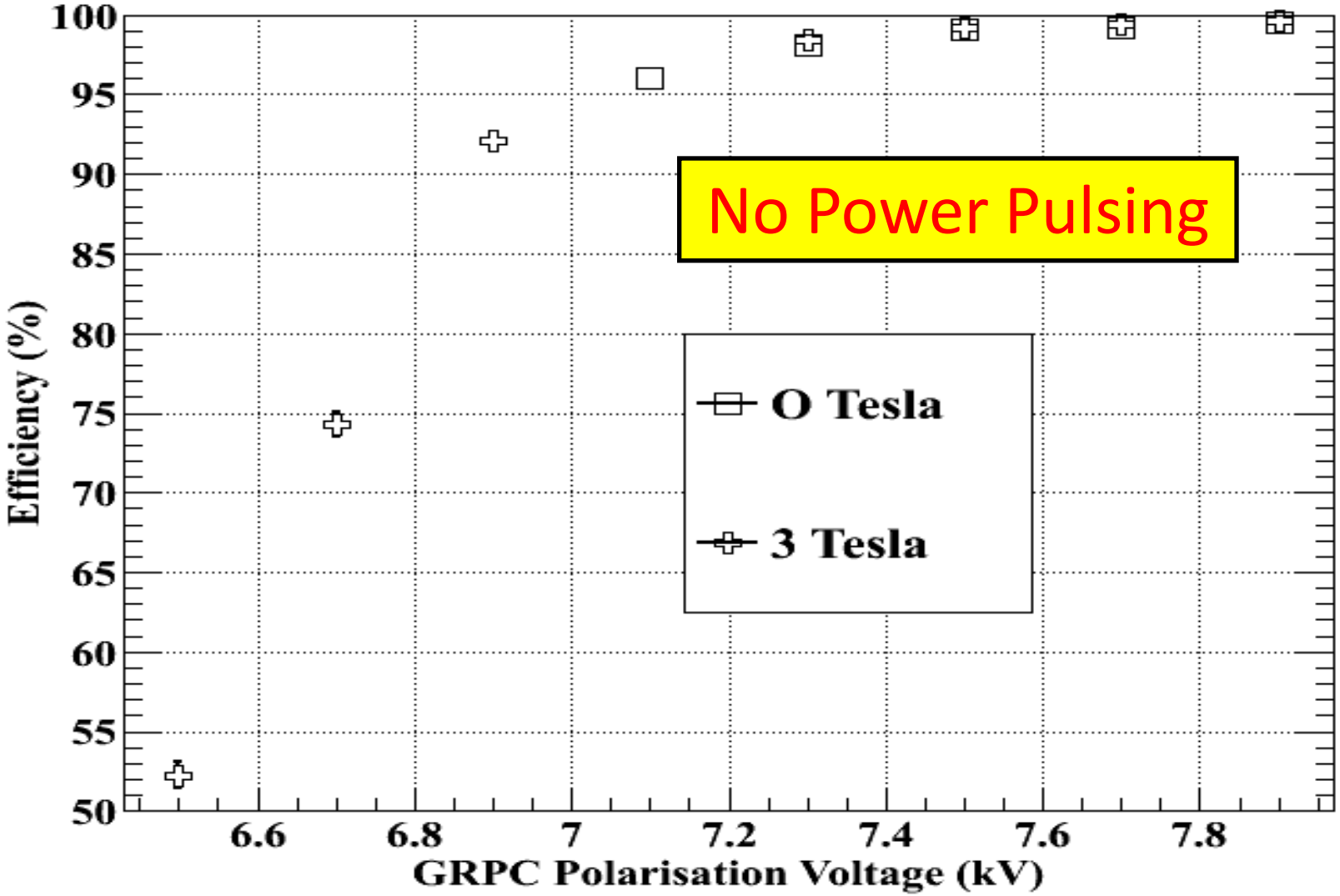


Preliminary tests using B field



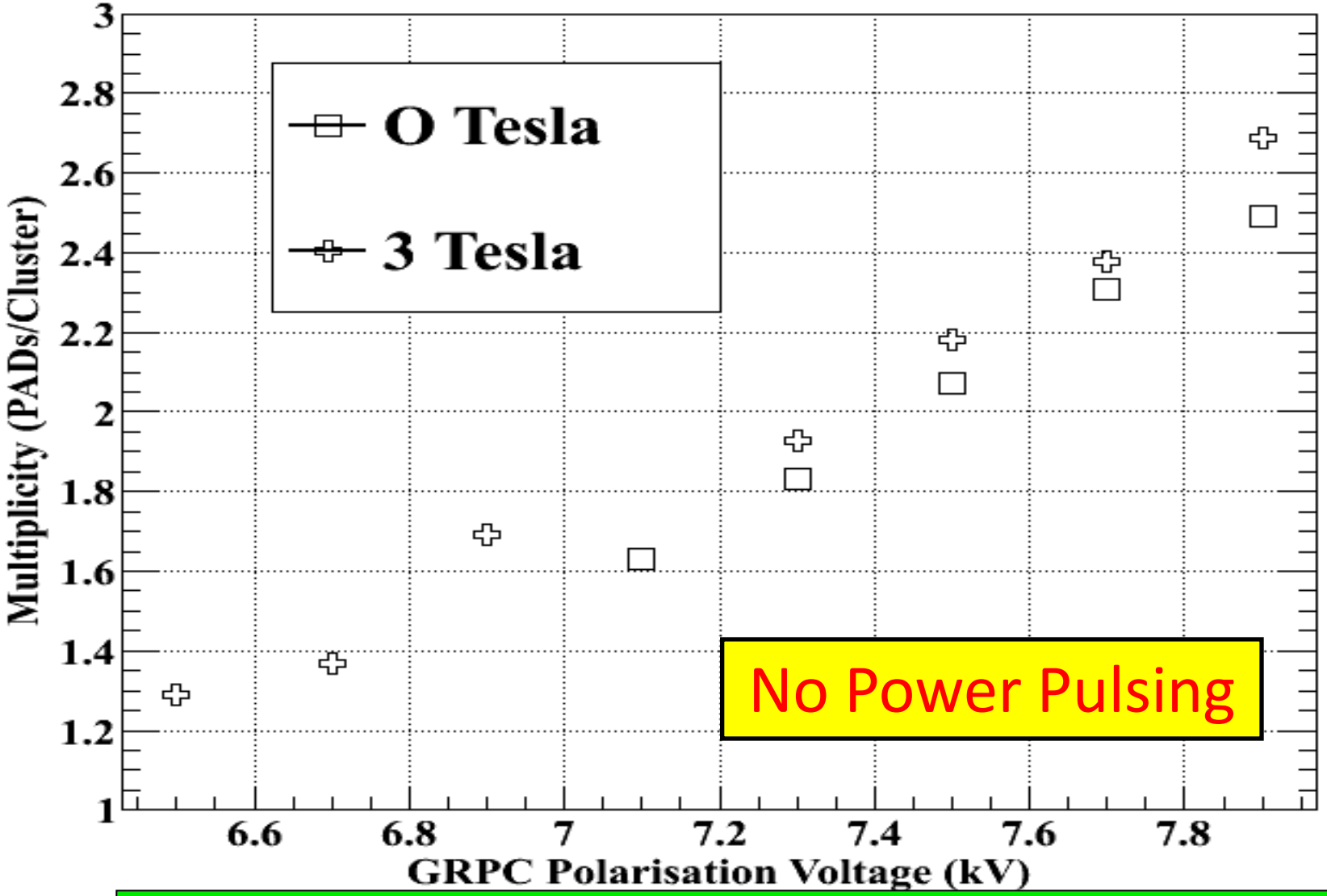
Is having an effect on cluster shape?

Preliminary tests using B field



B field has no impact on efficiency.

Preliminary tests using B field



increase a bit the multiplicity.