UNIVERSITY OF LIVERPOOL

Serial Powering for the ATLAS Inner Detector for SLHC

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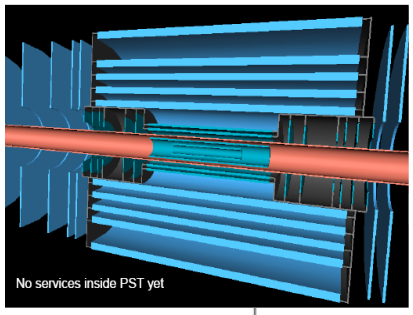
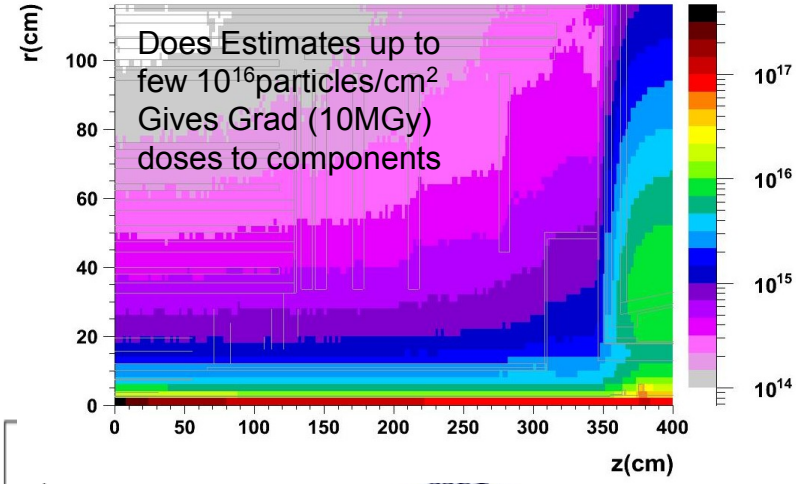
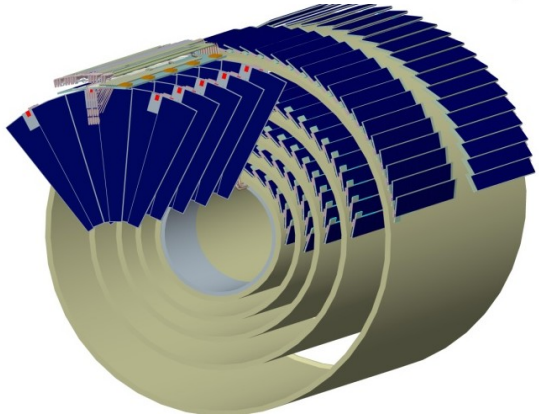
On behalf of the ATLAS Upgrade Community
SP work and most of the slides "borrowed" from Bonn, LBL, Penn, BNL, RAL, FNAL, Krakow

ATLAS Phase II Tracker Upgrade







Barrel Pixel Tracker Layers:	r = 3.7cm, 7.5cm, 15cm, 21cm
Short Strip (2.4 cm) μ-strips (stereo layers):	r = 38cm, 50cm, 62cm
Long Strip (9.6 cm) μ-strips (stereo layers):	r = 74cm, 100cm

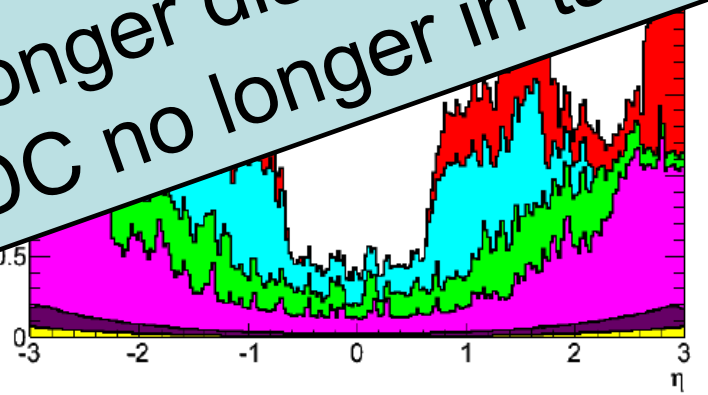
ATLAS pixels powering

LHC → sLHC

FE channels:	~80M	→	~455M	x5-6 gra…
Total FE power:	6.7kW	→	12.3kW	→ x…
Total FE current:	3.8kA	→	11kA	

- @LHC: independent powering
  - 20% efficiency
  - Very massiv…
    - Hi…
    - …ow
    - drop
    - …wer efficiency
    - Reduced cables cross section

Need for DC-DC or serial powering for SLHC silicon systems considered self-evident. Parallel powering no longer discussed; motivations for SP/DC-DC no longer in talks



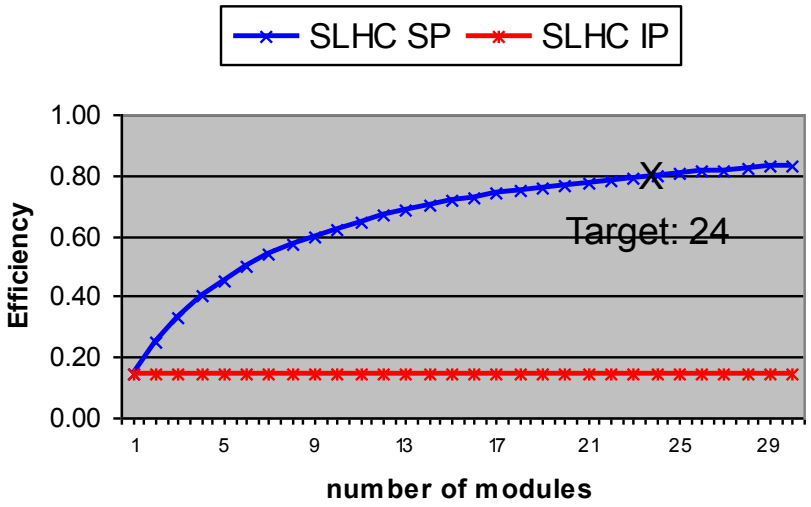
ATLAS inner det. material distribution (incl. IBL)

→ Serial powering or DC-DC conversion

Why Choose Serial Powering?

The power consumed by n hybrids is always **n I V,** but the power wasted in cabling depends upon the powering scheme!

for x = 6 (2.5A * 3.5 Ω / 1.5 V)



10 modules in series increases efficiency by factor ≈4

Consider n hybrids with:

- hybrid current I
- hybrid voltage V
- off-detector cable resistance R
- DC-DC gain g

and define **x= IR/V**

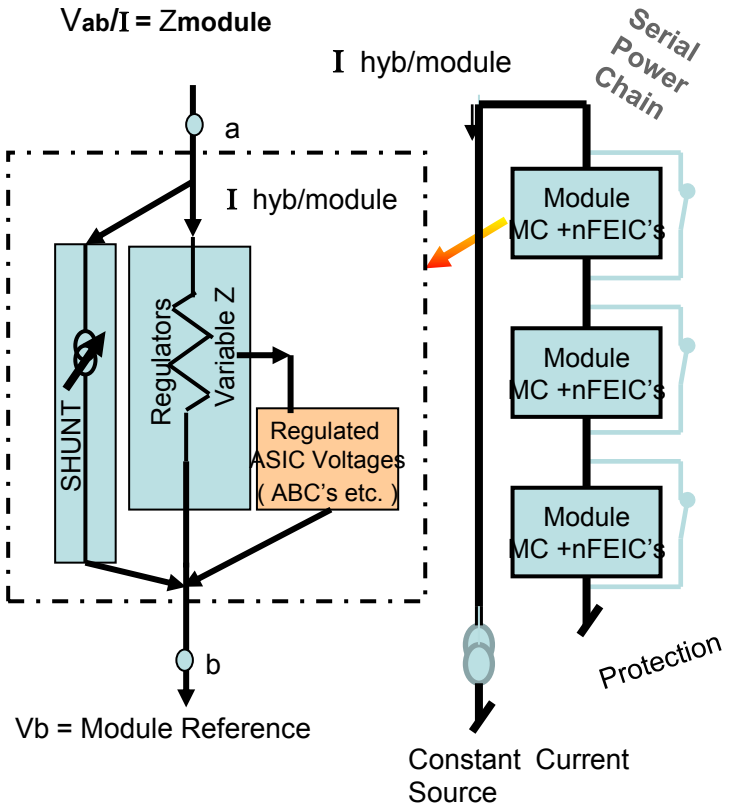
	I_{sm}	V_{drop}	V_{sm}	P_{cab}	Efficiency: P_{sm}/P_{total}
IP	nI	IR	V	nI^2R	$1/[1 + x]$
PP	nI	nIR	V	$n^2 I^2R$	$1/[1 + nx]$
SP	I	IR	nV	I^2R	$1/[1 + x/n]$
DC-DC	$\frac{nI}{g}$	$\frac{nIR}{g}$	gV	$\frac{n^2I^2R}{g^2}$	$\frac{1}{[1 + xn/g^2]}$

=> Low V bad, large R and I are bad

Values of these inputs are very system dependent. To get best results, they have to be considered at the design stages of ASICs, services, supports,….

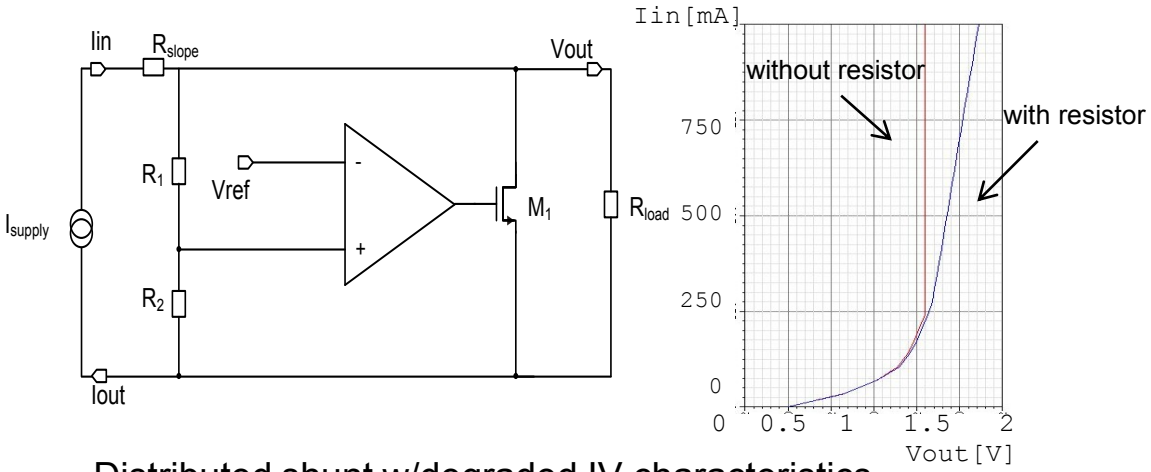
Serial Powering Concept

- Serial Power - One cable powers 'n' modules each with an equal current.
  - Benefits:
    - Low input current
    - Higher power efficiency (70-85% for systems)
    - Low material budget (extra ~0.03% radiation length for strips, excluding bus tape traces)
    - Simple, needs minimal external components
    - Highly flexible to changes to current/voltage after design
  - Requirements:
    - Constant current source
    - More complicated ground referencing
    - AC coupled Data & Control
    - Over-voltage and Open Protection
    - Module/Chip Bypass (Slow and automated)



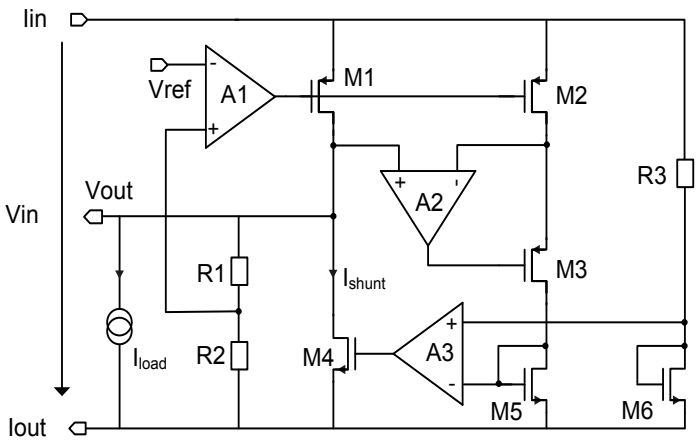
A good references for both Serial Power and for DCDC
The ATLAS – CMS Power Working Group Meetings
2011-https://indico.cern.ch/conferenceDisplay.py?confId=127662
2010-http://indico.cern.ch/conferenceDisplay.py?confId=85278

Two Shunt Layouts



Distributed shunt w/degraded IV characteristics

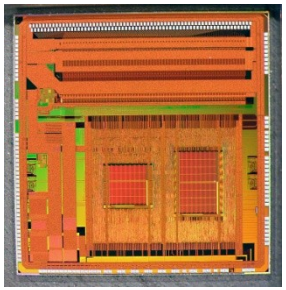
- Shunts in each FE ASICs
  - "Equivalent circuit" is a Zener diode
  - Resistor degrades IV characteristic to solve shunt turn-on mismatch issues
  - 1 regulator circuit per hybrid
  - 1 protection circuit per hybrid
  - Two voltages required generated by 1 or 2 LDOs on ASIC after shunt
- Already used in pixel FEI3 demostrator and strip ABCn 250 nm prototype chip
- One of the possibilities for strip upgrade



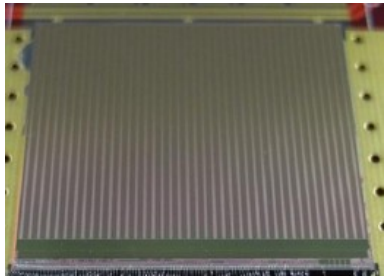
Distributed shunt/LDO

- Combined shunt/LDO pairs in parallel for each FE ASICs
  - "Equivalent circuit" is a resistor
  - Resolves shunt turn-on mismatch issues
  - Two voltages required generated by 2 Shunt-LDOs in parallel in each ASIC
    - Tunable voltage on both outputs
  - 1 protection circuit per hybrid
- Verified in 130 nm MPW submission and included and under test 130 nm FEI4 prototype pixel ASIC
- One of the possibilities for IBL and phase II pixels

Chip Summary



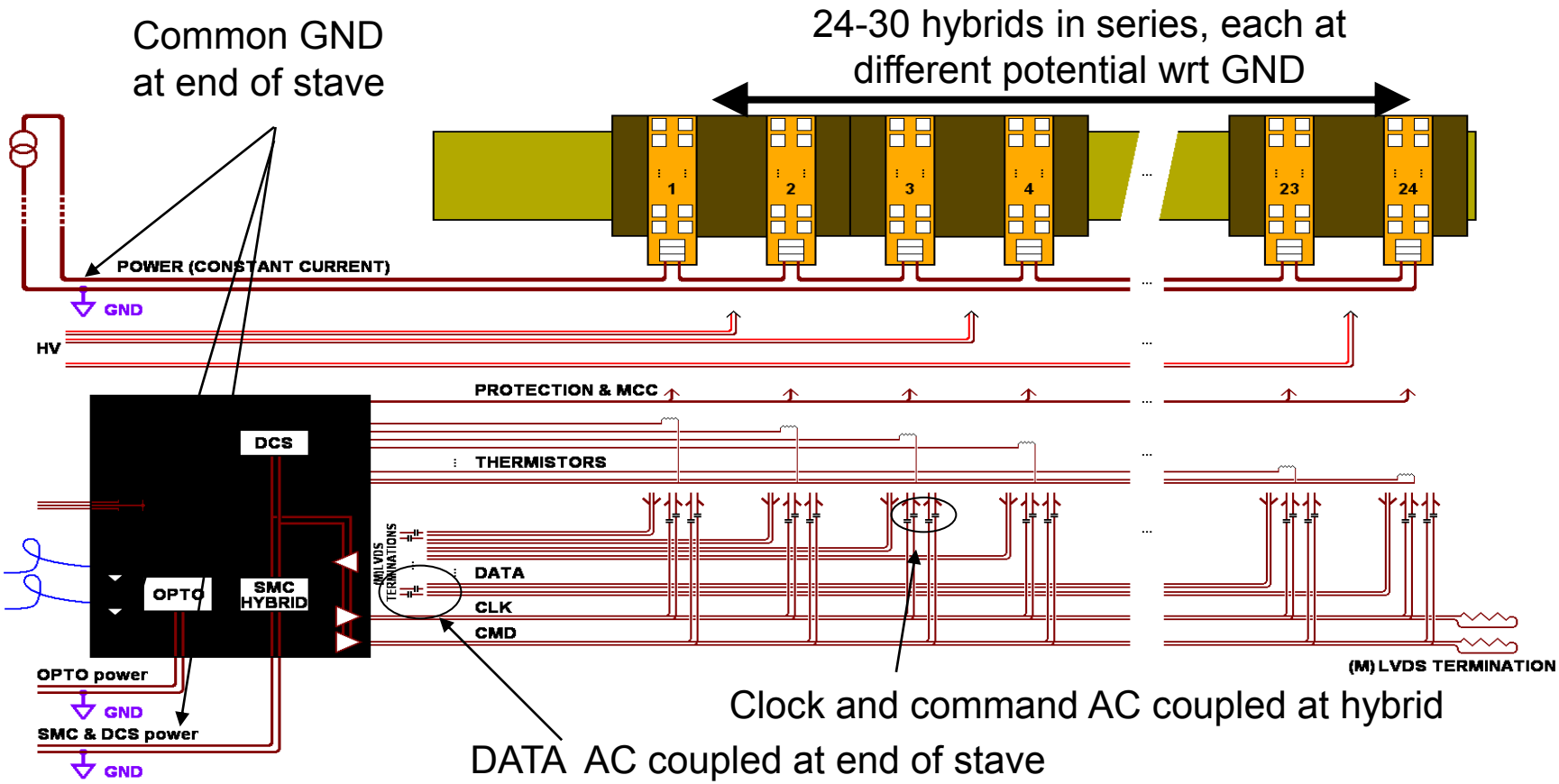
Currently In Layout



	ABCN (250 nm)	ABCN (130 nm)	FEI4 (130 nm)
Number Channel Per Chip	128	256	26880
Number of Chips per Hybrid	20	10	4
Number of Hybrids per Chain	8-24	24-30	10-12
Digital, Analogue Voltages	2.5 V, 2.2 V	0.9 V, 1.2 V	1.2 V, 1.5 V
Digital, Analogue Currents	92 mA, 90 mA	60 mA, 102 mA	150 mA, 360 mA
Current in Chain	5 A (3.6 A)	2.2 A	2.4 A

Strip studies shown use ABCN (250 μm)
Pixel studies shown use FEI4 (130 μm)

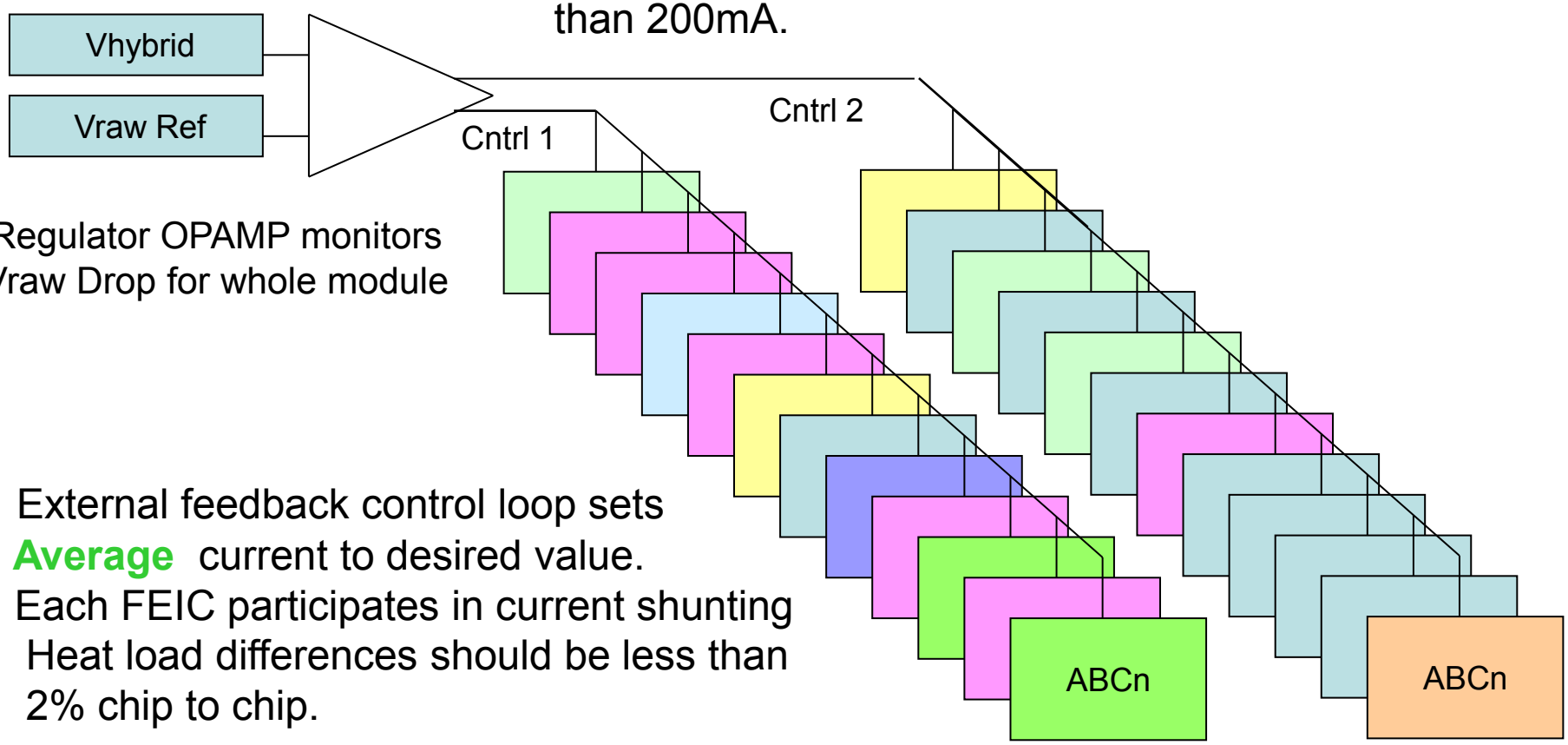
SP Strip Stave Architecture



- **Hybrid with Distributed Shunt**
  - Use one external shunt regulator and external SP protection
  - Use each ABCN's integrated shunt transistor(s)
    - Two (redundant) shunt transistors, 140mA each

Serial Power Control Circuit

Power current path **distributed** among ABCn chips. No interruption. **Highly redundant**. No chip shunts more than 200mA.

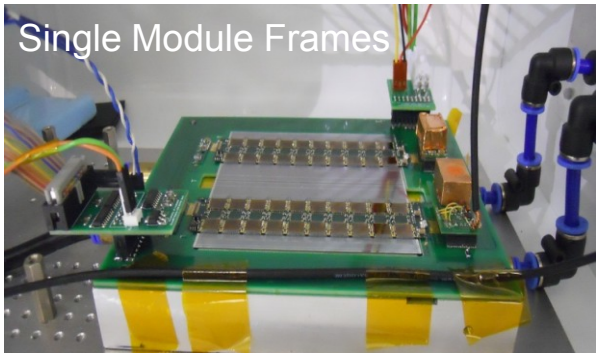


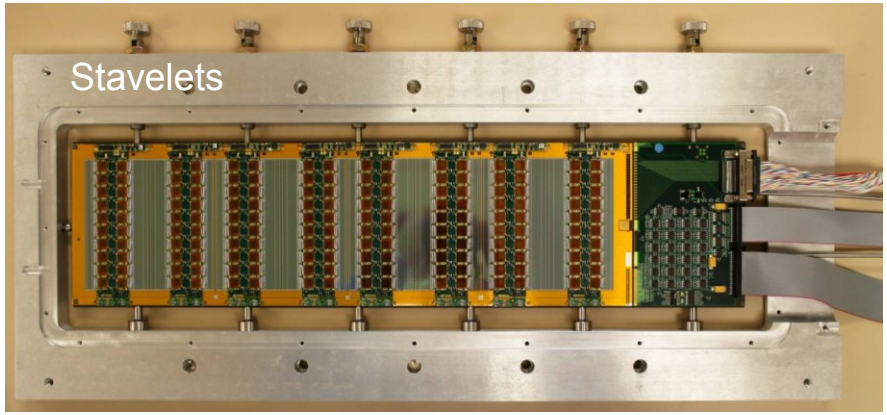
Regulator OPAMP monitors Vraw Drop for whole module

External feedback control loop sets **Average** current to desired value.
Each FEIC participates in current shunting
Heat load differences should be less than 2% chip to chip.

Strip Electrical Test Vectors

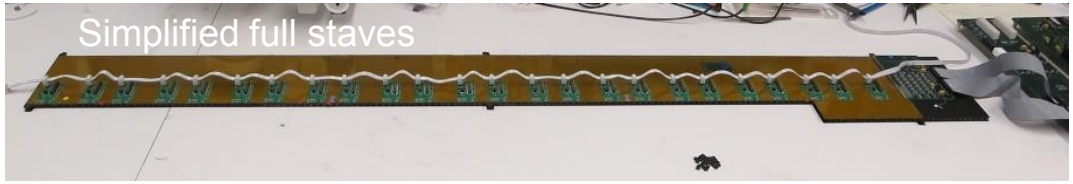
- Frame with plug-ins for early testing of:
  - Serial Power Control
  - Serial Power Protection (discrete or custom ASIC)
  - DC-DC convertors
  - Multi-drop AC-coupled LVDS clock/control
  - Shielding/Grounding





- 4 module devices for tests of:
  - System powering effects
    - DC-DC or Serial Power
  - Shielding/Grounding
  - Noise from AC-coupled MLVDS
  - DAQ development

- Simplified full length devices for specialized tests
  - Multi-drop AC coupled LVDS
  - Serial power protection

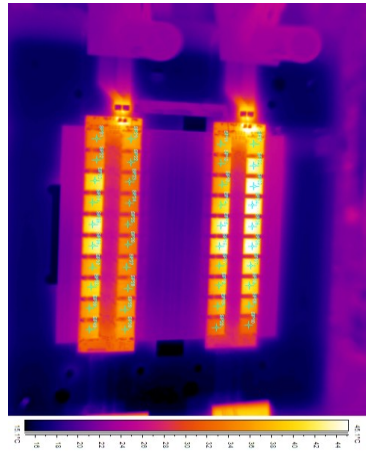


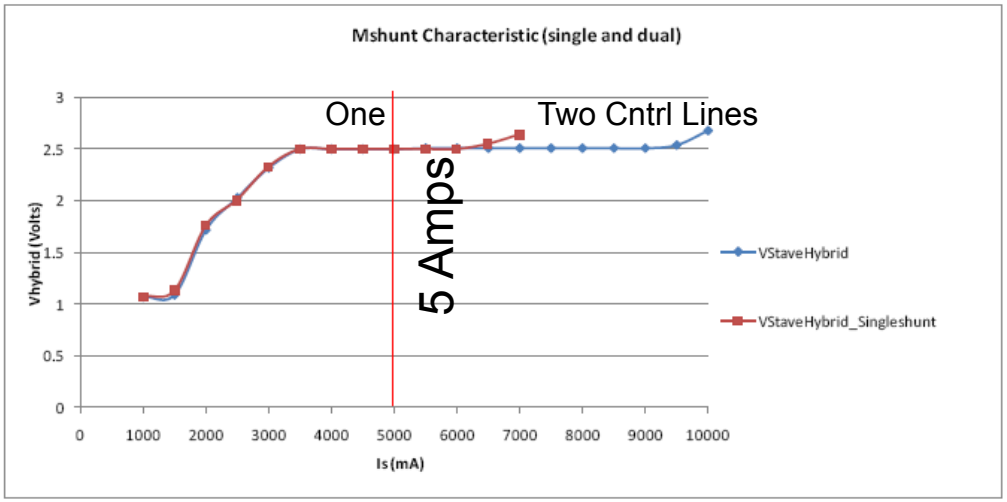
Stave Hybrids

Hybrids are designed for two powering schemes:

1. Parallel power, which could be provided by DCDC converters

2. Shunt regulation, using the distributed shunt regulators integrated within the ABCN-25s
   - Required for serial powering – Mshunt is the default scheme



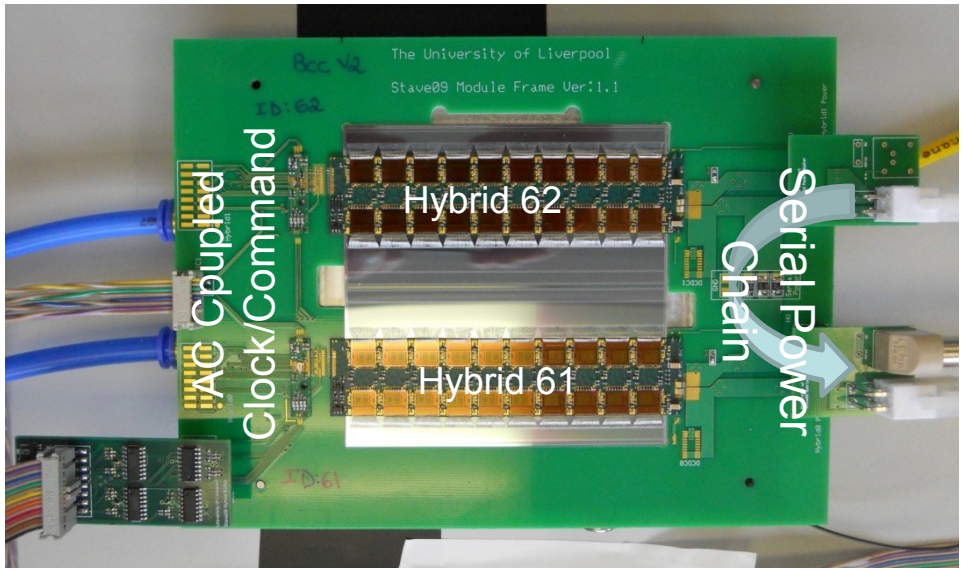


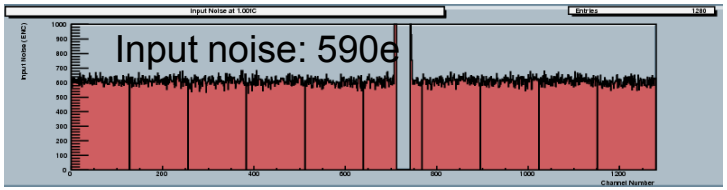
Mshunt characteristic for single and dual shunts enabled per ABCN-25 on a 20 ASIC hybrid
(expect max. Hybrid shunted current to be ≤5A)

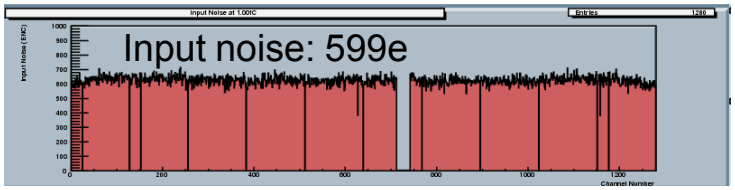
Single Shunt transistor enabled per ABCN-25 (20 x shunt transistors)
Shunt regulates Vhybrid to 2.5V at I_s>3.5A and diverges at I_s<6.5A (*cf* I_{hybrid} +I_{smax} (3.6 + (20 x 0.14))) = 6.4A

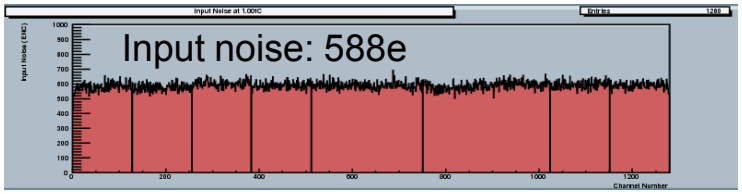
Dual Shunt transistors enabled per ABCN-25 (40 x shunt transistors)
Shunt regulates Vhybrid to 2.5V at I_s>3.5A and diverges at I<9.5A (*cf* I_{hybrid} +I_{smax} (3.6 + (40 x 0.14))) = 9.2A

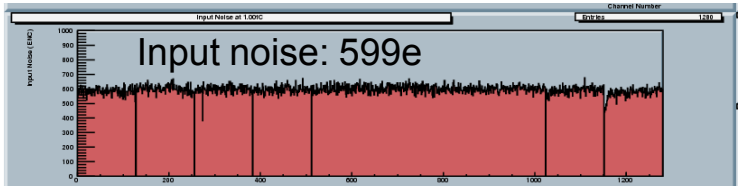
Stave Module Noise









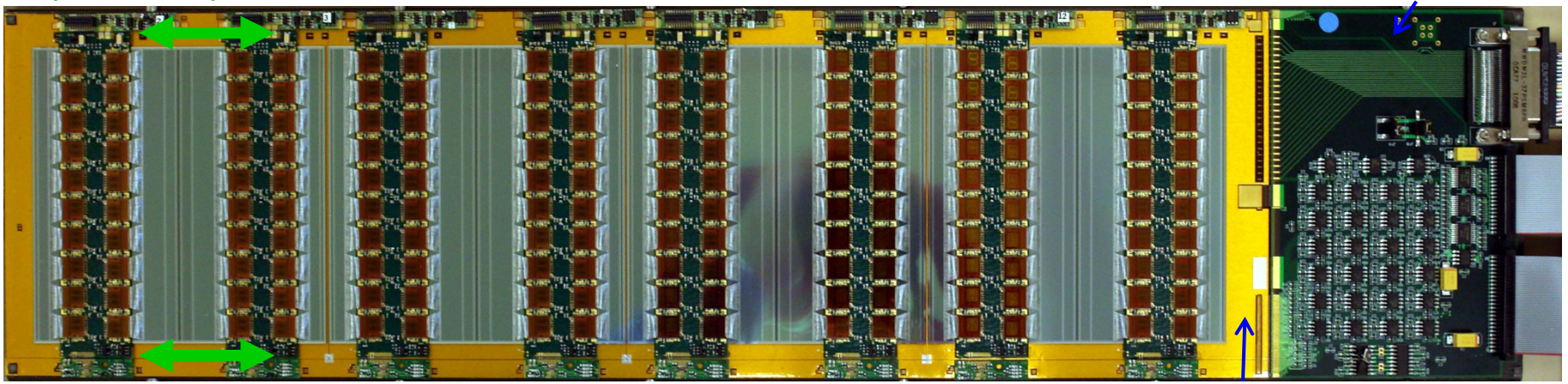


- 2.5V per hybrid, ~5V total across the module (using constant current source)
- One hybrid is DC referenced to sensor, the other AC
- Use BCC ASICs for digital communication (AC-coupled LVDS), powered from hybrid

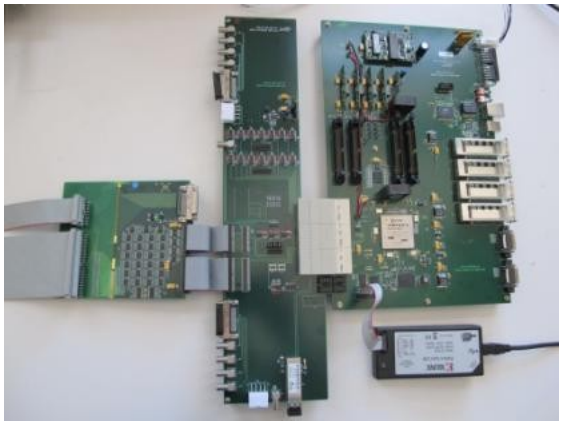
Serially powered module performs same as with parallel powering!!!

	Parallel Power	Serial Power
Hybrid 62	590e/596e	590e/599e
Hybrid 61	585e/591e	588e/599e

Stavelets



- Shortened Stave, built as electrical test-bed
  - Shielding, grounding, power, multi-drop LVDS
- First Stavelet serial powered with on-hybrid control
  - Power Protection Board (PPB) allows each SP hybrid to be bypassed under DCS control
  - Other powering options to be tested later
- Using Basic Control Chip (BCC)
  - Generates 80MHz data clock from 40MHz BC clock
  - 160Mbit/s multiplexed data per hybrid
- Readout using HSIO board from SLAC

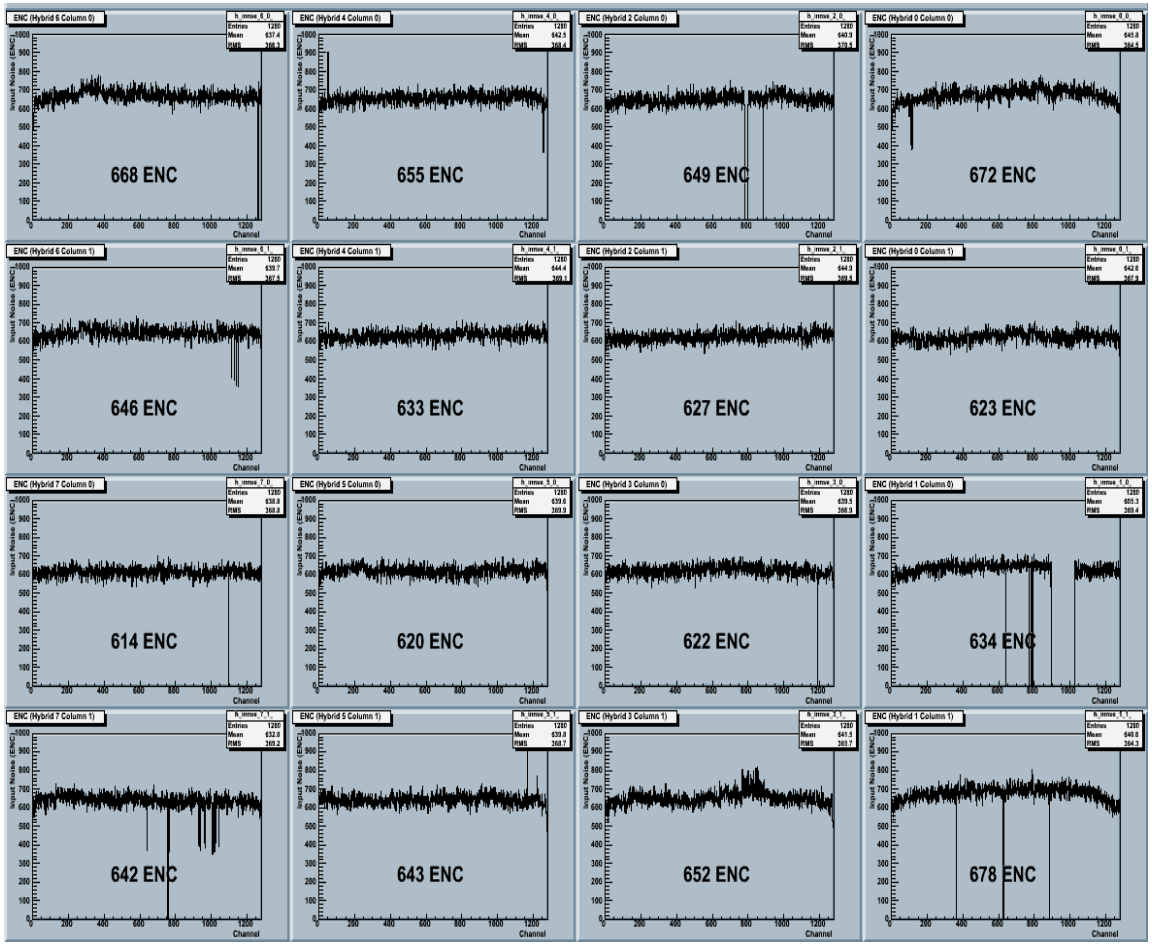


HSIO + interface

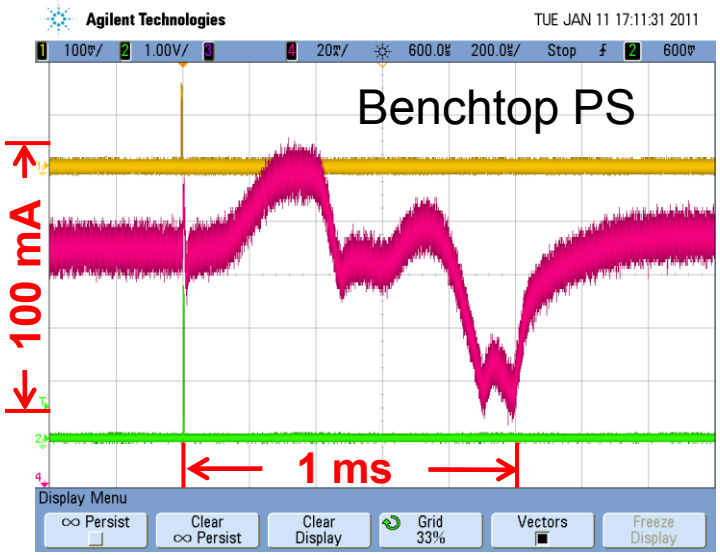
Serially Power Stavelet Noise Performance

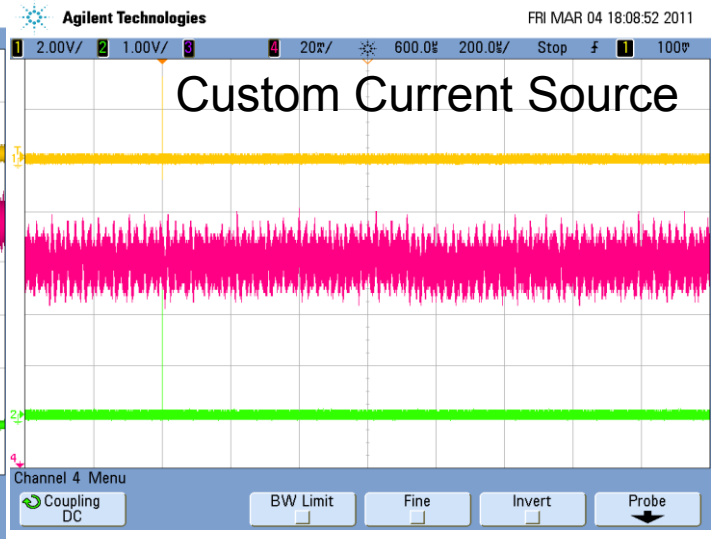
- Used on-hybrid shunt control circuit
- Stavelet noise approaching single module tests
  - Roughly ~20 e^- higher
- Plan to extend tests to other SP plug-in controllers (ASICs) as they become available
- Still more work to go to get ultimate noise performance, but already acceptable for needed signal-to-noise

Noise for 16 columns of chip on stavelet



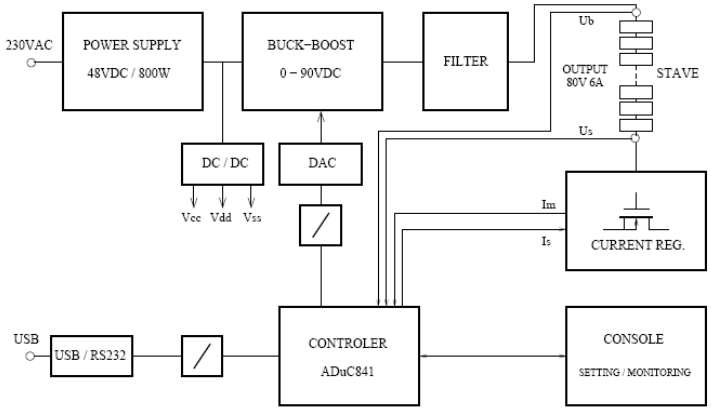
Custom Constant Current Source





Current source is “stiffer” to ABCN25 current bump after trigger

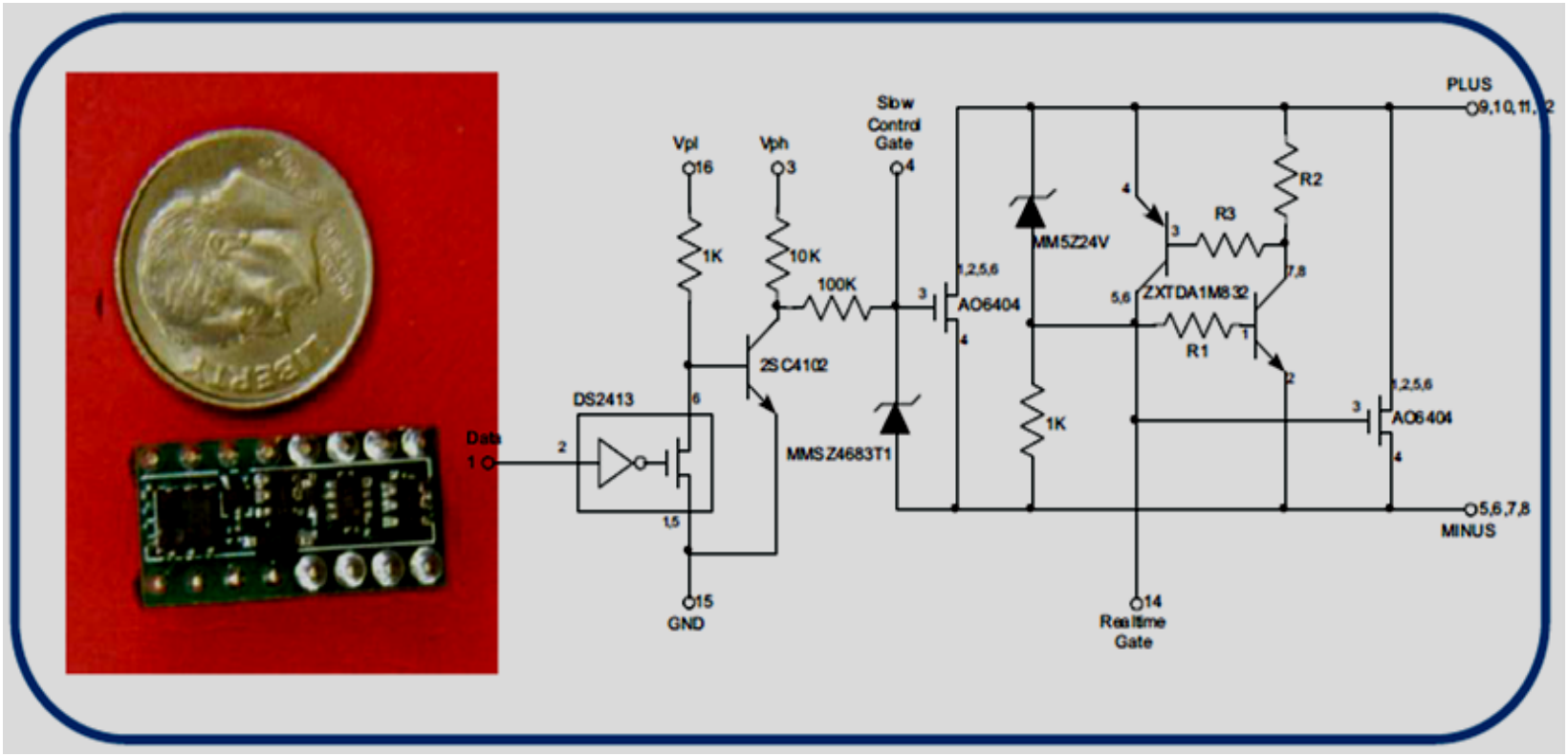
- Programmable current source has been prototyped
- Designed for full-length stave, output up to 80V at 6A
- Includes isolated USB interface and overvoltage protection/interlock



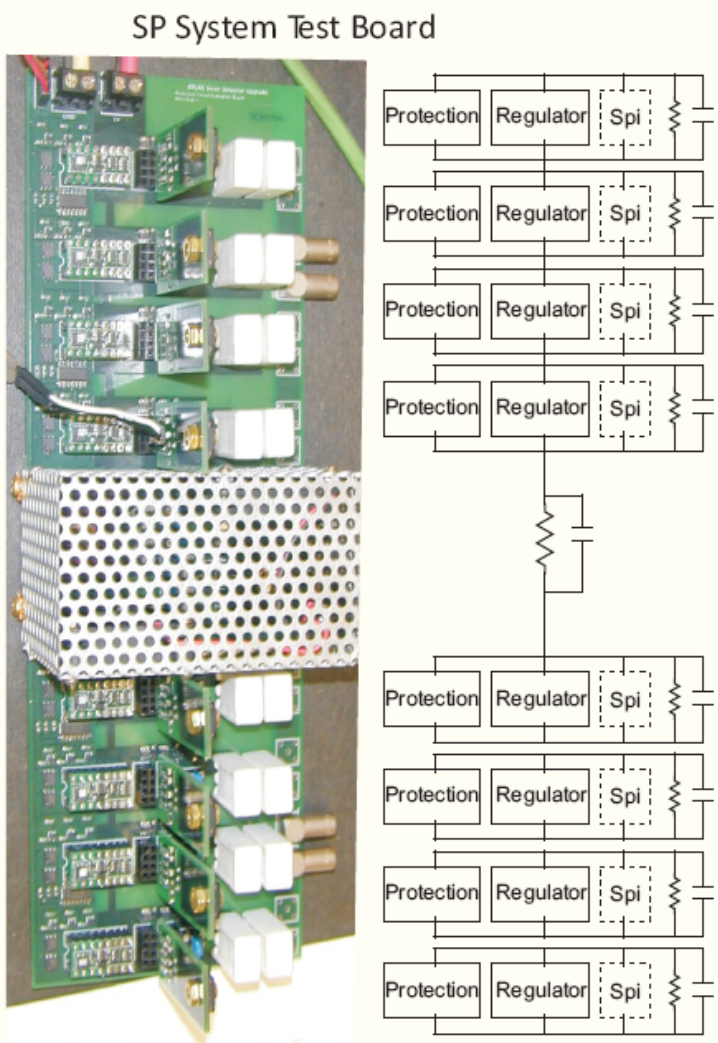
Serial Power Protection

For first test, serial power protection circuit made with discrete components

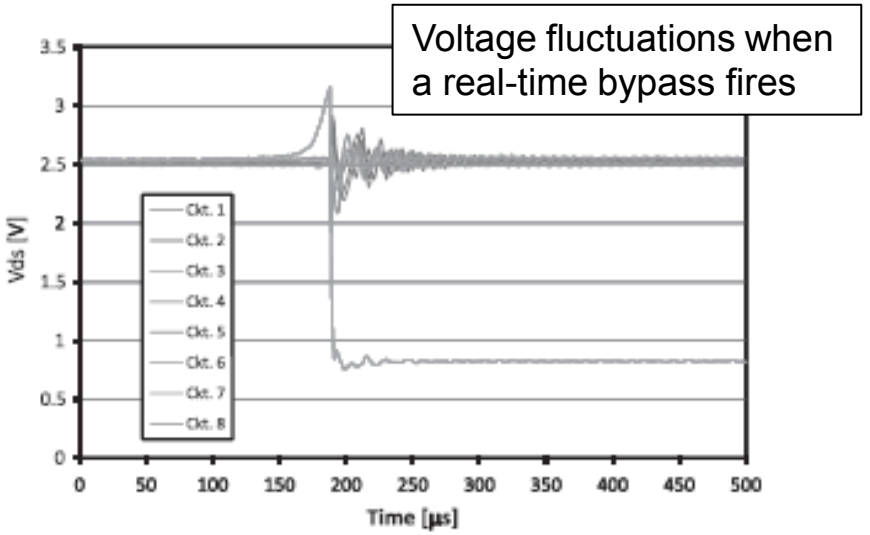
- One wire Addressable by Hybrid Serial Power Control
- Installed on each of the 8 Stavelet Hybrids.
- An SCR function allows autonomous shut down on Over Voltage Sense



Serial Power Protection Studies



- Mimics 8 hybrids + protection + regulators
  - Mimics clock dependent current loads
  - Studies power-up issues
- Tests real-time circuits; can induce controlled “open circuits”
- Tests 1-wire bypass circuits

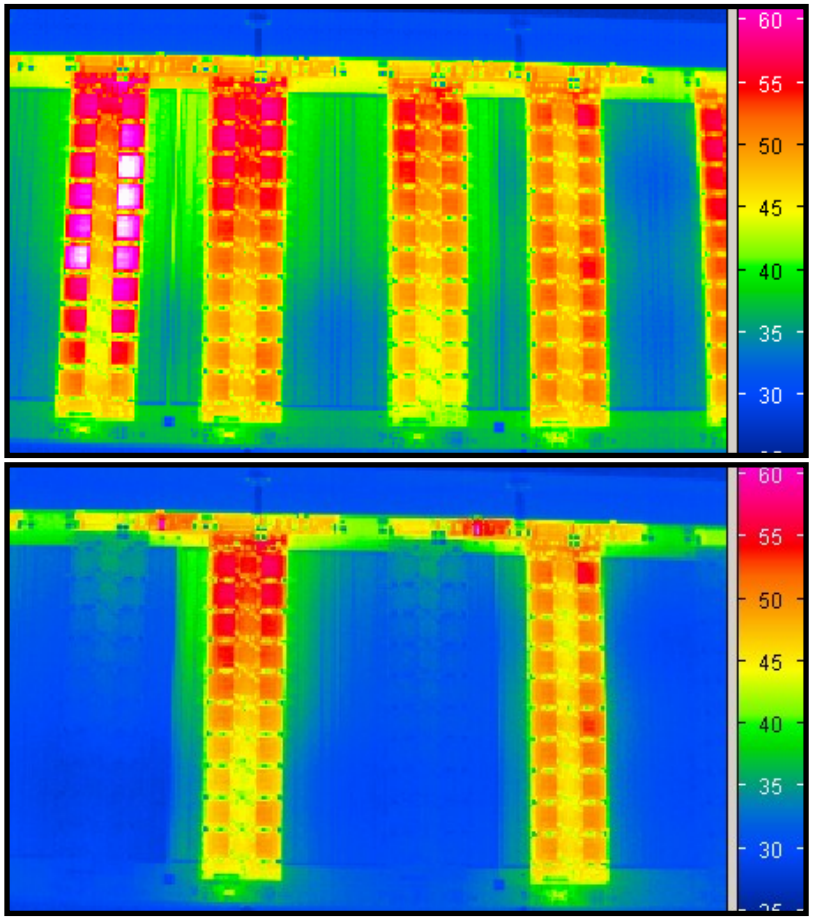


M-shunt board

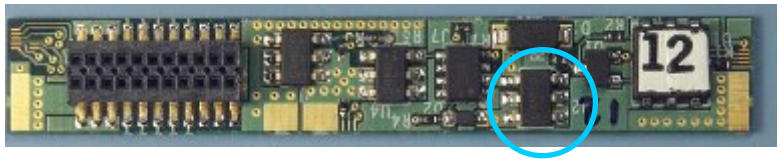
SPi board

“Serial power protection for ATLAS silicon strip staves”, D. Lynn, et al., Nucl. Instr. and Meth. A 633 (2011) 51-60

Serial Powering Protection on Stavelet

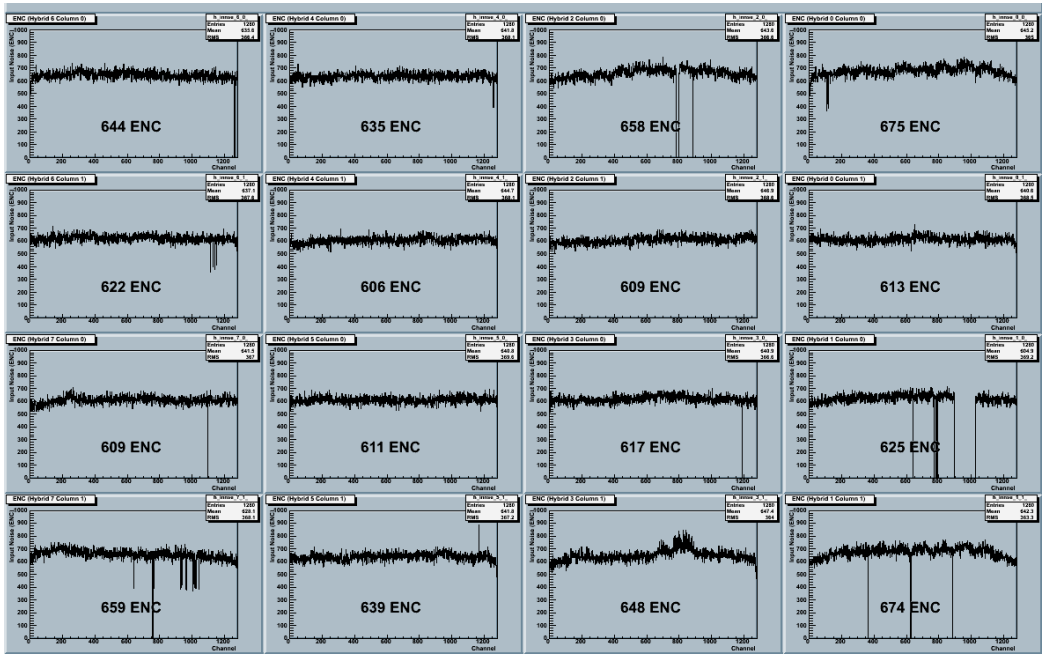


0.5 W



- Hybrid bypassing works as expected
  - P=VI=100 mV*5 A=0.5 W
  - Noise slightly lower with neighbour's bypassed

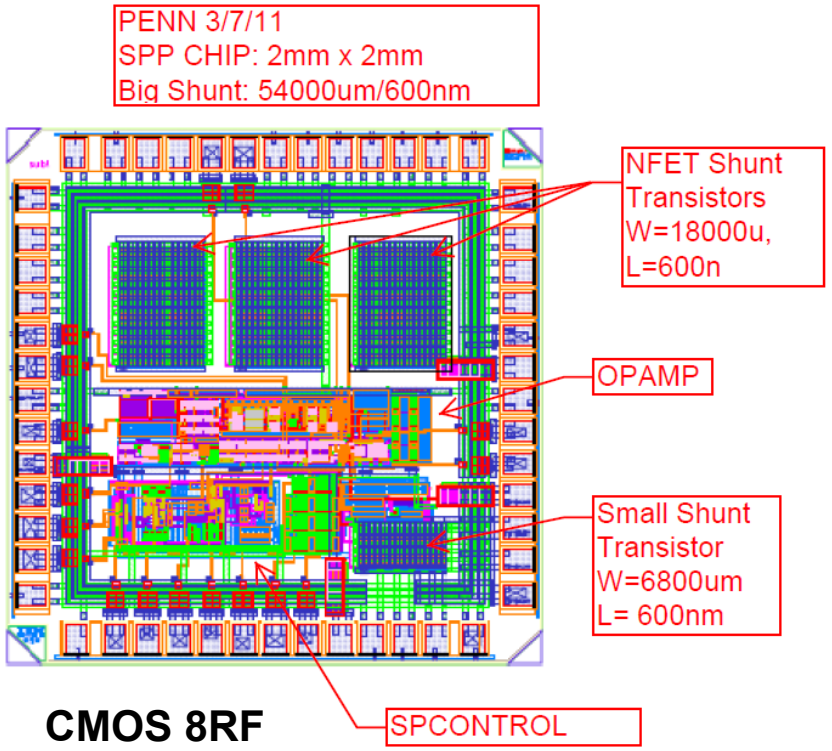
Constant Current Source at 5A, ODDS AND EVENS, Composite



Serial Power Protection ASIC

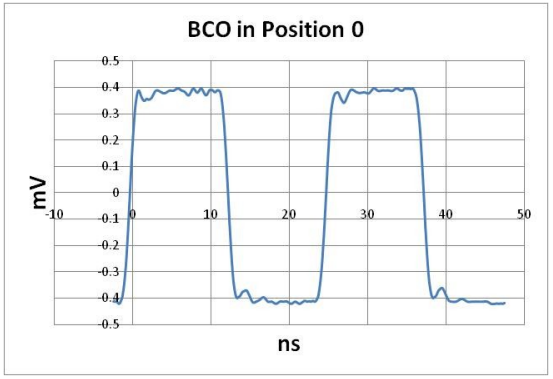
Custom serial power protection ASIC (130 nm) is in design.
Analogue only section prototyped in MPW under test
"Serial Power & Protection (SPP) ASIC for 1 to 2.5V Hybrid Operation"
http://indico.cern.ch/getFile.py/access?contribId=11&resId=0&materialId=slides&confId=85278

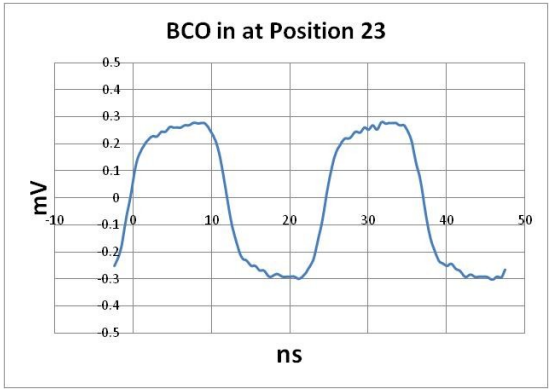
- Designed for use with 250 nm and 130 nm ABCNext
  - One wire control circuit supplies power to the SPP and controlled programmable shut down control
    - SPP chip has internal shunt regulator to set its voltage to 2.3V.
  - On chip band gap forms reference for SPP 2.3V and for hybrid voltage.
  - Hybrid voltage may be set from 1V to 2.5V
  - SCR for autonomous shut down for over voltage.
    - ~100 mV across hybrid with autonomous shutoff
  - On board shunt transistor available to guarantee hybrid switch off.
    - ~60 mV across hybrid with controlled shutoff

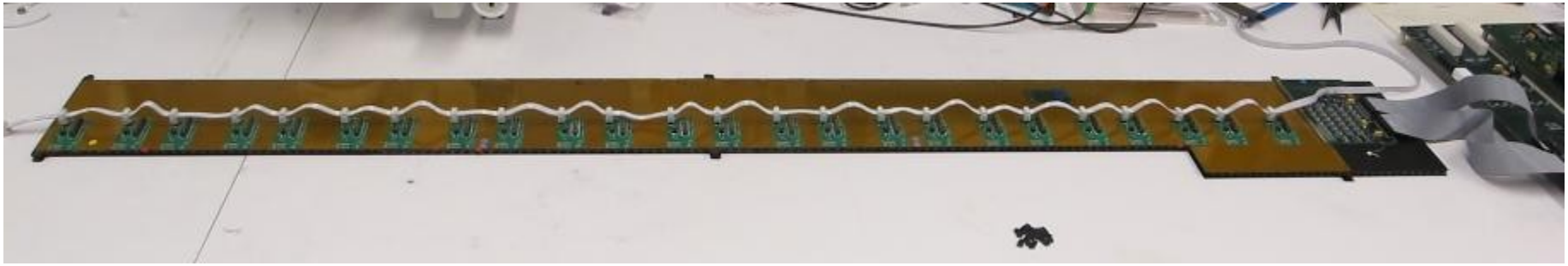


Full-scale LVDS Test

- Need to determine “maximal” chain for clock/command using AC-coupled multi-drop LVDS
- Designed/manufactured the Buffer Controller Chip (BCC) in 250 nm IBM to allow multi-module testing in a serial power chain
  - Developed by SLAC/UCL/Cambridge/LBNL
  - Generates 80 MHz data clock and multiplexes data lines
  - Replaced in final chip set by Hybrid Controller Chip (HCC)
- Chain of 24 BCC operated as a system on the full length bus
  - Sufficient amplitudes and short enough rise time for all positions for BCC to regenerate clocks correctly

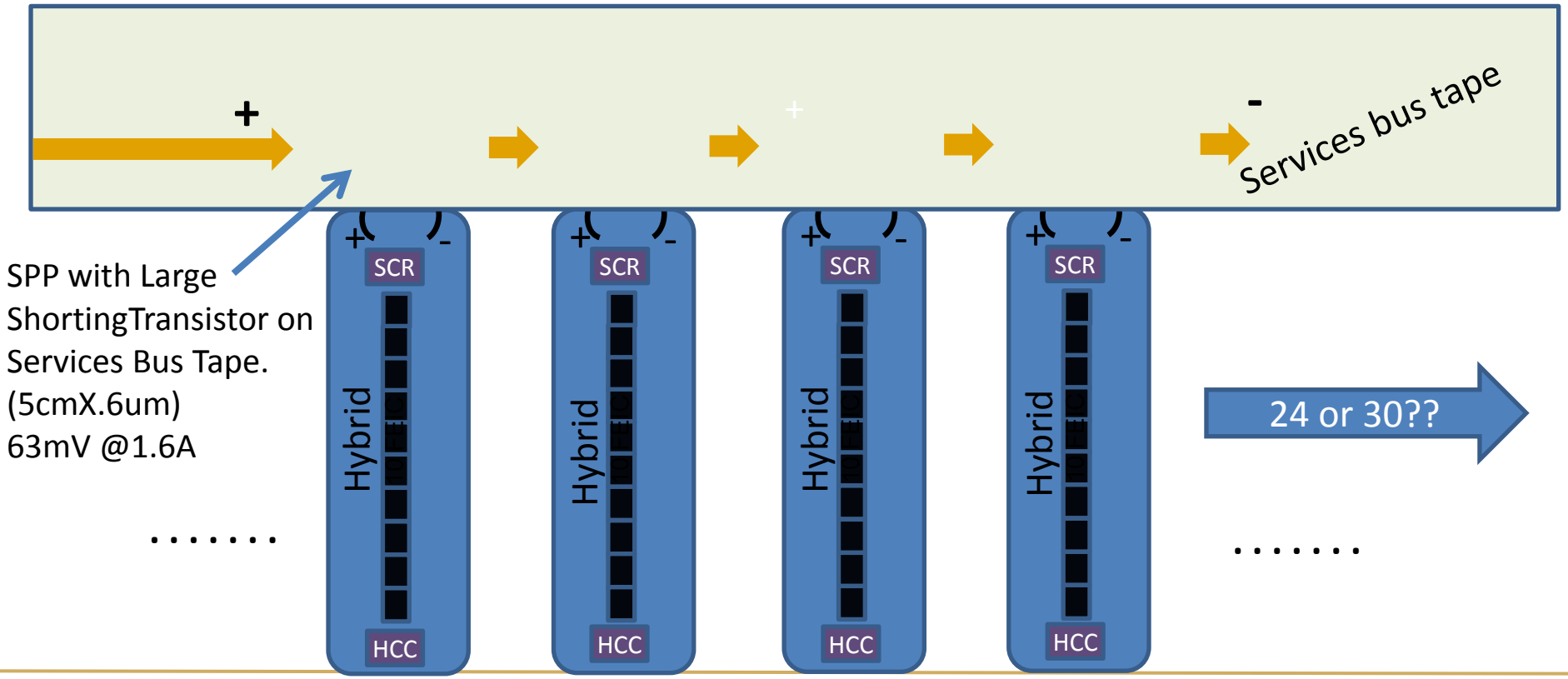






One "Final" Envisioned Serial Power Architecture

- **SPP directly attached to stave bus**
  - **Single Global power line supplies each SPP with independent power**
  - **SPP is addressable to turn "on" and "off" a hybrid.**
  - **Built in Transistor capable of shunting hybrid current independent of ASIC based shunt transistors**
  - **Includes serial power regulator and SCR circuit for overvoltage protection**
- **Extra SCR on each hybrid in case of SPP failure**
- **Shunt with LDOs in each ABCn to generate analogue/digital voltages**



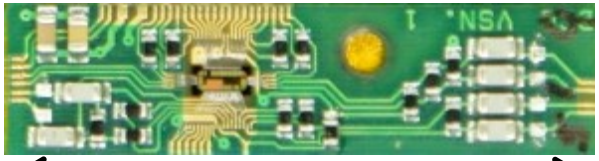
Material Estimate for Serial Power

Using currently understanding, the radiation length of material needed to service power has been estimated

– Excludes extra bus tape traces, support, traces

Goal of *less than 2%* for a stave's radiation length

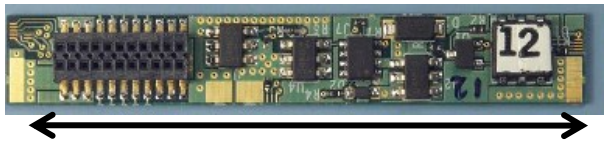
- Serial Power: 1 shunt per ABCN, 1 control and 1 protection ASIC per hybrid
  - Estimate 0.03% of a radiation length to stave from serial power
    - Mostly from extra needed hybrid area and AC-coupling capacitors



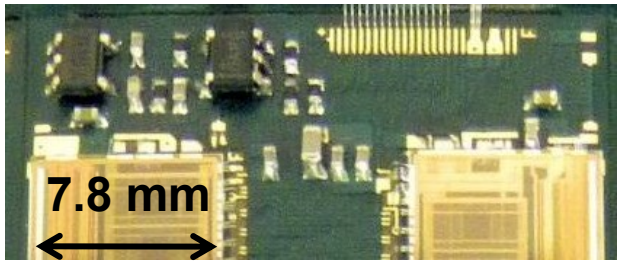
24 mm

BCC replaced by bare die hybrid control chip (HCC) on each hybrid. 10 extra 0402 capacitors need for AC coupling clock/command/trigger

Discrete serial power protection will be replaced with custom ASIC (3 mm^2), 1 1206 resistor, and 4 0402 capacitors



~35 mm



7.8 mm

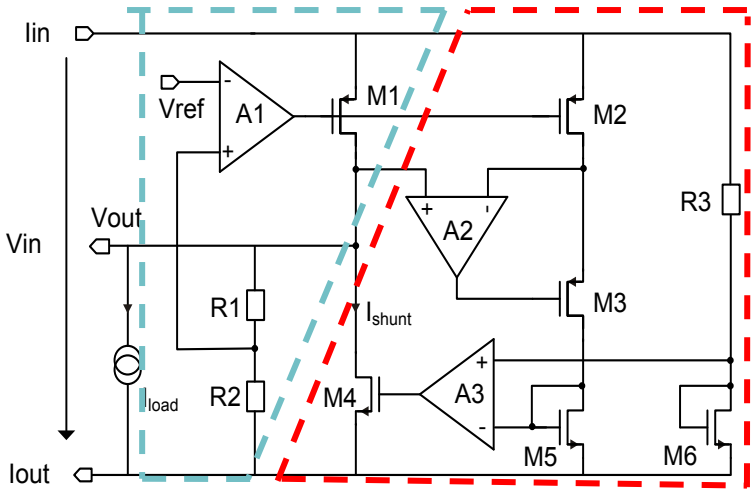
Discrete shunt control on current hybrid will be replaced with custom ASIC (9 mm^2), 2 0805 resistors, 2 0402 capacitors

Strip Serial Powering Conclusions

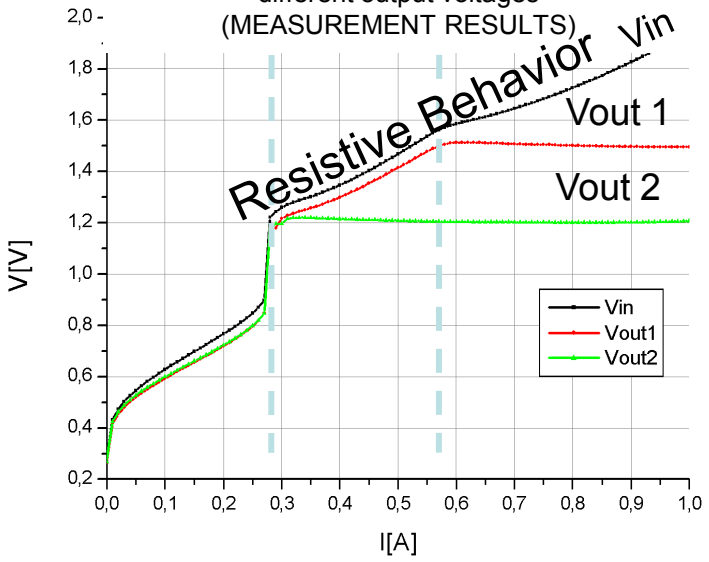
- All technology needed for SP has been prototyped and shown to work (and compatible with 130 nm CMOS)
  - Remaining concerns are locations of devices and number of units in a SP chain (concerned with both common mode build-up and failures)
- Largest continuous current channelled through any one ASIC will be les than 200 mA
- Largest power dissipation in SP control/protection ASICs is less than 50 mW
- Hybrid voltage regulation will have several amps of reserve current handling
  - Have shown up to 10 A in a hybrid
  - Allows flexibility for set voltages/currents
- Minimal impact on material budget
- Last bit for ultimate noise performance still under study
  - But measured noise would yield 15:1 S/N at end of life

ATLAS Pixels SP Shunt-LDO

- **Combination of a LDO and a shunt transistor**
  - Shunt transistor is part of the LDO load
  - LDO power transistor works as an input series resistor for the shunt
- **Advantages for Serial Power**
  - Removed input series resistor for shunt improves power efficiency
  - Shunt-LDO regulators can be placed in parallel without problems regarding mismatch & shunt current distribution
  - Shunt-LDO having different output voltages can be placed in parallel
  - Shunt-LDO can cope with an increased supply current if one FE-I4 does not contribute to the regulation
  - Failed regulator loses one ASIC instead of one hybrid
- Working principle and good performance demonstrated with 2 prototypes already
  - 130 nm MPW
- Nominal Power Efficiency of 2 Shunt-LDO in parallel with different V_{out} = 75%

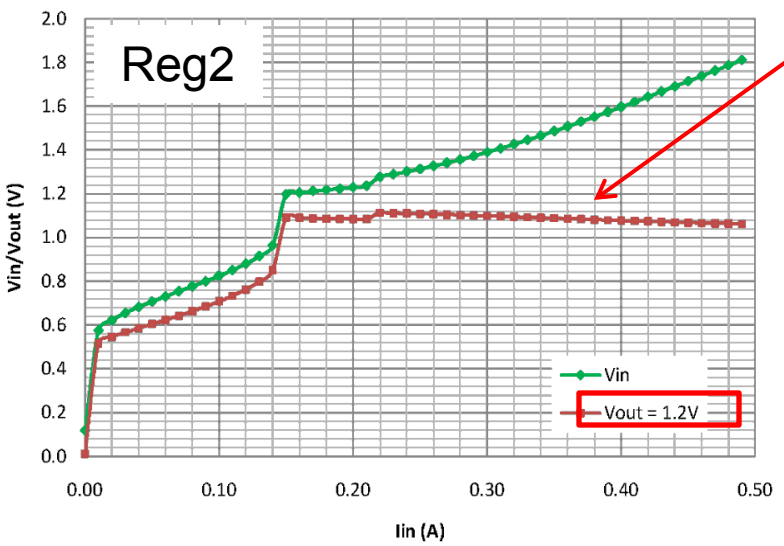


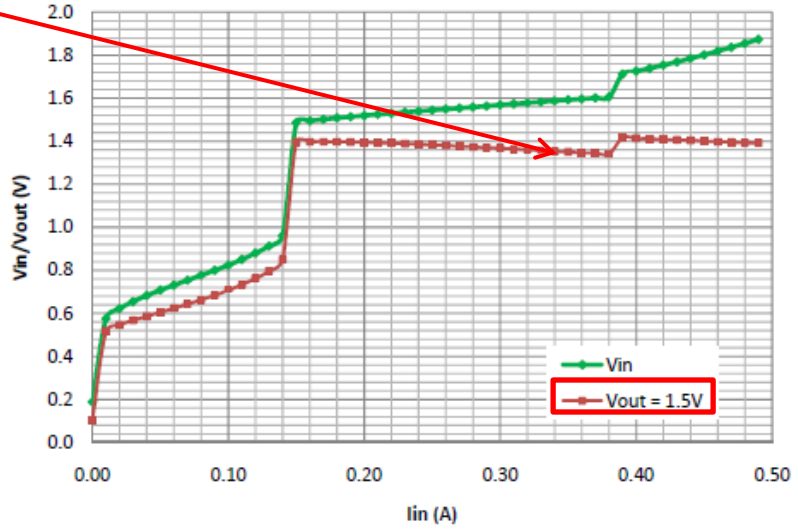
V-I characteristic of 2 Shunt-LDO in parallel @ different output voltages (MEASUREMENT RESULTS)



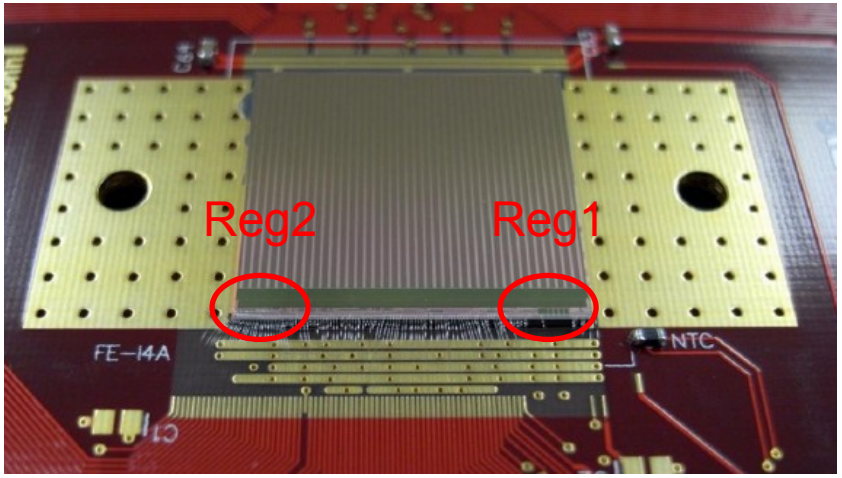
FEI4 Pixel ASIC

Voltage drop between chip and board ground



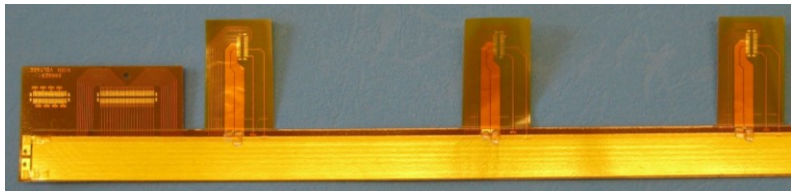


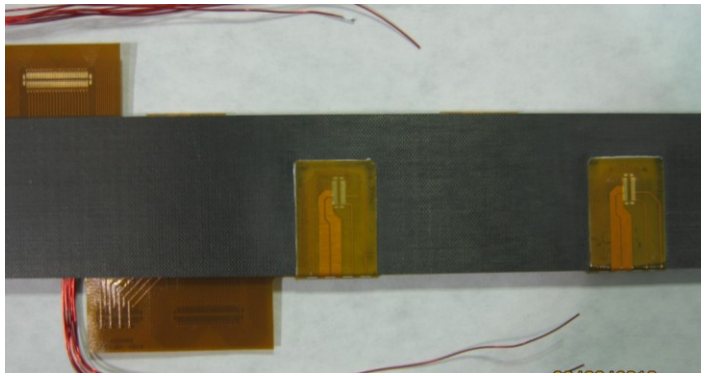
- Prototype FEI4 ASICs and packages undergoing first testing now
- So far, Shunt-LDOs working as expected



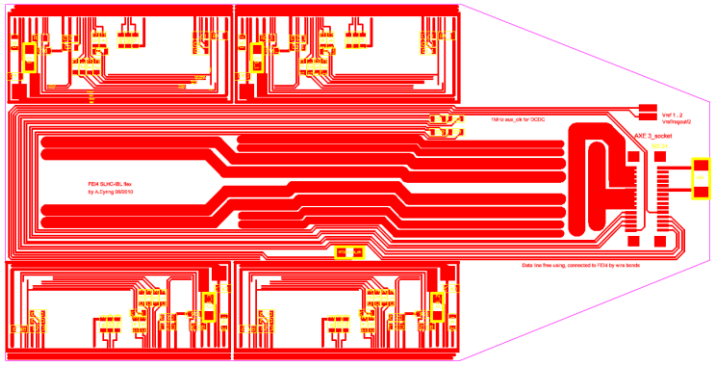
Phase II FEI4 Serial Powered Pixel Modules

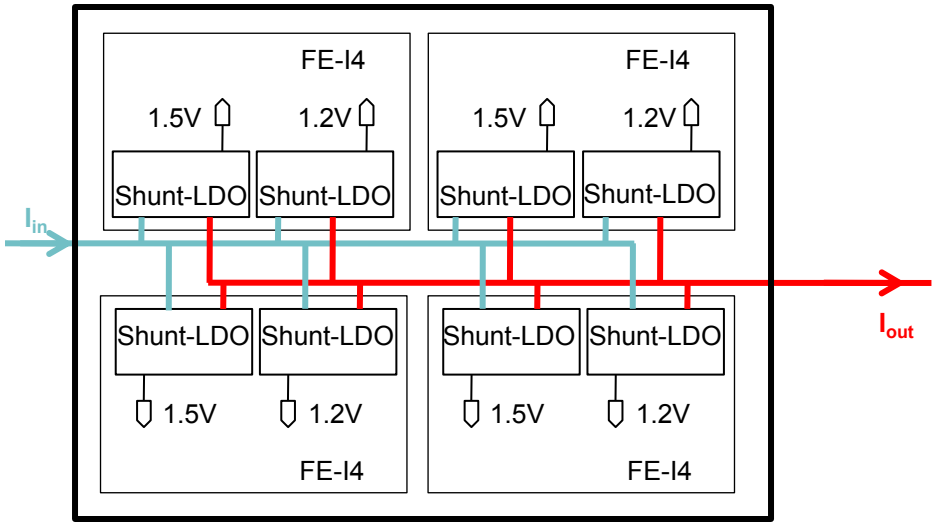
- Cable prototype for serial power has made
  - 8 modules in chain on a stave
- At module level, the current is routed in parallel to the 4 FE-I4s
  - Prototype module flex in production
  - I = Imod = 2.4A (max)
- 2 Shunt-LDO/FE to generate VDDA = 1.5 V and VDDD = 1.2 V per ASIC
- 8 Shunt-LDO regulators per module in parallel





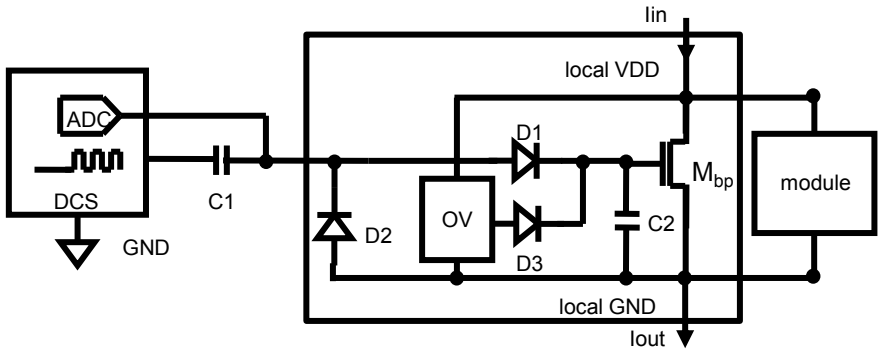
Module flex



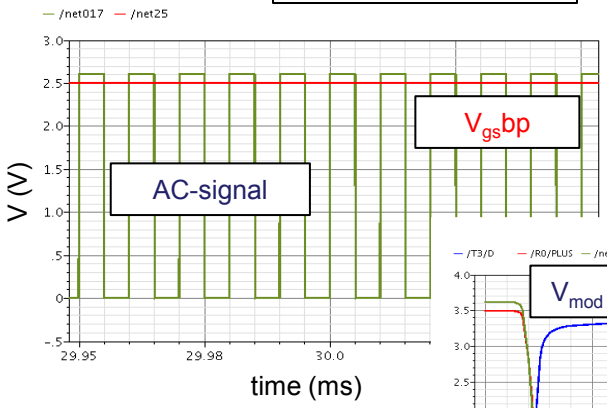


Pixel Module Protection Chip

- Chip ASIC in design
  - 130nm IBM
  - Bypass transistor
- Independent slow ctrl line & OV protection
  - OV protection = Silicon controlled rectifier
- Preliminary simulations:

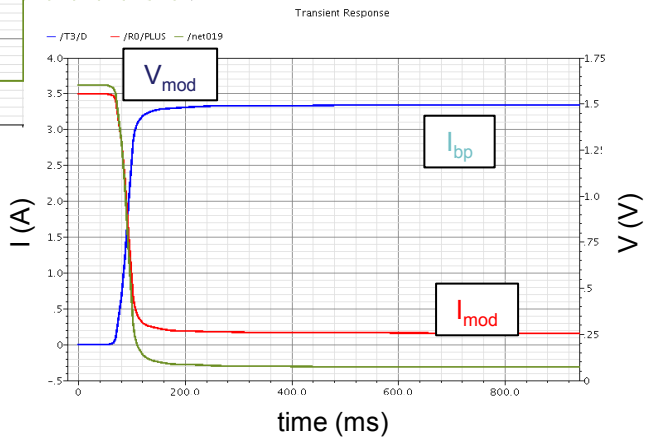


Slow ctrl



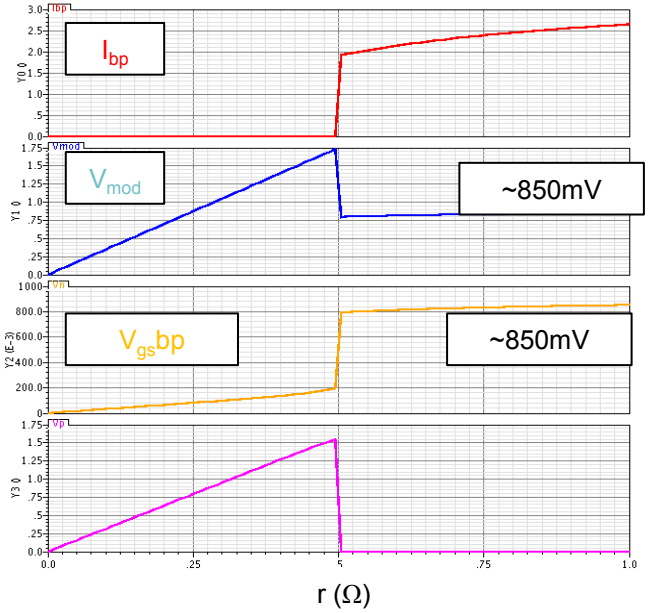
Bypass

DGNMOS
W = 48mm
L = 0.24µm



C1 = 100nf
C2 = Cgs = 33pf
D1, D2 = PMOS

Fast response



Conclusions

- Modification of power schemes necessary for SLHC Silicon Systems
  - Much high segmentations and larger areas
- Serial powering has been shown to be a viable option
  - Low mass, higher power efficiency, simple, flexible
- Two different systems are under test for ATLAS pixels and strip detector systems
  - So far, all results are positive
  - Still in serious consideration for final system

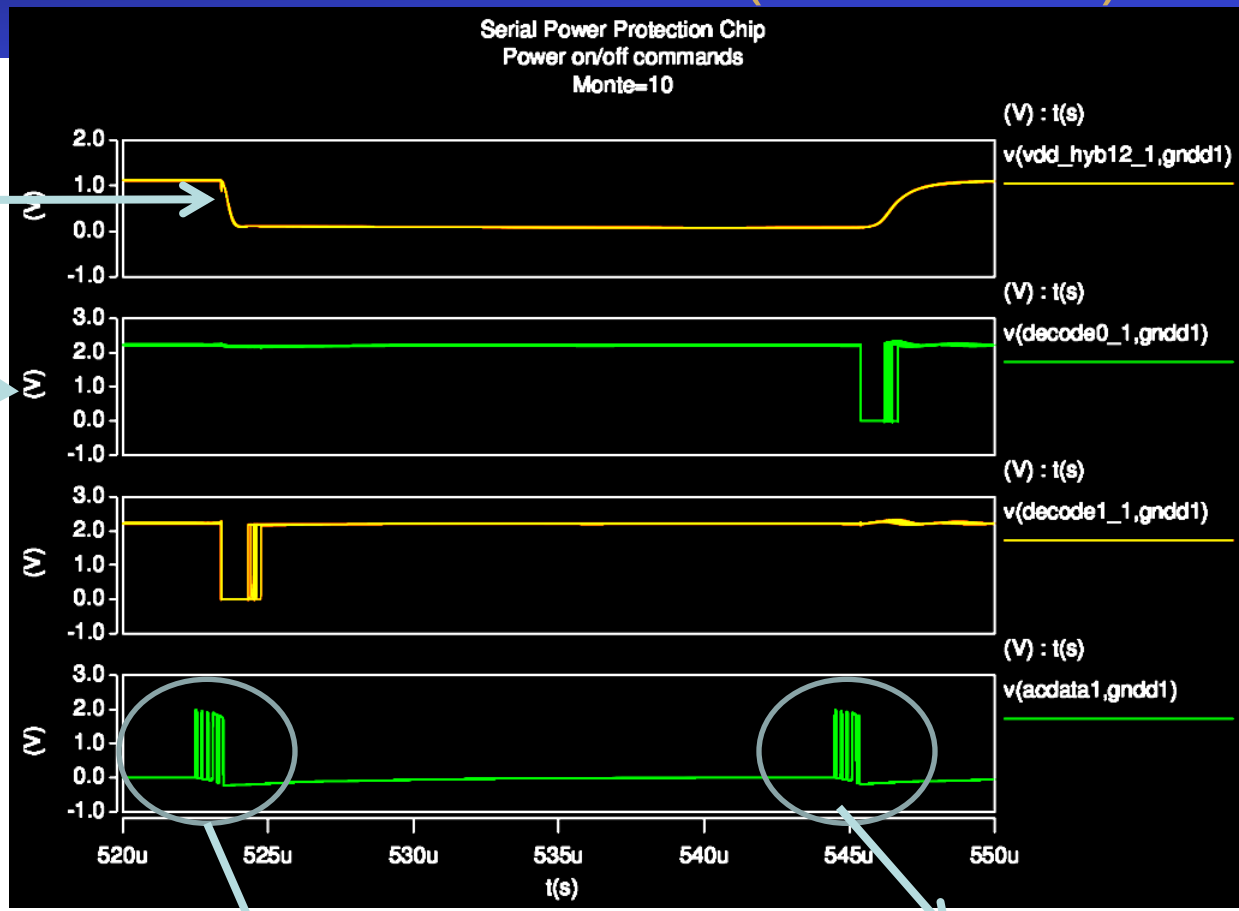
BACKUP MATERIAL

SPP – 12 Hybrid HSPICE simulations (Monte=10)

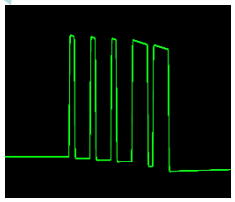
Hybrid voltage (1.2v)
80mv when shorted

Decode 0:unshort hybrid

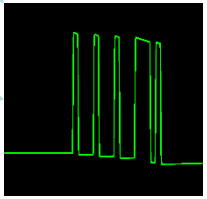
Decode 1: short hybrid



Decode 1: short hybrid



Decode 0: unshort hybrid



SPP – 12 hybrid HSPICE simulations (Monte=10)

Vglobal (25v) SPP pwr

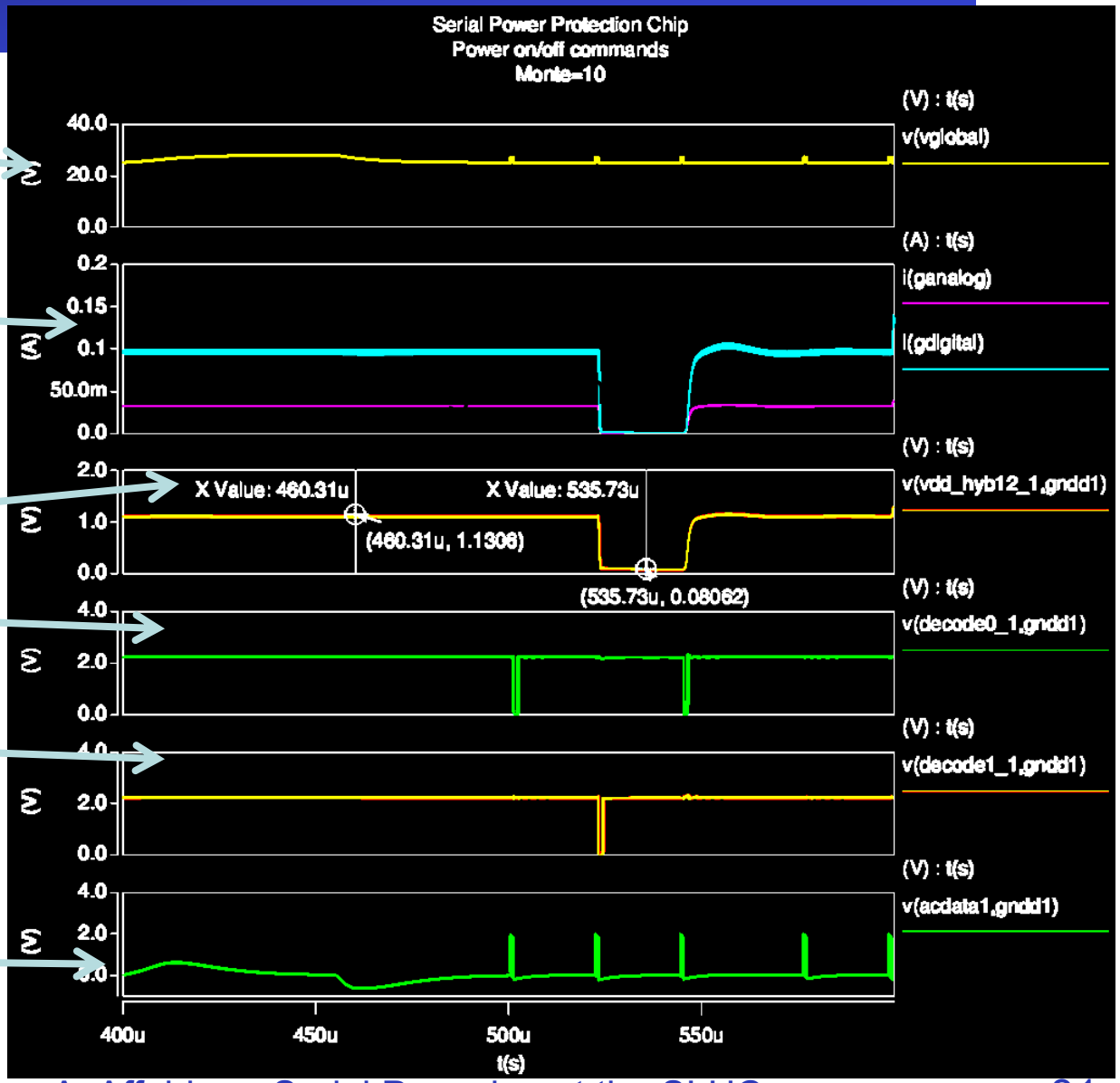
Load Current in one FE IC

Hybrid voltage (1.2v)
80mv when shorted

Decode 0: unshort hybrid

Decode 1: short hybrid

AC coupled pulse-width modulated signal



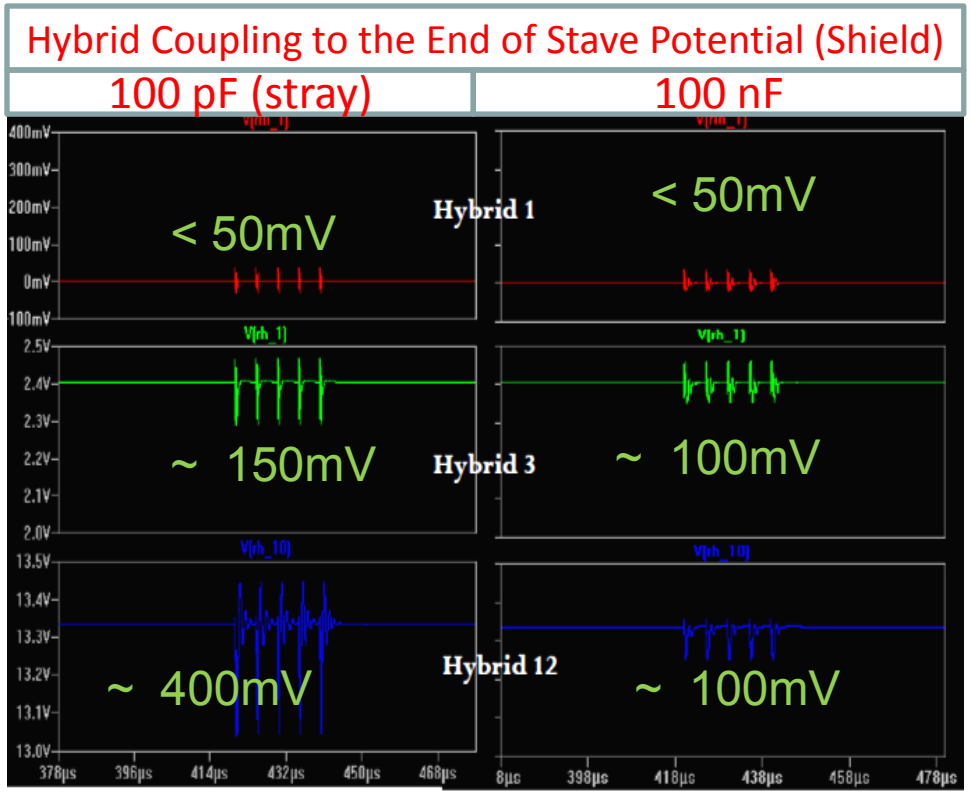
Scaling up the Serial Powered System

The length of the SP chain and it's reverence connections needs careful examination under dynamic conditions as we begin to scale up from one module towards a full stave

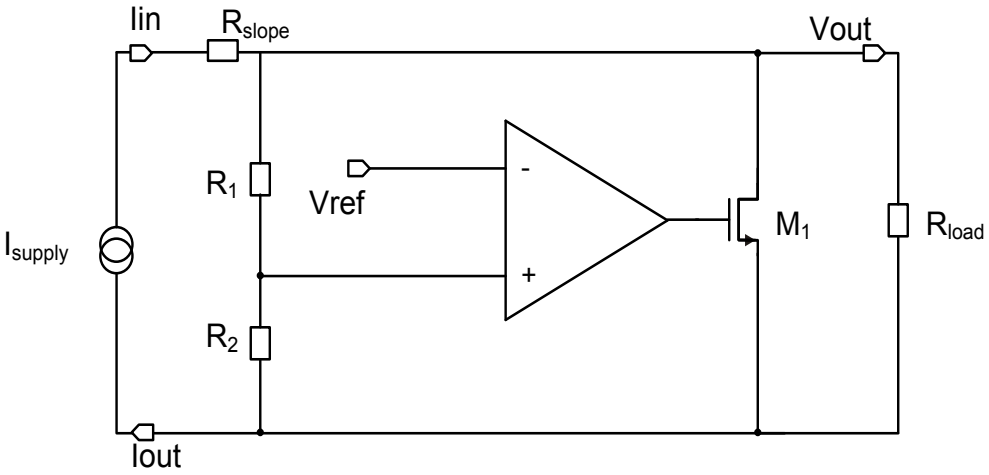
The plot on the left shows a simulation result for a 12 hybrid SP loop when L1's are being issued (modeled as a 20% increase in digital current for all ABC chips.) The plot shows the local hybrid reference vs EOS ground. This represents one source of common mode noise in the digital signaling between the EOS and Hybrid. These simulations show a significant the potential for a growing common mode signal as the length of the SP chain is increased.

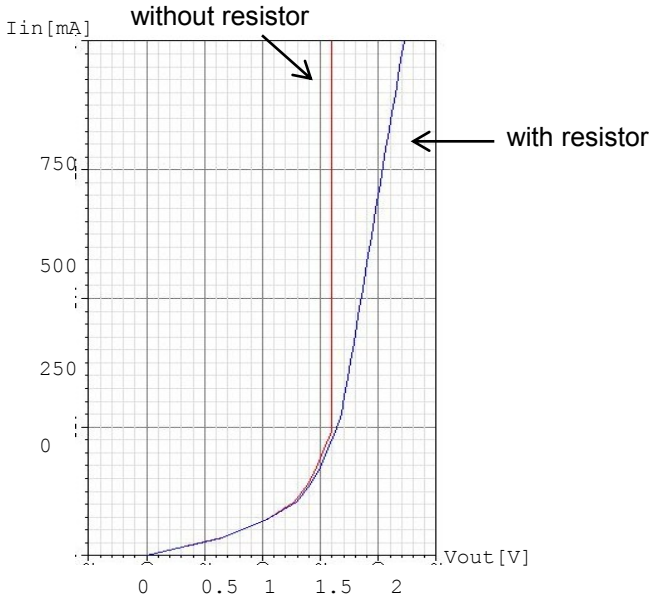
Simulation results

Common Mode for Hybrid to EOS Signals



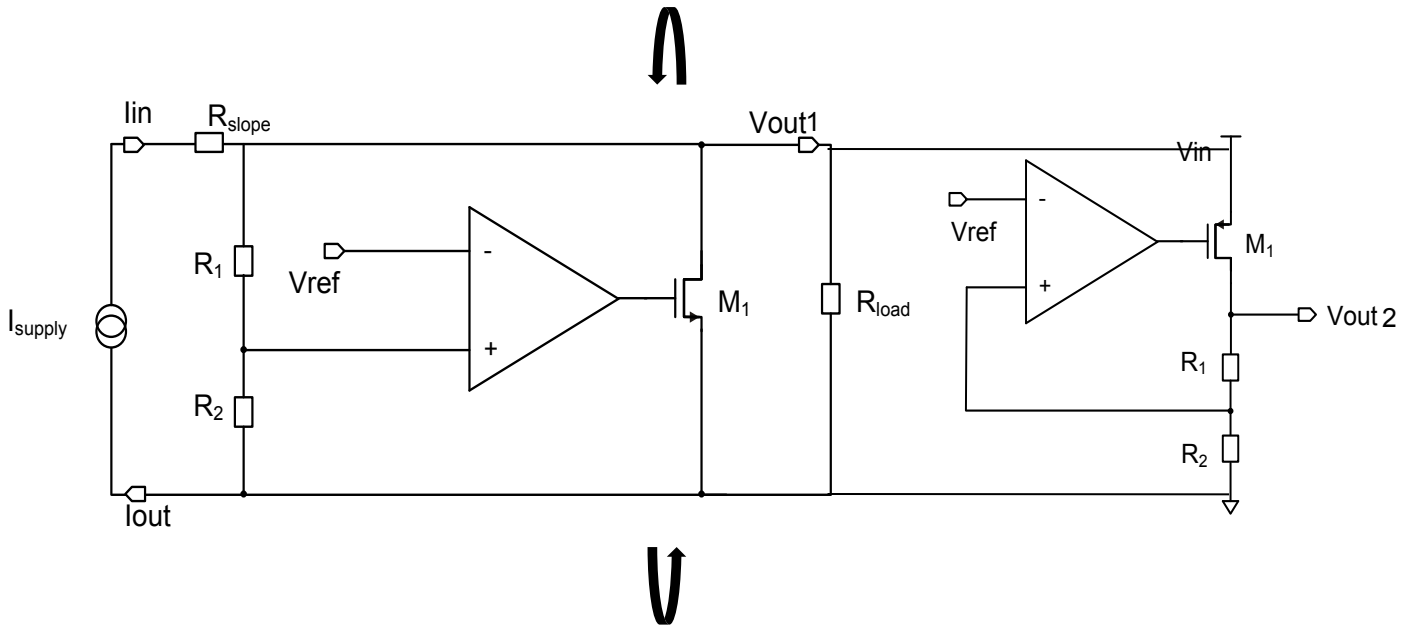
Shunt Regulator (FE-I3 approach)





- Shunt regulator generates a constant output voltage out of the current supply
- current that is not drawn by the load is shunted by transistor M1
- Very steep voltage to current characteristic
- Mismatch & process variation will lead to different Vref and Vout potentials
- Most of the shunt current will flow to the regulator with lowest Vout potential
- Potential risk of device break down at turn on
- Using an input series resistor reduces the slope of the voltage to current characteristic

LDO Regulator (FE-I3 approach)



• Second supply voltage of lower potential is genareated by a LDO regulator powered by the shunt regulator

• The LDO power transistor operates like a regulated series resistor which controls the voltage drop between input output voltage to have a constant output voltage

• Change order of regulation chain

• R_{SLOPE} replaced by the LDO power transistor

• Shunt transistor connected to the LDO output

Shunt Regulator Architectures

- **Hybrid with Shunt "M"**

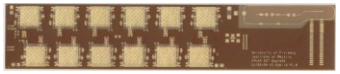
- Use one external shunt regulator
- Use each ABCN's integrated shunt transistor(s)
  - Two (redundant) shunt transistors, 140mA each

Each option has its merits. All now available in silicon: final choice to be based upon test results.

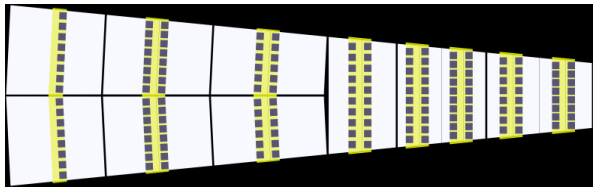
Science & Technology Facilities Council

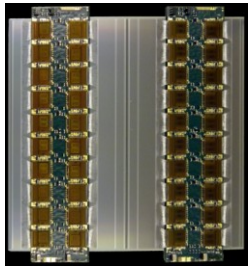
Stave+Petal Programme

- Collaboration of more than 25 institutes from 5 countries
- Designed to minimise material
  - Early electrical systems tests needed to determine which mass-saving changes possible
- Requirements of automated assembly built in from the start- *Simplify build as much as possible!!*
- Minimize material in thermal management by shorting cooling path- Gluing module to a stave core with embedded pipes
- Design aims to be low cost- *Minimize specialist components!*

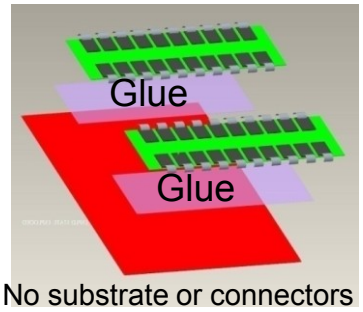


Petal Hybrid

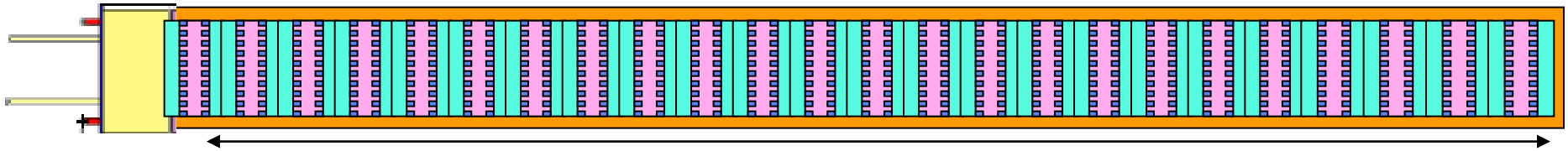




Stave Module



No substrate or connectors



~ 1.2 meter