DCDC converters for the upgrade of the LHC experiments

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Information on the development, and datasheets, can be found in the public web page of the project:

http://cern.ch/project-dcdc

Motivation for the development of radiation and magnetic field tolerant DCDC converters

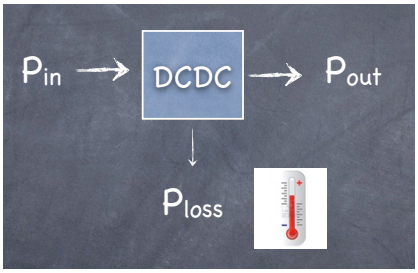
Electronics installed in the LHC experiments is typically powered directly from power supplies (PS) located remotely in the experimental cavern or even farther. Current required by the FE circuits flows in the long cables from the PS and originates losses equal to RI^2. To reduce them, the cable R has to be made small - but this comes at the cost of material (large cables). When material can not be used, cables have to be made thinner at the cost of larger power dissipation - hence larger requirements on the cooling system.

For LHC upgrades, in particular for the trackers, it would be beneficial to modify the power distribution such that thinner cables can be used along all the current path. This is particularly true since we are aiming at a larger number of readout channels, possibly increasing the total power requirement of our systems.

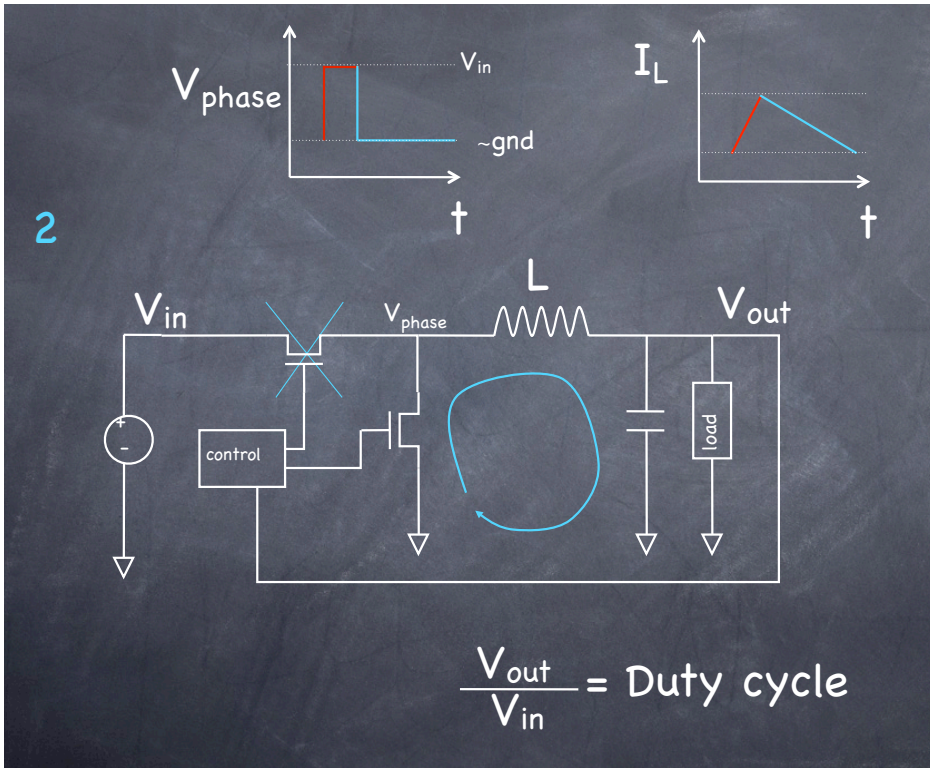
One possible approach is the distribution of power in the form of a higher voltage, which is locally (on-detector and actually on-board) converted to the lower voltage required by the FE electronics. To distribute the same power, a higher voltage means a lower current (P=VI) and therefore smaller losses on the same or even thinner cables. The conversion is performed by DCDC converters. Since these converters are placed on-board, they are exposed to the same environment as the FE circuits: magnetic and radiation fields. Such components can not be found in the marketplace and have to be custom developed. An R&D activity started in CERN-PH officially in 2008.

How a DCDC converter works, and what makes our converters different than those available in the marketplace

A DCDC converter transforms a DC input voltage into a DC output voltage. In our case, we need a step-down converter ($V_{in} > V_{out}$). The simplest and most widely used type of converter is called ‘buck’. After a study of the different converter’s topologies, we concluded that this is indeed the best converter for our application since it allows to minimize the size and complexity, still yielding high efficiency. Efficiency is the ratio between ouput and input power (P_{out}/P_{in}). The difference P_{in}-P_{out} corresponds to the losses inherent to the converter’s operation, and we struggle to minimize them.



Converters are switching circuits: they cyclically operate at a frequency (fixed for the Pulse Width Modulation -PWM- converters like the one we are developing) and their duty cycle D determines the conversion ratio V_{out}/V_{in}. Buck converters use an inductor to store energy and filter a switching voltage to provide a DC output voltage. Energy is transferred from V_{in} when one of the two main switches (the 'high side' MOSFET transistor) is turned on, for a fraction D of the switching period. So the step-down conversion can be seen as a periodic transfer of energy from a source (V_{in}) to a constant DC V_{out} which is regulated by an internal control loop (whose function is to decide the duty cycle D).



Buck converters can be widely found in the marketplace. They use ferromagnetic inductors and commercial-grade semiconductor processes, without any precaution to protect them agains radiation. With ferromagnetic cores, inductance values of several uH can be used while keeping the parasitic resistance of the inductor very small (less than 10 mOhm). Ferromagnetic cores unfortunately saturate in the magnetic field of the LHC experiments, and in our application we necessarily need to use coreless (or air-core) inductors. Without the ferromagnetic core, the inductor requires many more turns to yield the same inductance, meaning a much longer wire needs to be wound. This leads to much larger parasitic resistance, and larger volume. To limit somehow these drawbacks, we limit the inductance value to below the uH - we choose 200-500 nH. This in turn determines a higher switching frequency for the converter - 1 to 4 MHz.

The second fundamental difference from commercial products is that our converter is designed to survive to the HL-LHC trackers radiation environment. The semiconductor technology choice is determined by this requirements, and dedicated design and layout

provisions are followed to ensure protection from cumulative and Single Event radiation effects. Our final production-grade converter will be qualified for radiation effects.

What are the components of a full DCDC converter. Do we have them all by now?

The full DCDC converter we are developing is a small plug-in PCB engineered to meet the typical specifications of HL-LHC experiments. They include:

Electrical specs

Input voltage	10-12V
Output voltage	1.2-3.3V
Output current	up to 3A*
Efficiency	>80% (for V_{out}=2.5V)
Conducted and radiated noise compatible with installation in close proximity to FE electronics and detectors	

* We will know the real output current limit soon, with measurements of a mature ASIC in a realistic configuration (cooling)

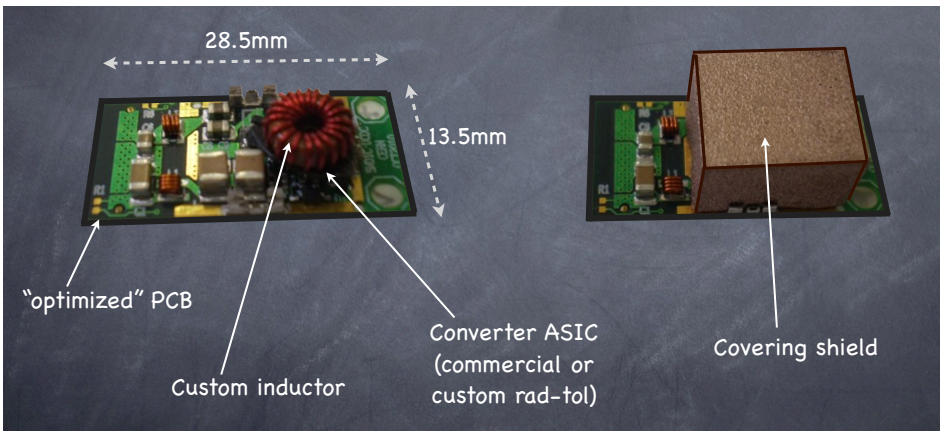
Mechanical specs

Small size (footprint, height)
Small contribution to material budget
Connectable to cooling system

Environmental specs

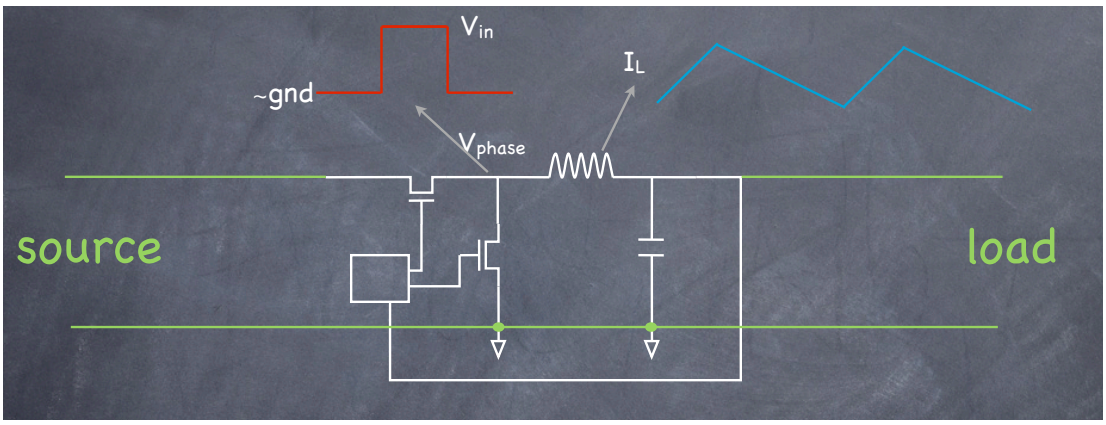
TID tolerance	250 Mrad
Displacement damage	$2.5 \cdot 10^{15}$ n/cm^2 (1MeV equivalent)
SEE	Absence of destructive SEEs and Vout transients when tested with heavy ions up to an LET of 30 MeVcm^{2}mg^{-1}
Magnetic field	4 T
Temperature of cooling pad	-30 to +10 °C

Prototype DCDC converter PCBs satisfying part of these requirements have been produced already. Some of them use a commercial DCDC integrated circuit which will be replaced by our radiation tolerant ASIC in the final version. An example, with its main components detailed, is shown in the figure below. The status in the development of the main components is summarized in the table below.

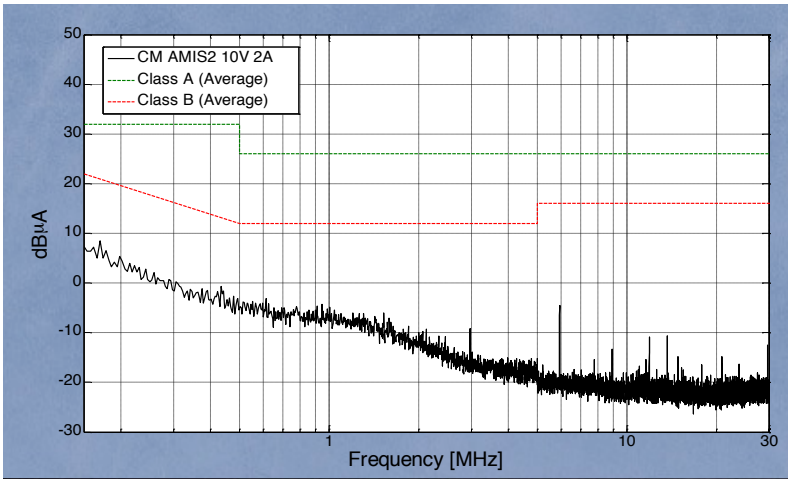


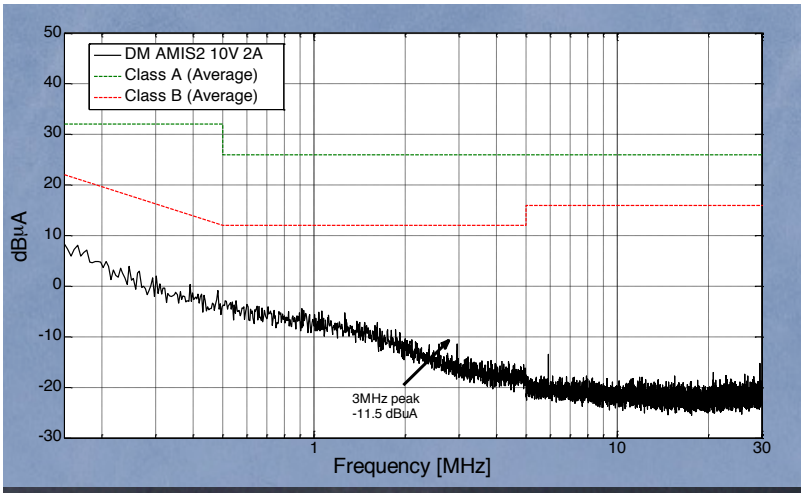
Rad-tol ASIC	Custom air-core inductor	Shield
An adequate radiation-tolerant CMOS technology has been found. It is a 0.35um offering N-channel LDMOS rated to 14V Vds. Radiation tests for both TID, displacement damage and SEEs have been passed.	The inductor design better suitable for our application has been selected: an air-core toroid custom wound. The air-core topology allows containment of the main magnetic field (low emission).	To achieve the ultimate low noise performance, all 'noisy' components of the DCDC are segregated inside a shield. One side is the gnd plane of the PCB, while a custom cover is placed on top of the PCB to cover selected components.
Prototype designs have been produced in 2 CMOS technologies. Measurements validated the chosen topology. A prototype in the selected technology - called AMIS2 - passed all radiation tests and has already been used for detector systems' tests.	The design has been finalized with industry (Coilcraft). Materials used in the construction have been verified for radiation effects. The component is available for series production.	Different shield constructions are being studied to find the most efficient and more suitable for our application (sufficient E and H field attenuation, low mass).
An ASIC complete with all protection features is in production now (called AMIS4). If successful, minor modifications will be done before the end of 2011.		Final shield is expected to be selected within a few months.

The PCB design is finalized and allows meeting the noise requirements. If we remember that the 'phase node' in between the two switching transistors swings between about gnd and Vin at every cycle, we understand the challenge of preventing this voltage noise to propagate in the system. Additionally, the largely varying current in the inductor is another source of EM noise. All noise generated by the switching shall not propagate to the system towards the source or the load of the converter. This could happen via conduction (conductive noise) or EM emission.



The PCB has been optimized to prevent noise propagation with several techniques: layout, component choice and placement, identification and segregation of noisy components, shielding, addition of input/output filters. The best results, obtained on a prototype board using a rad-tol custom ASIC, are shown below. The top one refers to Common Mode, the second to Differential Mode conducted noise. This is noise conducted along the power cables (differential circulates in a loop where power cable is one way and gnd cable the return; common mode in a loop where the pair power+gnd cable is one way and the return is some parasitic path in the system). The curves show the noise measured in uA (0dBuA=1uA) on the output cable - the one from DCDC to the load. The continuous line is the background noise of the measuring instrument. The peaks are the noise signals: the main component at the switching frequency and then the harmonics. They are all well below the CISPR11 Class B limit, evidencing an excellent performance.



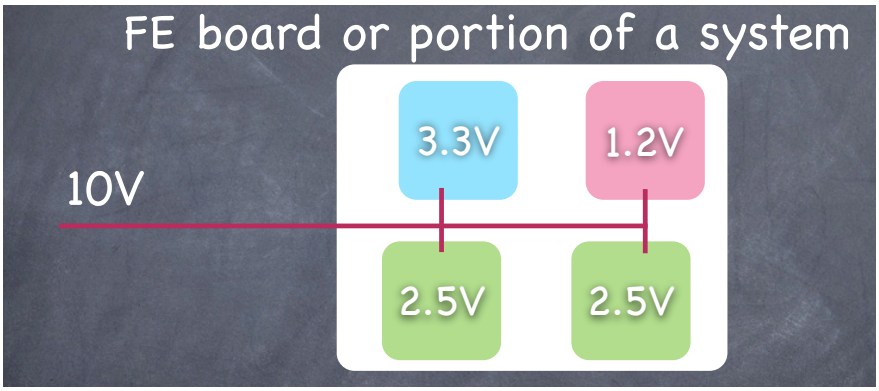


The compatibility of the DCDC prototypes with installation in close proximity of the FE electronics has been demonstrated in measurements done on the prototype ATLAS SCT tracker modules, and on CMS HCAL FE cards.

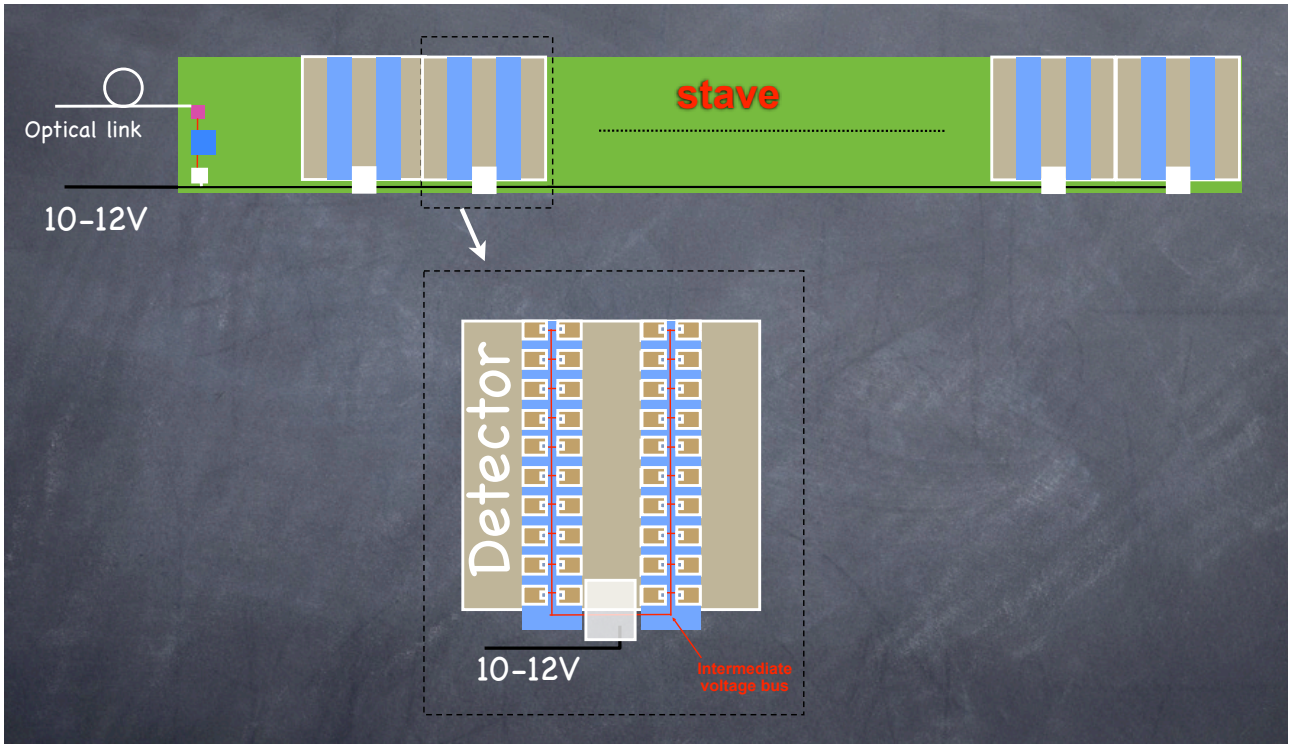
In summary, what can a DCDC converter bring to a HEP experiment's system

The main motivation for the development of the converter is the possibility to distribute power at a higher voltage, hence the need to push smaller current in the cables connecting the FE electronics to the power supplies. This translates into thinner cables, or more power transferred in the same cables. Moreover, the DCDC installed on-detector adds local regulation in proximity to the load.

Once rad-tol and magnetic field tolerant converters exist, it is possible to use them to build a modular power distribution system where the power is distributed as a single 10-12V line. From this line, local DCDC converters can provide power at different voltage to segmented power domains.



An example from a possible architecture of a tracker stave is shown below. A single 10-12V line powers the full stave. Represented as white squares, DCDC converters provide the required voltage to the optical components at the end of stave (left) and to every single module. On module, the converter provides an intermediate voltage bus at 2.5 or 1.8V. A second conversion stage, embedded on the FE readout ASICs as a switched capacitor converter, takes power from this bus and converts it to the 1.2 or 0.9V for the analog and digital portions of the ASIC.



The modularity is useful to isolate the loads or the portions of the system/board, so that they can be separately turned on/off (easy turn-on and turn-off procedure for the full system without large current surges, easy turn-off of defective portions to prevent disturbances to the rest of the system).

As an additional information for possible application in power pulsing, system-level behavioral simulations targeted at the CMS pixel upgrade in phase1 show that the present version of DCDC converters can be turned on (and off) in about 2ms. This is the time pre-set for the soft-start procedure which ensures the absence of excessive currents at startup. This time is necessary if the output voltage is drop to 0, while the converter answer to a transient in the output current is much shorter (100-200us).