EMI aspects for systems with train cycled operation: CALICE-AHCAL

EMI: electro magnetic interference

Cycle : power gets ON and OFF ?

Systems: signal chain from sensor to power supply

CALICE-AHCAL: as example the analogue hadron calorimeter

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For CALICE collaboration
DESY
Orsay, May, 9th/10th, 2011

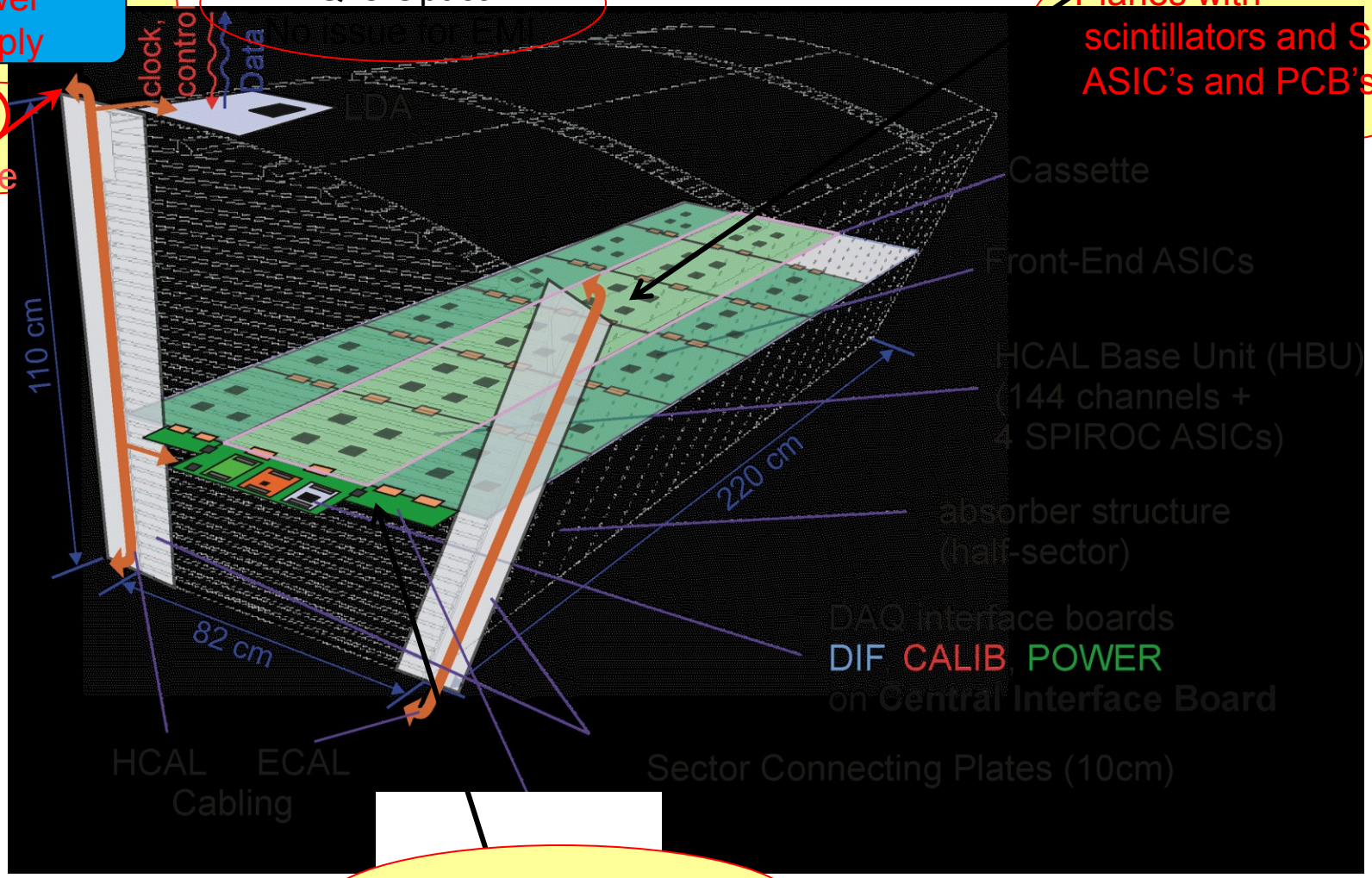
HELMHOLTZ ASSOCIATION

DESY

Outline

- CALICE-AHCAL: View of power/EMI/grounding
- General issues for EMI in a system
- The design chain of a system
  from frontend to power supply
  - The layer with the sensors
  - The end of layer region
  - The cable to power supply
  - Power supply
- Summary

CALICE-AHCAL: Design in a few words



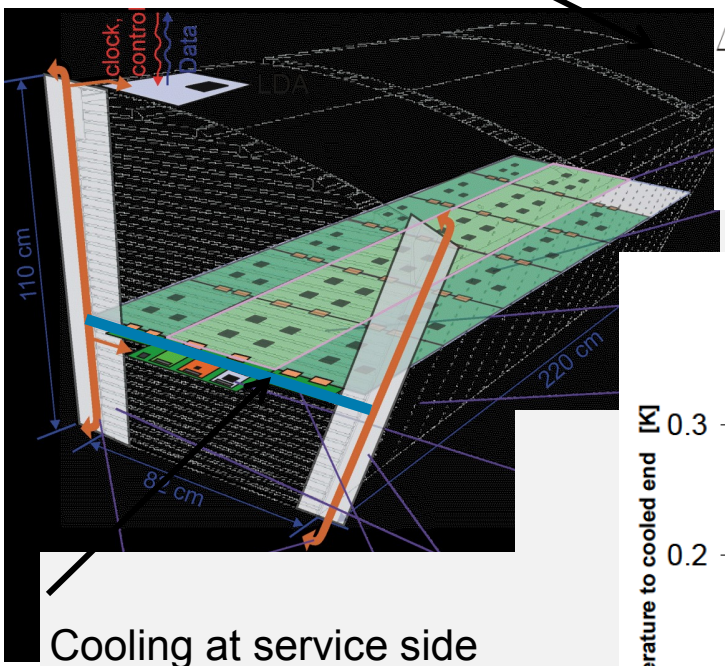
CALICE-AHCAL: Why power cycling?

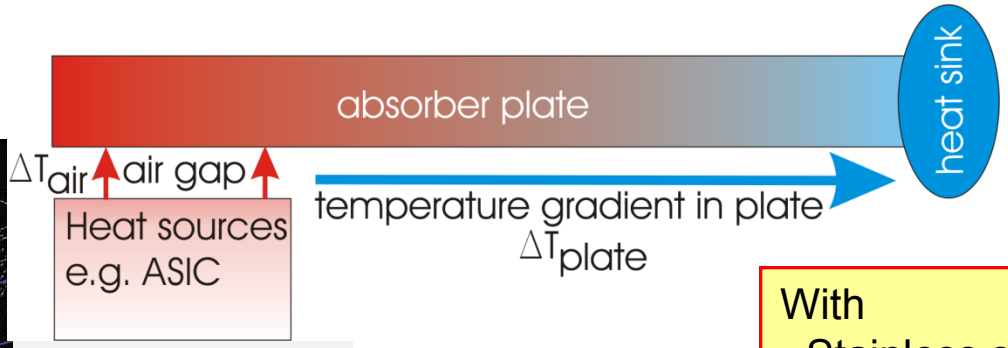
See : P.Göttlicher, TWEPP07, Prague, proceedings

Simplified model:

- No heat transfer radial
  "bad due to sandwich"
- Cylindrical symmetry
- Symmetry at IP-plane

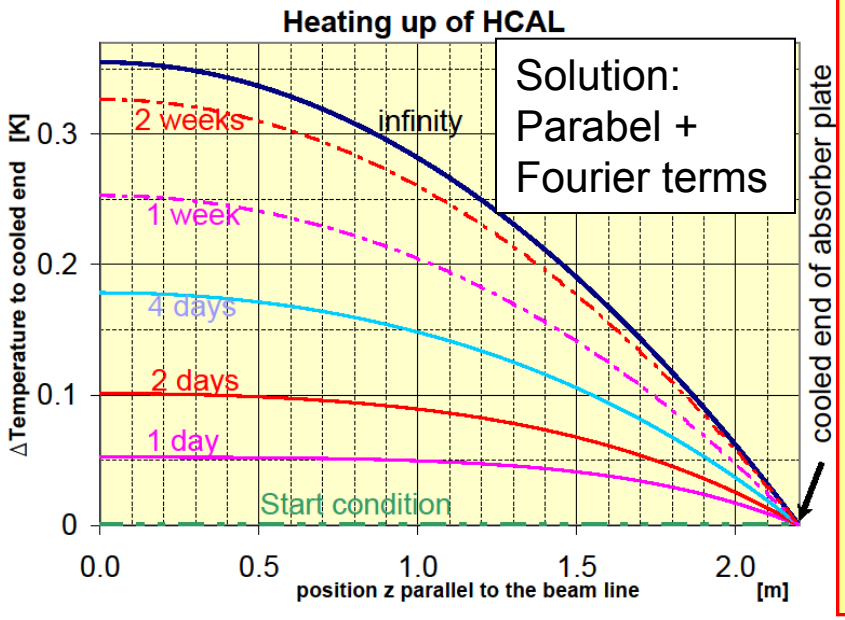
$$\frac{\partial T}{\partial t} = \frac{1}{heat\ cap./area}\frac{power}{area} + \text{heat conductivity}\ \frac{\partial^2 T}{\partial z^2}$$





Cooling at service side

- No cooling within calorimeter to keep homogeneity and simplicity



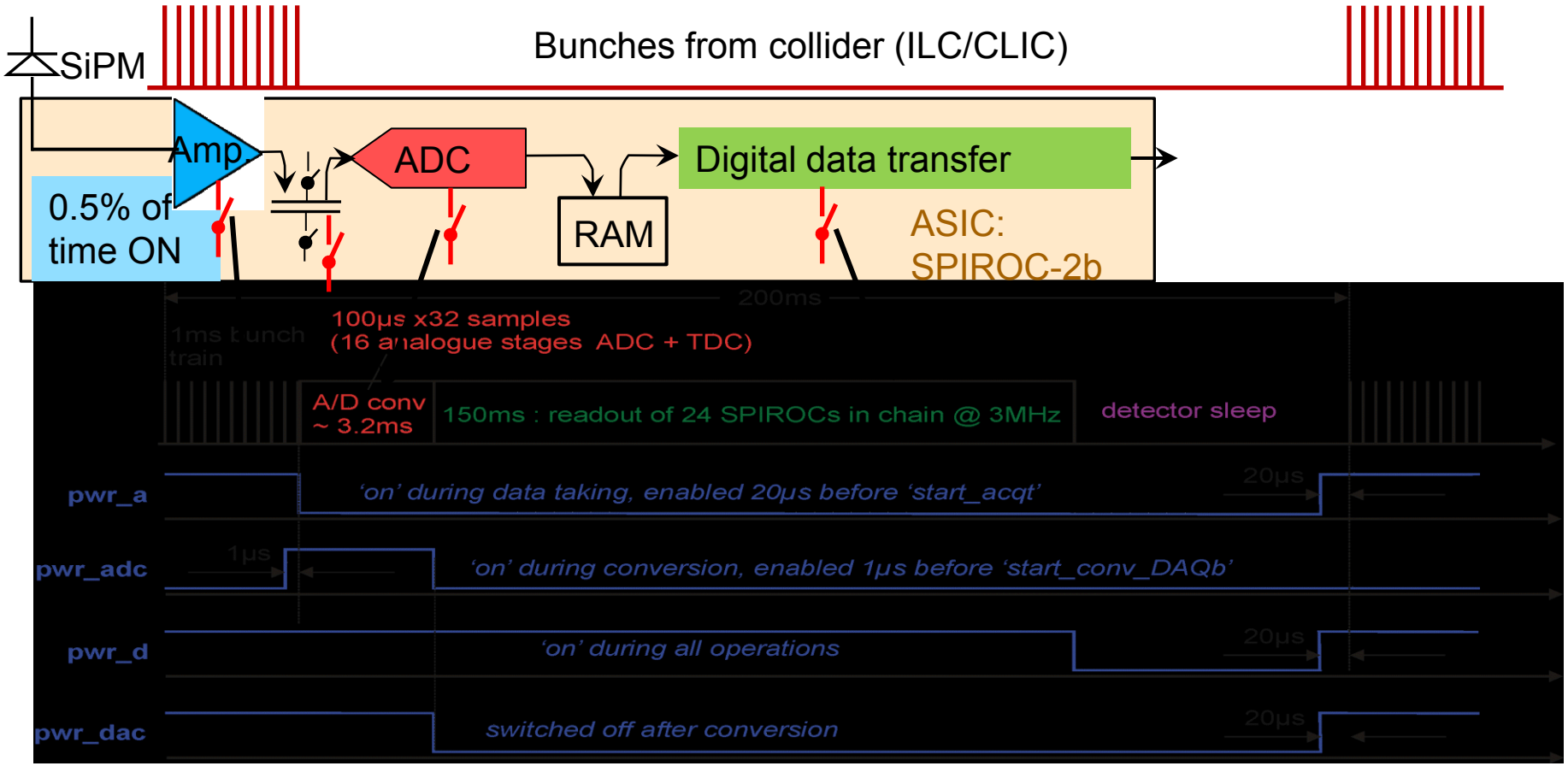
With
- Stainless steel
- Long structure

Electronics power of 25µW/channel
+
SiPM-dark current 15µW/channel

⇒ **Need power cycling**
When no need switch OFF: 99%@ILC

CALICE-AHCAL: ASIC for power cycling

L. Raux et al., SPIROC Measurement: Silicon Photomultiplier Integrated Readout Chips for ILC, Proc. 2008 IEEE Nuclear Science Symposium (NSS08)

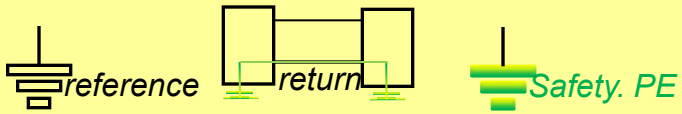


Algorithm for CALICE-AHCAL:

The ASIC **switches the current** of the functional blocks OFF.
ASIC gets supplied **all the time with voltage**.
PCB electronics and instruments **stabilize the voltage**

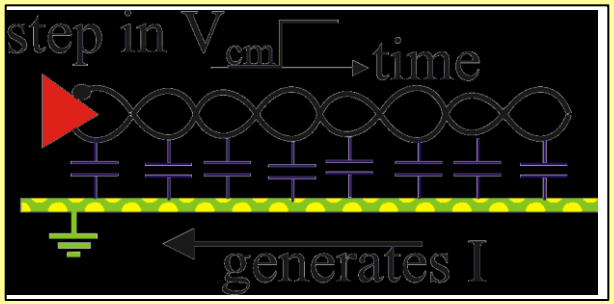
General issues for EMI in a system

Reference ground:



- Need good definition
- Any induced/applied current produces voltage drops
- Separation between reference / power return / safety or controlling currents and keeping currents within “own” volume and instrumentation

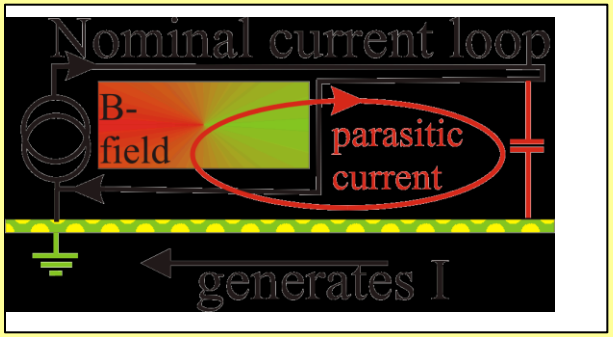
Capacitive coupling



To do:

- Keep common mode voltage stable
- Keep voltages on plates stable, facing to other plates
- Keep reference closer than foreign

Current loops

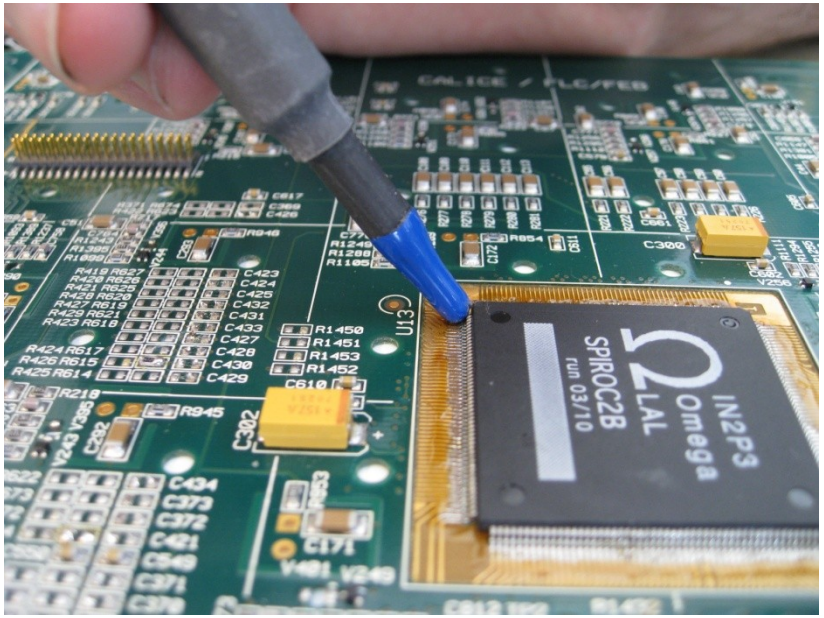


To do:

- Controlling return currents
- Keeping loops small
- Avoid overlapping with foreign components.

Guideline: Avoiding emission avoids in most cases picking up of noise

The design chain of a system: ASIC, the current switch

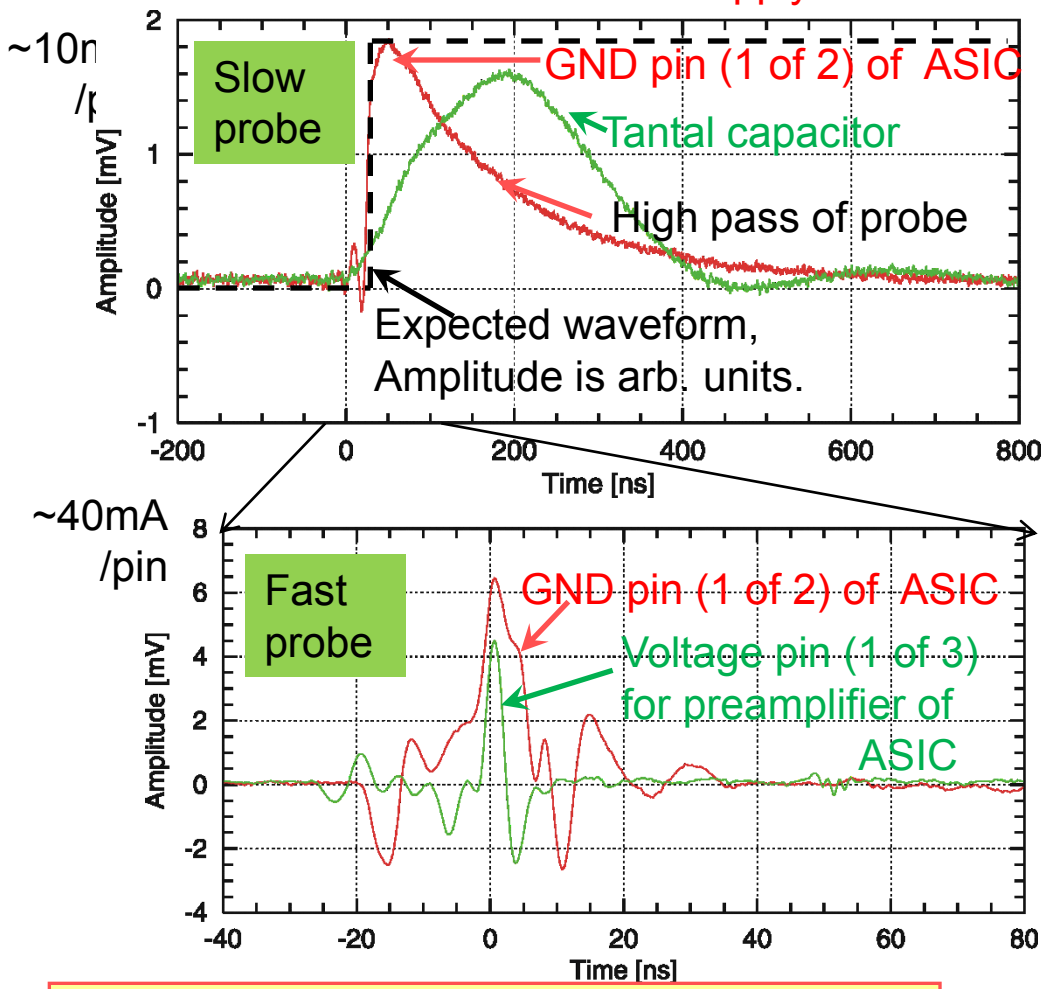


Board available with
12 x 12 channels, each 3 x 3cm^2
A layer will be around 2m^2: 2200 channels

Each ASIC 36 channels:
Currents switched: ~36mA/ASIC
~ 144mA/board
~2.2A/layer

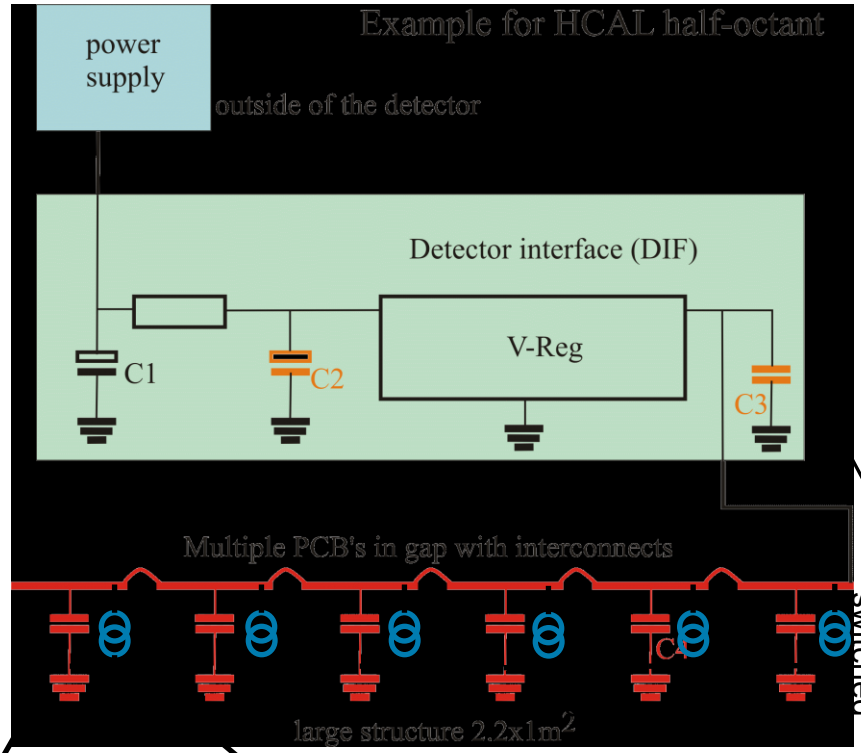
Measurement: Slow: 0.25 – 50MHz
Fast: 30MHz-3GHz

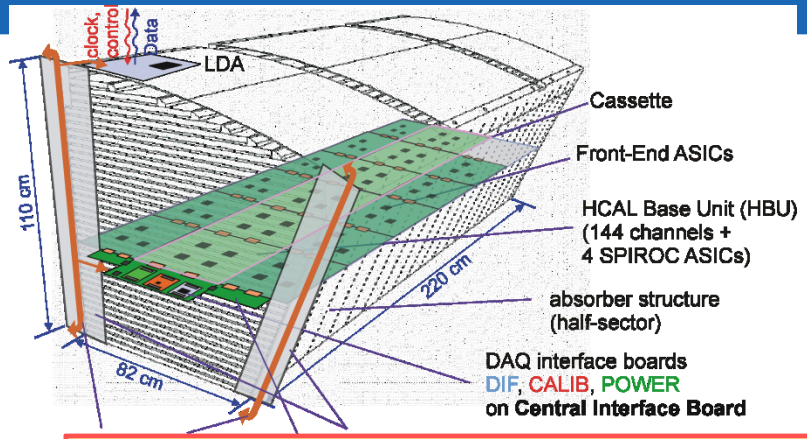
Measured currents at the GND-supply of ASIC



System has to deal with:
5Hz from train repetition to few 100 MHz
2.2A for a layer

The design chain of a system: Chain for voltage stabilization

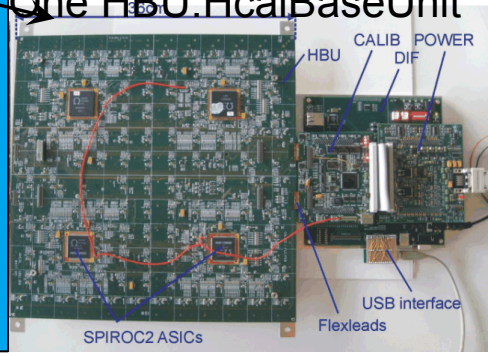




Concept:

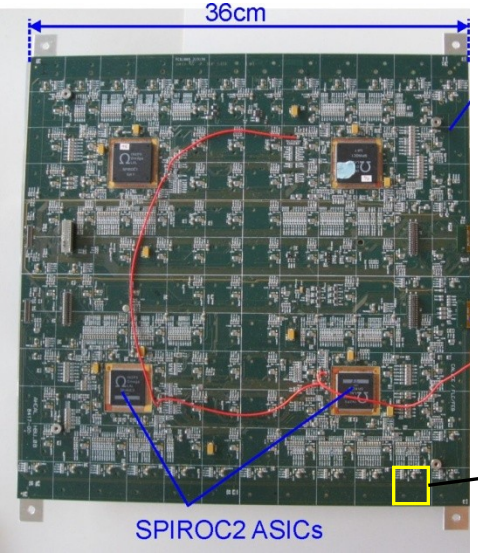
- High frequency local with large PCB and capacitors near ASIC: $2.2m \equiv 15ns$
- More charge and voltage regulator at end of layer: Q_{train} = 2A * 1ms = 2 mC
- Filter before cable from power supply
- Galvanic isolated power supply

Reality on lab-desk:
One HBU:HcalBaseUnit



Future

The layer with the sensors: HcalBaseUnit

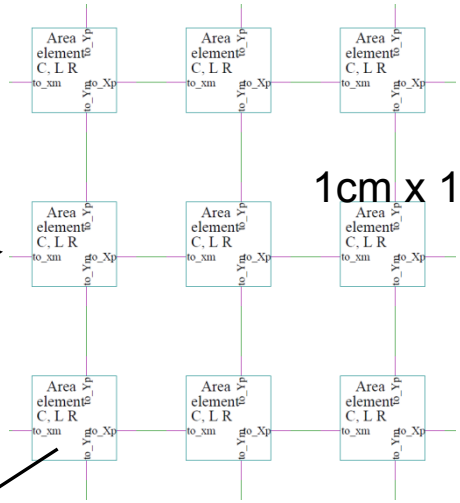


36 x 36 cm PCB
with scintillators, SiPM's LED

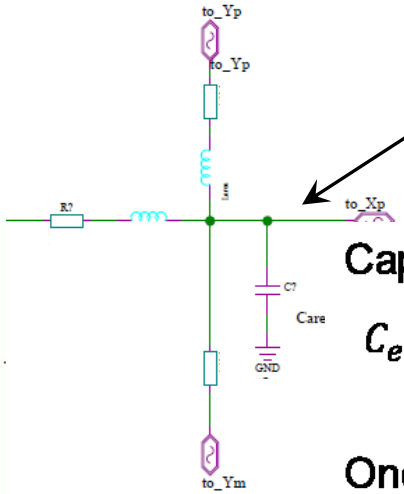
144mA switched current

Part of a thin cassette between absorber layer of HCAL

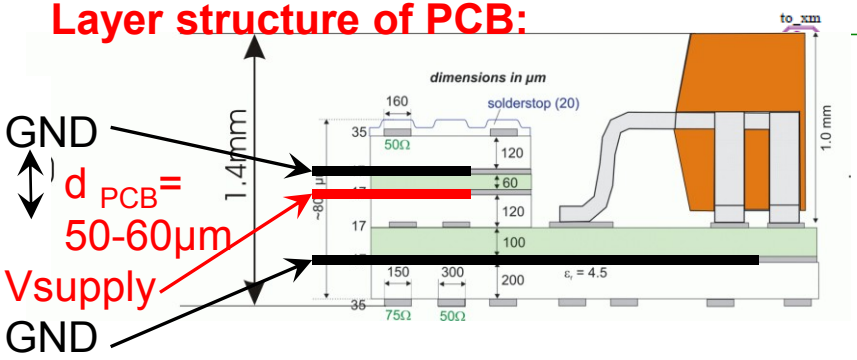
Simulation model:
"two diomensional delay line"



1cm x 1cm



Layer structure of PCB:



Capacitor well known:

$$C_{element} = \varepsilon_0 \varepsilon_r \frac{Area_{element}}{thickness_{PCB-layer}}$$

One dimensional delay well known:

$$Time_{delay} = \frac{c}{\sqrt{\varepsilon_r}} length_{element}$$

$$\Rightarrow \quad L_{element} = \frac{Time^2_{element}}{C_{element}}$$

By that one get
- a thin PCB and also
- **A good high frequency capacitor 60pF/cm²**
- layout with short distance to via maintain the performance.

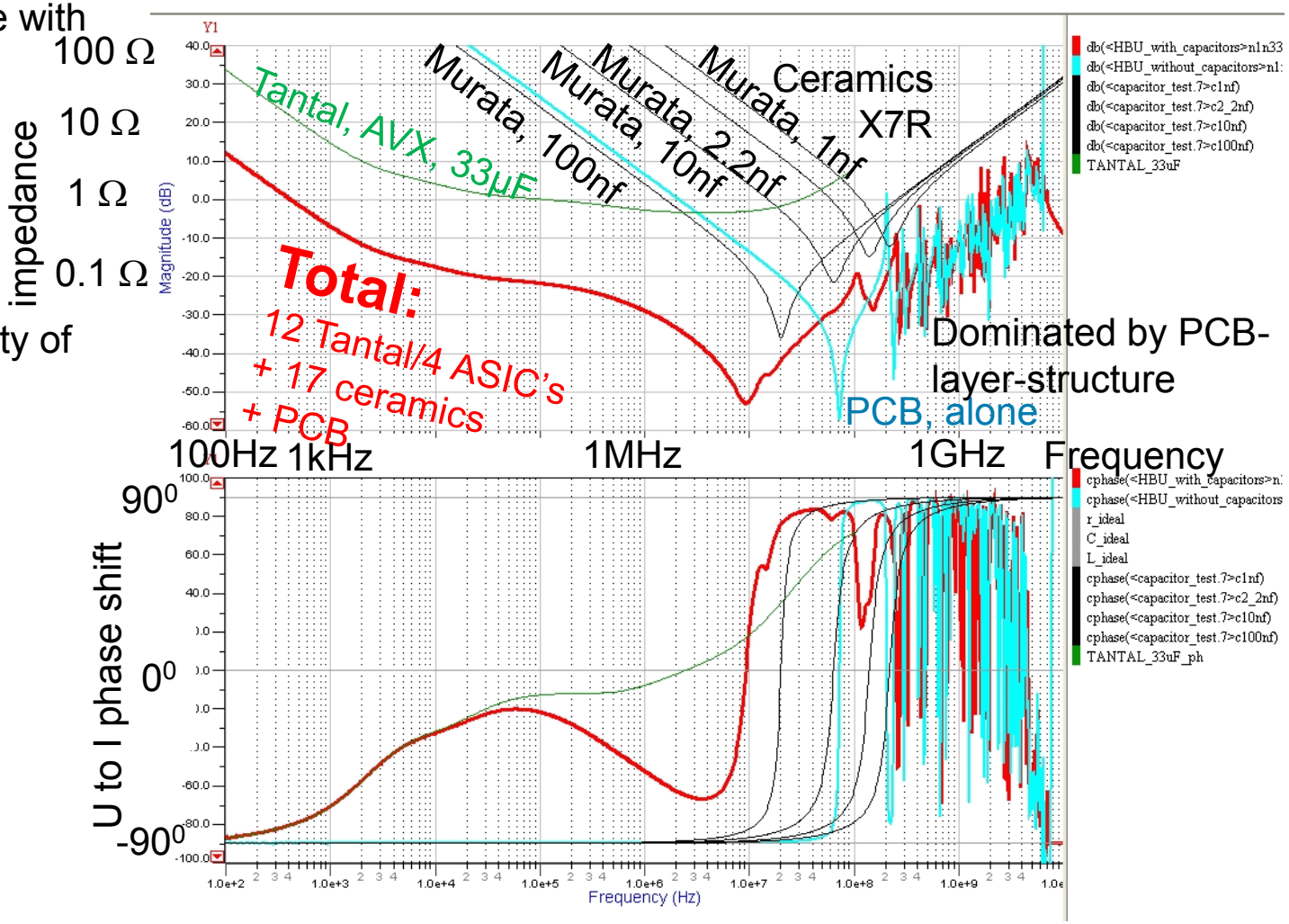
The layer with the sensors: HcalBaseUnit
The impedance, simulation

Wide frequency range with
Z< 0.1Ω
144mA: <20mV.

Below 10kHz
To be supported by end-of-layer module:
Need low DC-resistivity of connections.

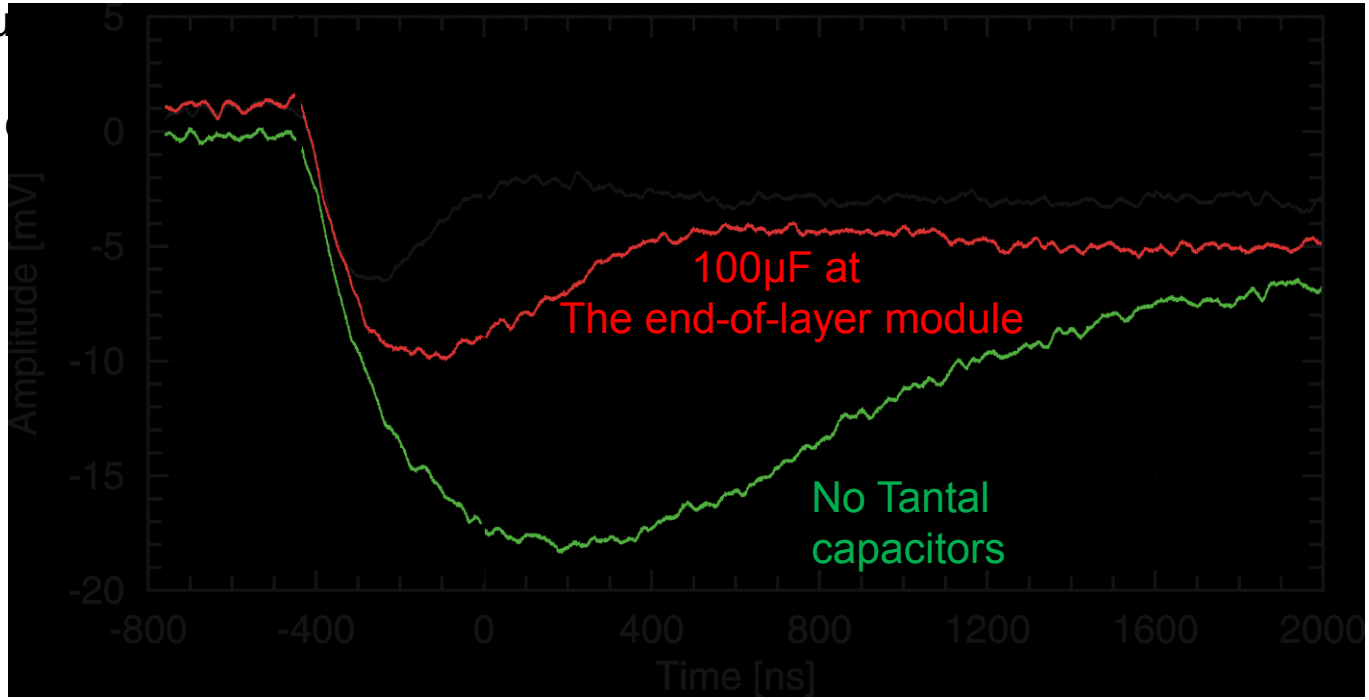
15GHz is granularity of simulation elements.
Trust until ~1.5GHz

Wide range with phase ≠ ±90⁰
So oscillation gets dumped,
not only reflected.



The layer with the sensors: HcalBaseUnit , Voltage stability, measurement

Analogu
supply
voltage
ASIC



DC-voltage shift:

For the test OK,
To be looked at for extension from one to six HBU's in a chain
Resistivity of voltage source, interconnect,

With 6 boards total current and resistance grow: Voltage drop 60mV, is still OK. ✓

Higher AC-shift, if Tantal is further away

CALICE AHCAL: thin 33µF-Tantal available to mount near ASIC's on HBU
Nice to understand, whether DC-resistance or distance is the source, or?

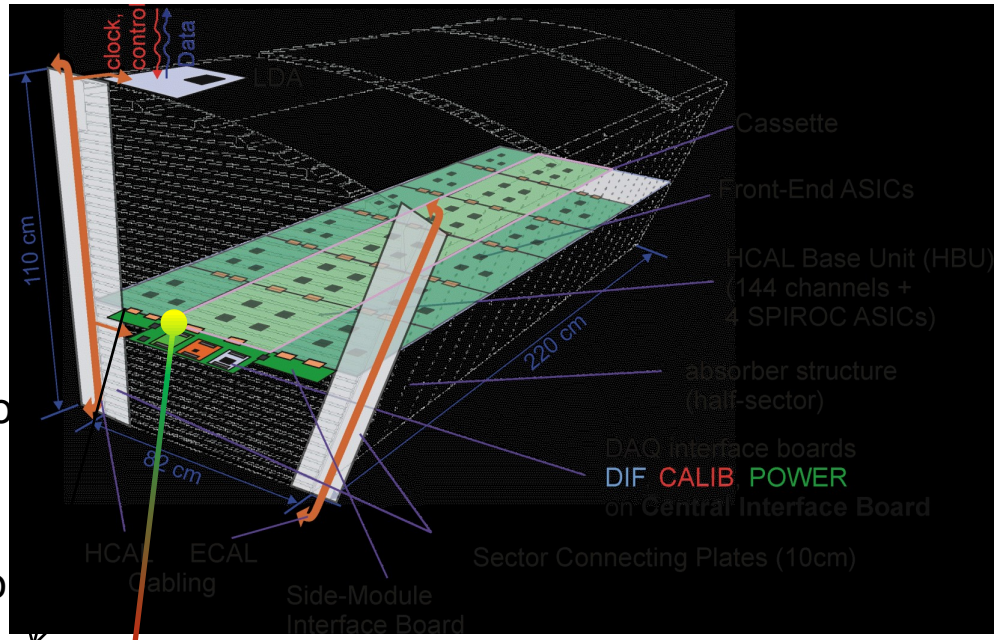
The layer with the sensors
Definition of the GND to surrounding

Within the detection layer the GND is return path (ΔV~60mV) and reference

Steel of structure is part of general GND_{safety}
so it is not good to use,
because currents might not stay there and move into whole ILD.

Slow control and bias voltage regulatio is at end-of-layer electronics.
Bias is the most critical in the system.

There it is easy to get a connection fro $GND_{surrounding}$ to $GND_{electronics}$ and very good to keep the SiPM bias defined.



Proposal:
Connect it at end-of-layer and per layer

Doing so and per layer means:
No other connection is allowed and all other should be kept galvanic isolated or the risk to introduce currents into the PE-system has to be managed.
Within the layer: up to 60mV between GND-PE and local GND-electronics.

Disadvantage:
- A supply and return line per layer
- Space constrains:
  Pair in a multi pair cable?

Compromise:
- Grouping neighboring layers
  (keep current limit of connectors within the range of fused supply)

The layer with the sensors, Stray capacitance to steel structure

Voltage drop of supply voltage:
- Voltage and return path have similar resistance: return ½

⇒ voltage drop on outer layer plane of PCB facing to a metal plate on GND

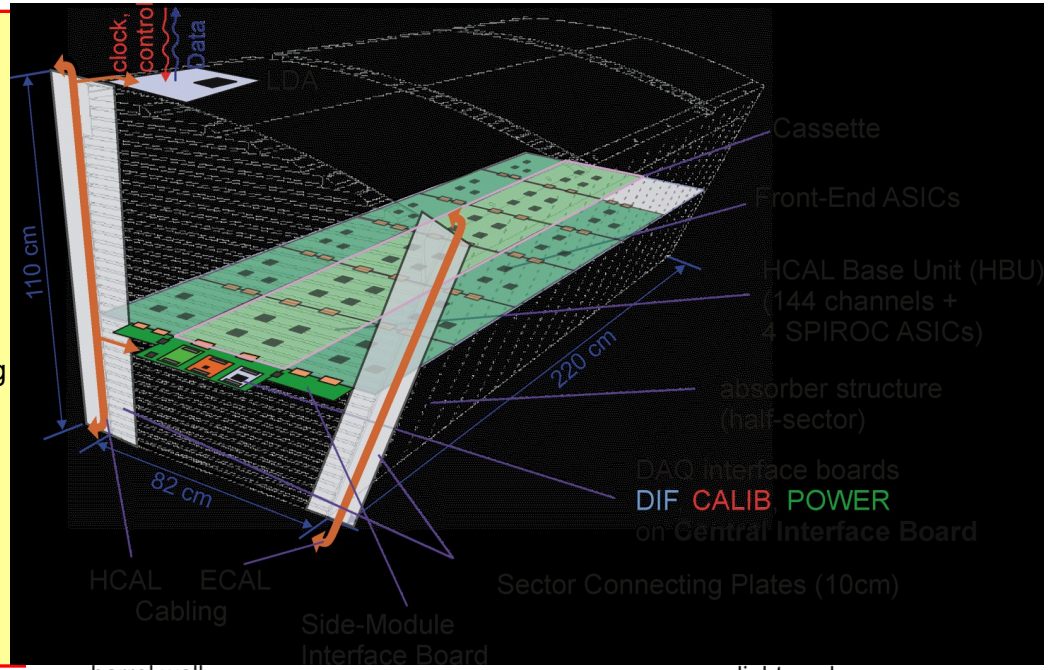
rounding

$$C_{stray} = \varepsilon_0 \frac{2m^2}{1.3mm} = 13nF$$

$$Q_{stray} < C_{stray} * 60mV = 0.8nC$$

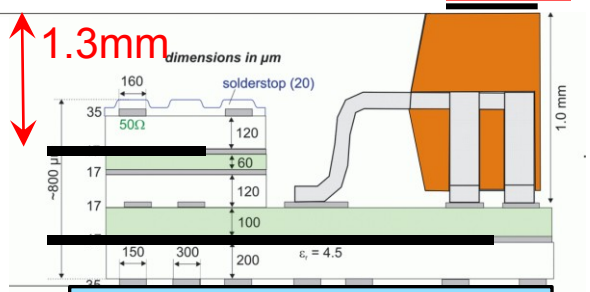
$$I_{stray} = \frac{Q_{stray}}{time(\sim 400ns)} = \frac{2.2mA}{layer}$$

⇒ **Reasonable small !!!!!**

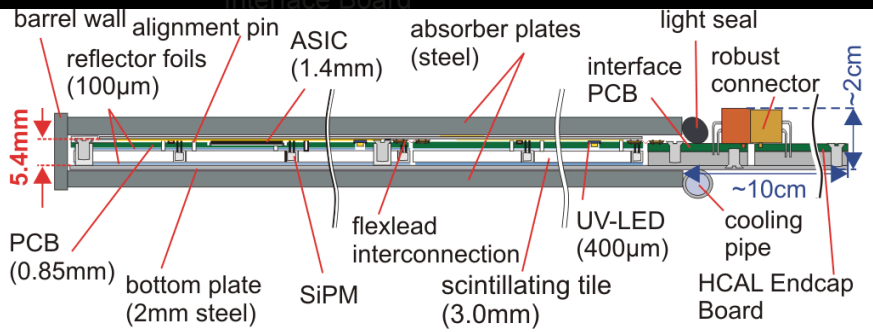


Metal plate

GND

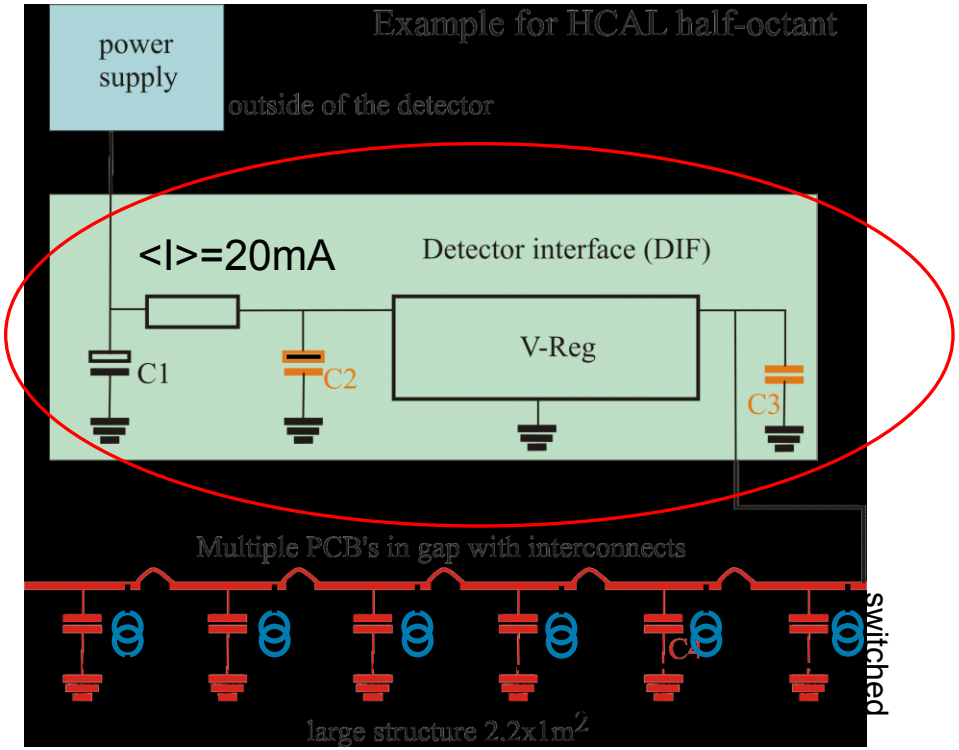


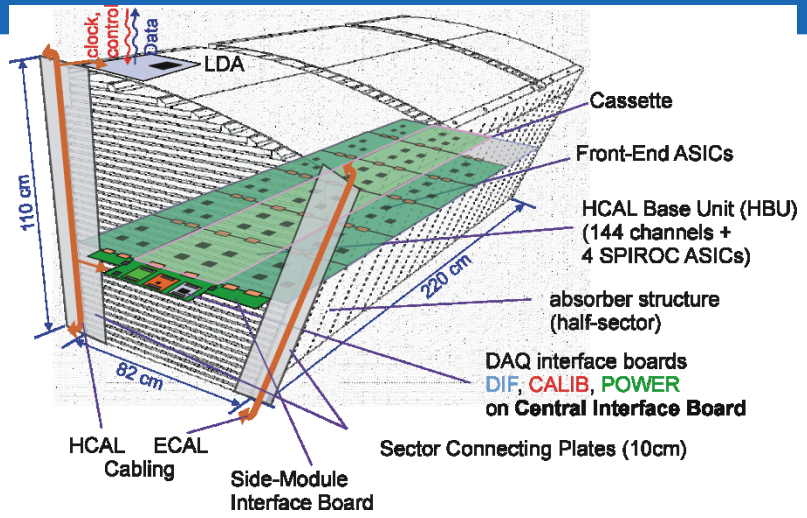
Plastic scintillator: 3mm



Currents of the electronics stays within the Very small loop of the Power-GND system of the PCB. ⇒ Risk is managed

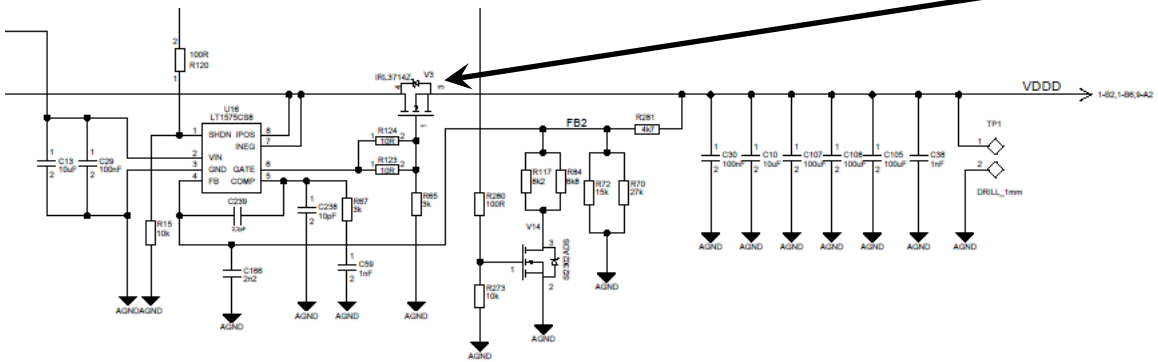
The design chain of a system: Chain for voltage stabilization





Need voltage regulator,
that reacts with 10µs
Need of 2mC within 1ms

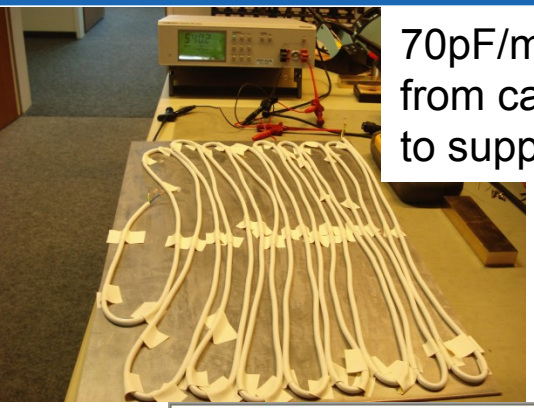
For prototype, we have
- fast voltage regulator
with external FET



Charge storage in C_2:
3.4mF,
voltage change: 0.6V

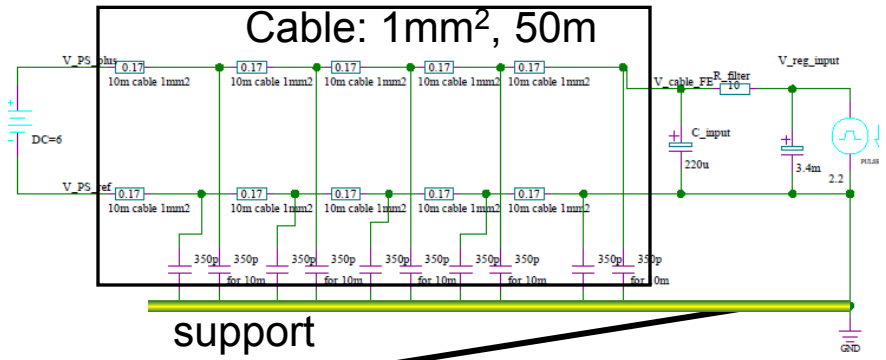
Input filter under investigation
See next slide: 10Ω, C_1=220µF ?

The design chain of a system: Feed back into the supply cable and its support

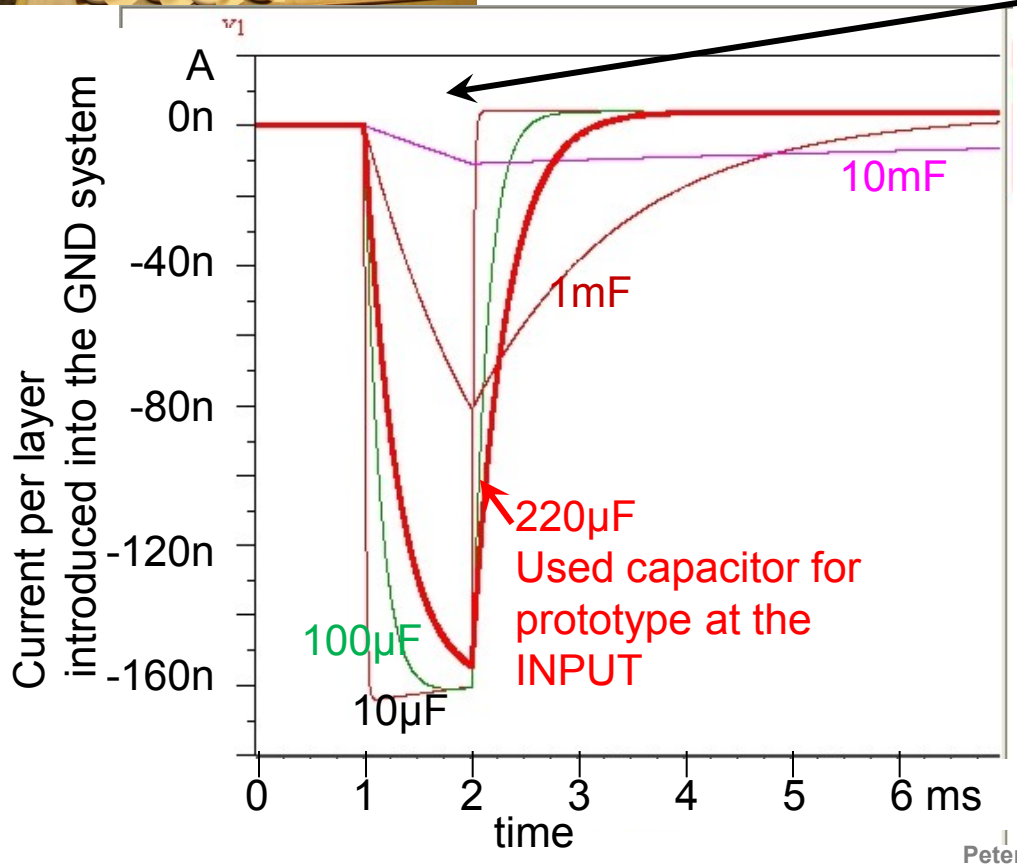


70pF/m from cable to support

Ideal power supply



ASIC as switched current sink



With a filter at the input of 10Ω and 220µF the curves looks reasonable smooth

Induced currents are low:

…. Assuming ideal power supply !!!

For full barrel:

48layers/half octant

16 half-octants/side

2 sides from interaction point

160nA/layer

⇒ **0.25mA** for the AHCAL barrel through cable chain

Remark

additional other contributions!

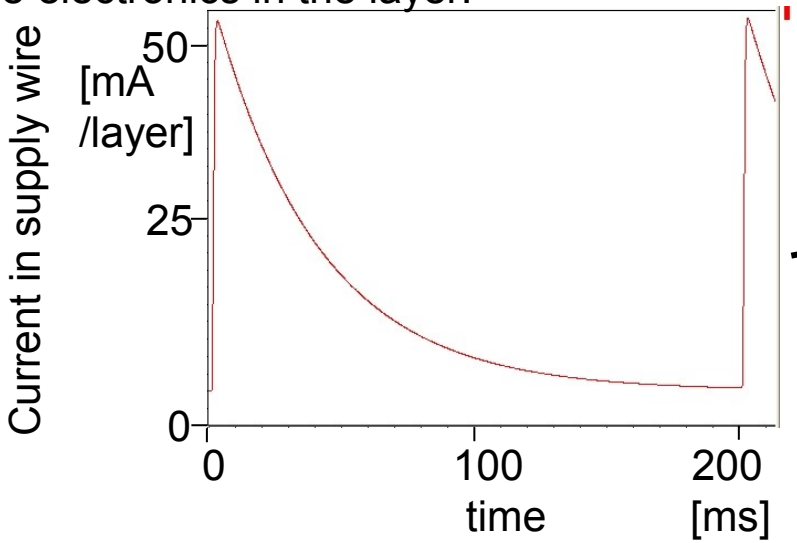
From EMI: 10mF look much nicer, but space constrains, compromise

The design chain of a system: Other cable issues

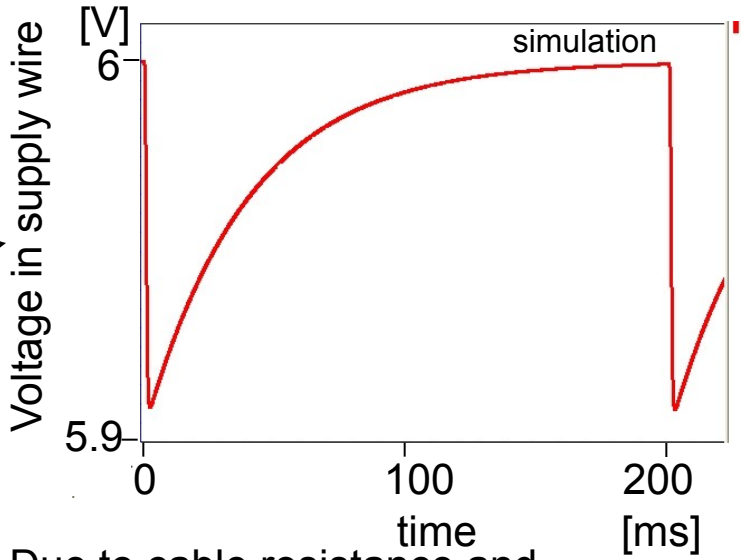
DC-current in cable:

- Additional constant load at the end of the layer: ~0.7A : 6kW for AHCAL-CALICE,
  FPGA-based, charge storage w/o DC/DC-converter
  Voltage drop for 1mm^2, 50m : 1.2V, reasonable efficiency.

Modulated current by power cycling the electronics in the layer:



Ideal Supply and resistance of cable



The common mode current (160nA)is 10^5 smaller.
To avoid, that the total supply is picked up by GND or foreign:
Keep supply and return wires close to each another, or well understood overlay regions with GND/foreign.

…. That good performance, because of closing higher current loops locally and local charge storage.

Due to cable resistance and supply return= GND and frontend half of that voltage change appears as common mode change at supply:
50mV.

Careful:

Simulation underestimates parasitic effects

The design chain of a system: Power supply

Tasks, requested for functionality?

- Galvanic isolation needed for: Definition of GND-point at sensitive frontend
  Compensation of voltage drop on cable
  Avoiding currents in the safety GND system
  Need exactly ONE cable per channel to detector

- Low capacitive coupling from electronic-system to GND_{safety}
  typical supplies have few 100nF, small laboratory 1-10nF
  factor 1000 more than the cable…… 0.25mA for AHCAL-barrel
  induced current transform immediately into 250mA.

- From Frontend requested reaction times of power supply: < 1ms
  That is fast for standard power supplies !
  Slower reaction times causes higher voltage changes and
  larger induced currents…..

Options: It is outside experiment:

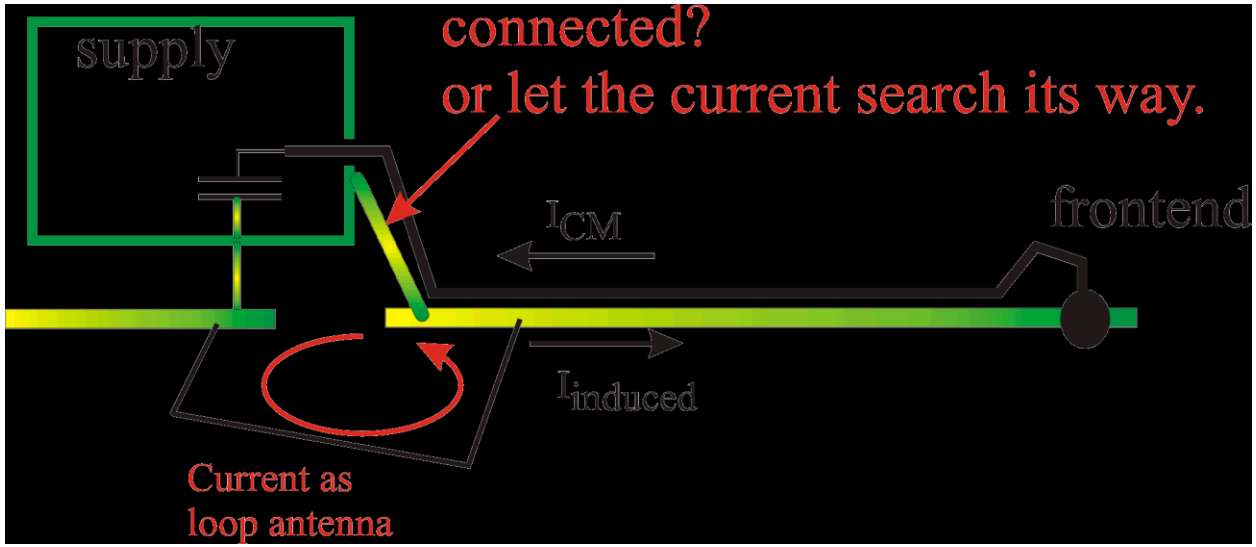
Most of that is not investigated so far in the context of CALICE-AHCAL
- more mechanical space opens options
  - charge storage to slow down before power supply start to regulate
  - filter for common mode currents

The design chain of a system: Power supply

Integration issues:

Connection of cable support to the housing?

+ good to dump the currents induced to the cable support without loop antenna
-- No galvanic isolation between service-room and experiment, most modern systems don't allow that at all, too many connections anyway, but if fully realized: No pickup of low frequency noise-currents



- Fusing, current limits to weakest point of chain until next fuse/limit
  front end likes small connectors, but also grouping layers to reduce cables
  Compromises including the frontend

Summary

- Detectors for Linear Colliders requires many channels with low power
- Train structure allows 99% time to be OFF: Factor 100 in critical regions
- Coherent fast switching ON/OFF of high current:
  CALICE-AHCAL: 2.2A*layers : 3.4kA for the barrel
  5Hz to few 100MHz
- System aspects at local design
  - Keeping currents local with well defined return-path
  - Local charge storage for wide frequency range with
  - Good circuit and PCB design: ceramics, tantals

  keeps
  - the impedance small
  - the currents leaving a defined volume small with slow rise times
- System aspects within whole experiment
  Lower frequency part has to be handled by cables and power supply
  Need well control of cable routing and good integration of power supply.
- Simulation leaves many parasitic effects out
  Underestimates the high frequency EMI-disturbance
  …. Experiments, concepts to be better than simulation promises