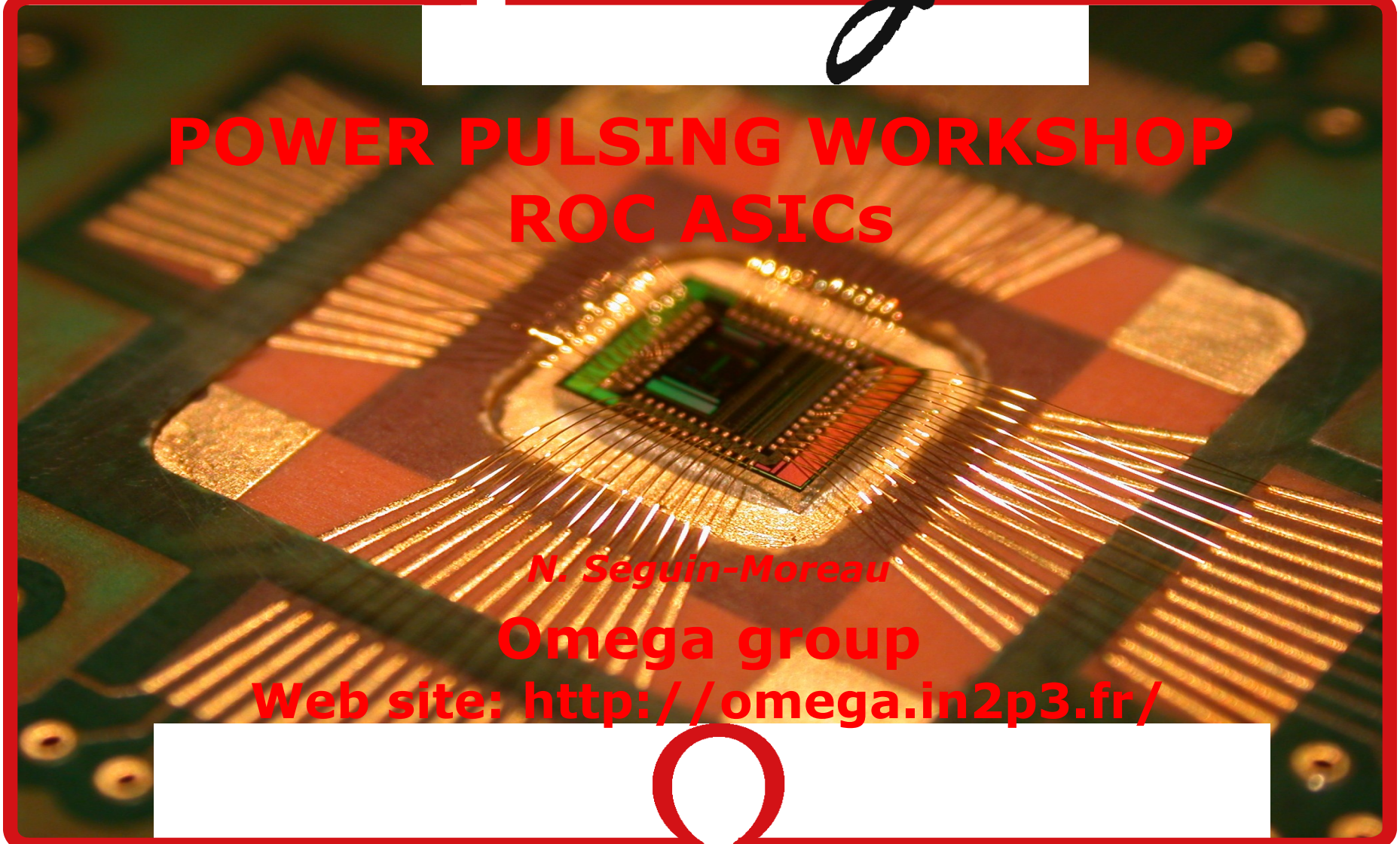
POWER PULSING WORKSHOP
ROC ASICs



N. Seguin-Moreau

Omega group

Web site: http://omega.in2p3.fr/

Orsay MicroElectronics Group Associated

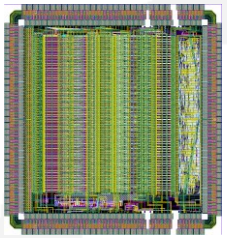
ROC ASICS: POWER ISSUES

It is gonna heat, hopefully, there is the power pulsing

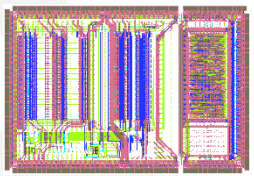
ROC chips

- **Silicon Germanium 0.35 µm BiCMOS** technology
- Readout for MaPMT and SiPM for ILC calorimeters and other applications
- Very high level of integration : System on Chip (SoC)
- Start of **3D integrated 130nm** electronics for sLHC pixels in 2008
- Start of design for spatial applications (EUSO) in 2009
- Web site: http://omega.in2p3.fr/

MAROC3
ATLAS luminometer

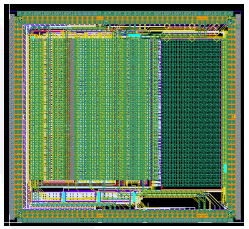


PARISROC2
Pmm2 exp.

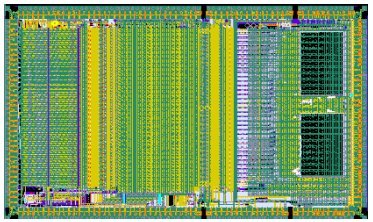


ROC for ILC calorimeters power pulsed designs

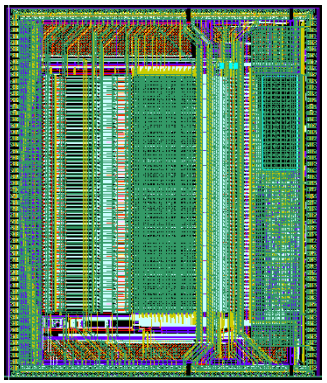
HARDROC2



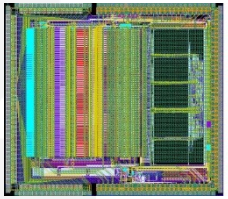
SPIROC2



SKIROC2

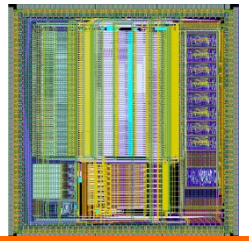


MICROROC1



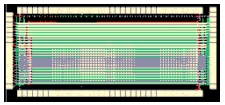
Ultra Low power designs

SPACIROC (EUSO,Spatial exp.)



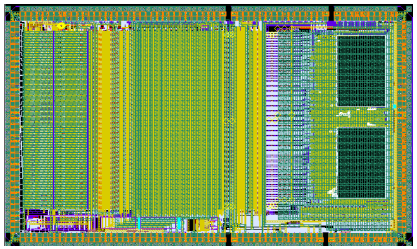
0.35 µm SiGe

OMEGAPIX (3D, ATLAS-SLHC pixels detector



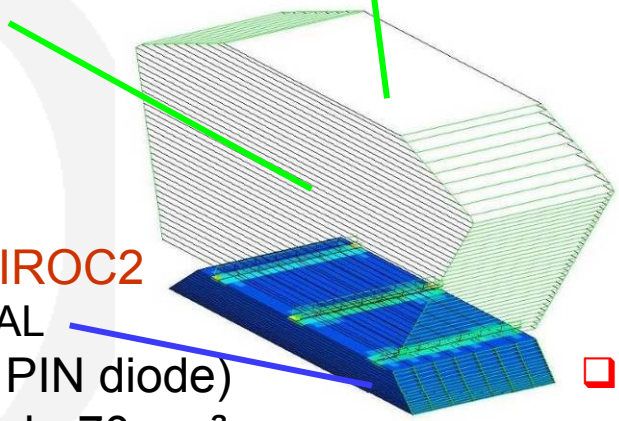
3D 130nm

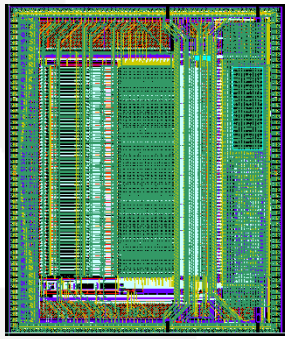
ROC chips for ILC prototypes



SPIROC2
Analog HCAL (AHCAL)
(SiPM)
36 ch. 32mm²
June 07, June 08, March 10

HARDROC2 or MICROROC
Digital HCAL (DHCAL)
(RPC or μmegas)
64 ch. 16mm²
HR: Sept 06, June 08, March 10
Microroc: June 10



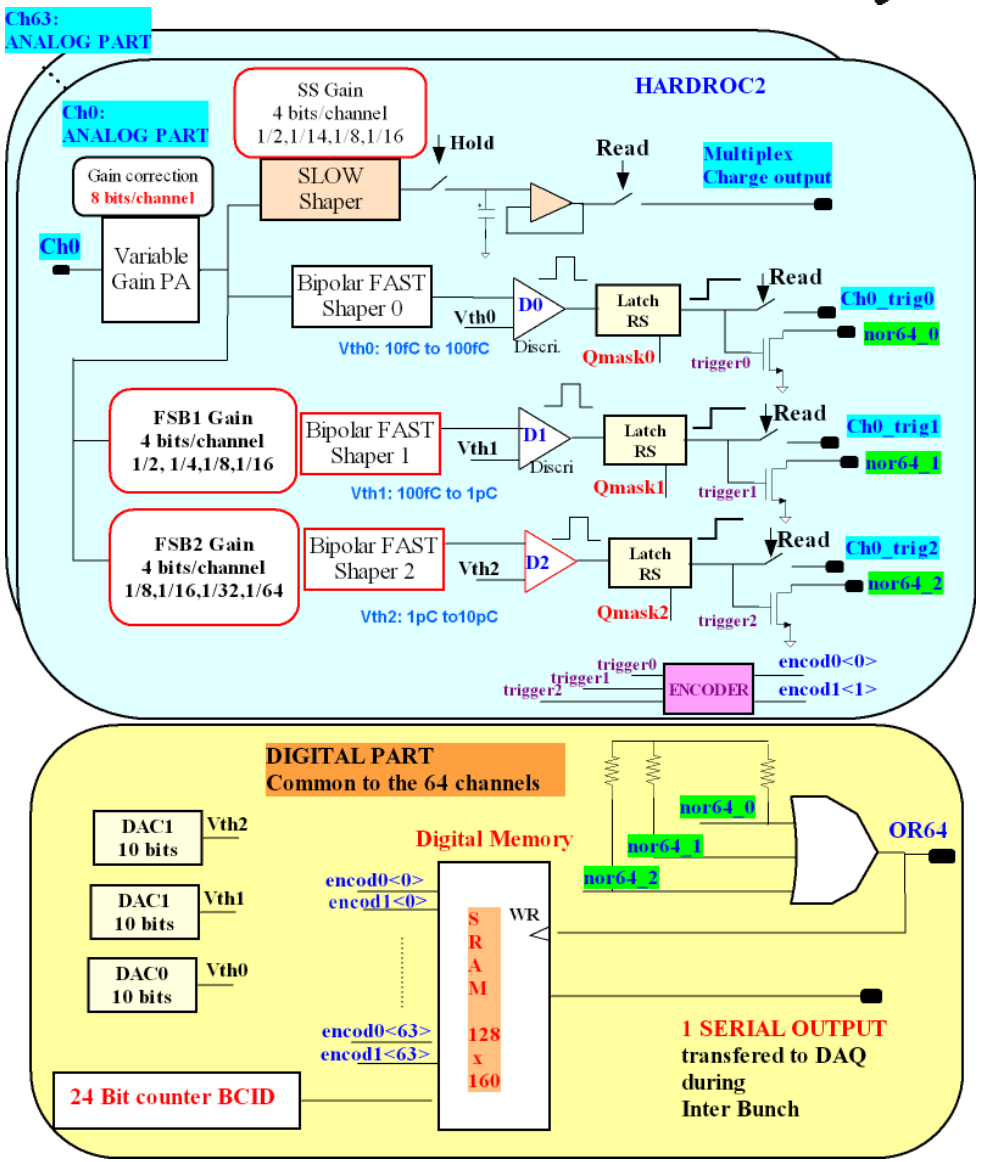


SKIROC2
ECAL
(Si PIN diode)
64 ch. 70mm²
March 10

- ROC chips for **technological prototypes**: to study the feasibility of large scale, industrializable modules (CALICE,Eudet/Aida funded, DHCAL ANR)
- Requirements for electronics
  - Large dynamic range (15 bits)
  - Auto-trigger on ½ MIP
  - On chip zero suppress
  - Front-end embedded in detector
  - **Ultra-low power : 25μW/ch**
  - 10^8 channels
  - Compactness
- « Tracker electronics with calorimetric performance »
- No chip = no detector !!

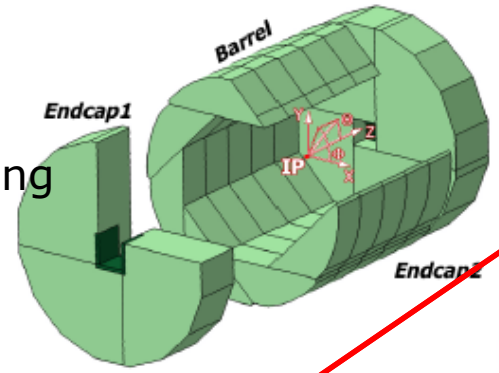
HaRDROC : ILC DHCAL readout

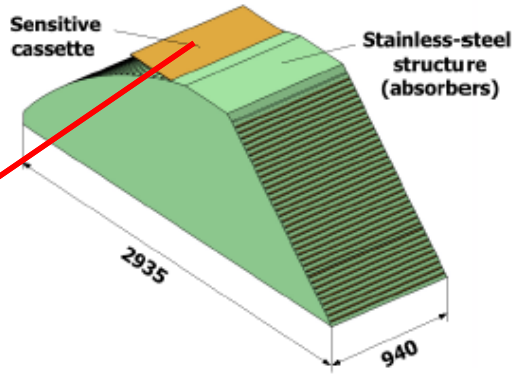
- **64 inputs**
- Current preamp with **8 bits** gain correct: G=0 to 255 (analog G=0 to 2)
- **3 shapers**, variable Rf,Cf and gains:
  - Fsb1, G= ½,**1/4**,1/8,1/16
  - Fsb2, G= 1/8,**1/16**,1/32,1/64
- **3 discriminators**
  - 3 10 bit-DACs to set the thresholds (100fC, 1pC, 10pC)
  - Encoded in 2 bits
- **Auto-trigger down to 10fC up to10pC**
- Store all channels and BCID for every hit in a **127 bit deep digital memory**
  - Data format : 127(depth)*[2bit*64ch+24bit(BCID) +8bit(Header)] = 20 kbits
- **872 SC registers**, default config
  - Mask of bad channels
- **Full power pulsing: < 10µW/ch**
- 10 000 chips produced to equip 400 000 ch of the technological prototype (ANR DHCAL)
- collab. LLR, IPNL, LAPP



HaRDROC : DHCAL integration issues

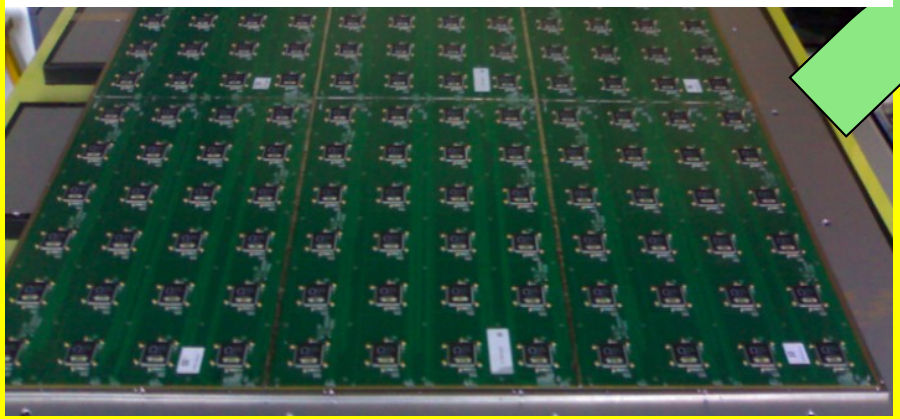
- 1 cm2 Pads, 50 Millions of channels
- 1 m2 = 6 ASU (Boards) X 24 Hardroc2 = 10 000 channels/ m2
- Few external components
- Power < 1mW/ch when running continously, 10 µW/ch with a 0.5% duty cycle





Each **sensitive cassette** contain a **readout board** stick to a **GRPC**.

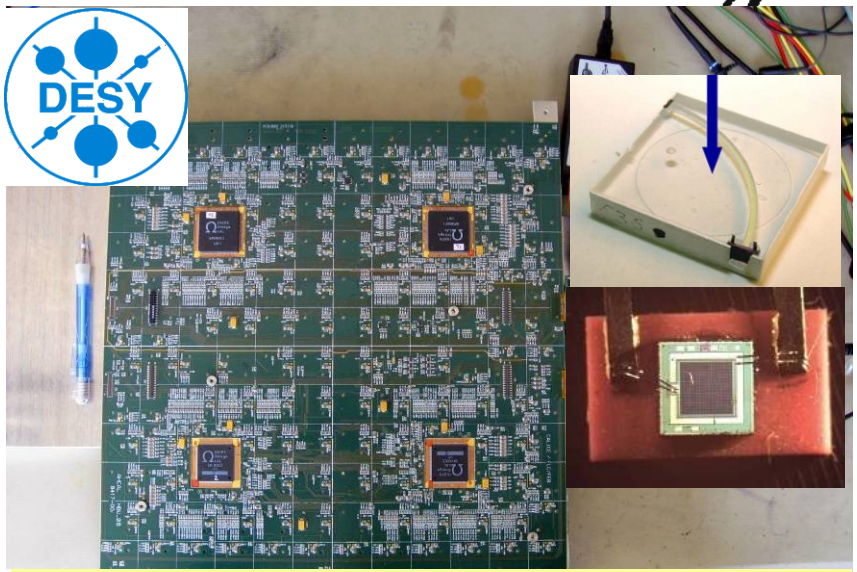
1 m² semi-digital readout HARDROC



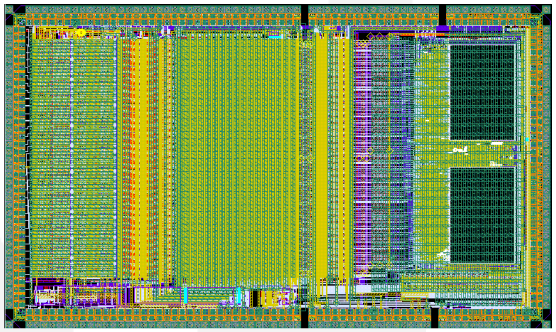
1 m² GRPC

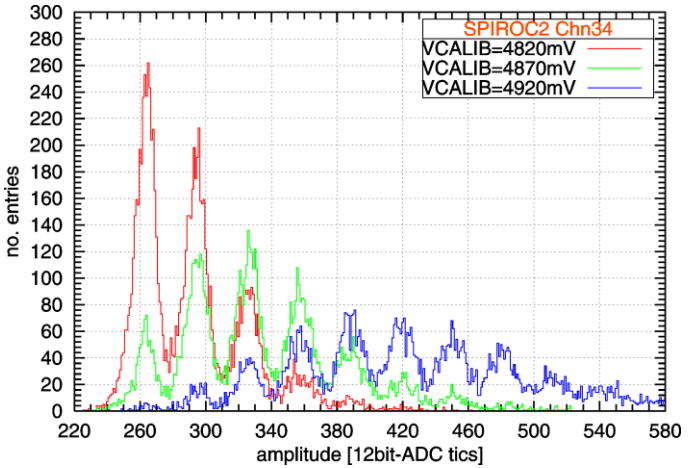
SPIROC : ILC AHCAL readout

- SPIROC : Silicon Photomultiplier Integrated Readout Chip
  - Silicon PM detector G=10^5-10^6
  - 36 channels
  - Internal 12 bit ADC/TDC
  - Charge measurement (0-300 pC)
  - Time measurement (< 1 ns)
  - Autotrigger on MIP or spe (150 fC)
  - Sparsified readout compatible with EUDET 2nd generation DAQ
  - Pulsed power: **25 µW/ch**



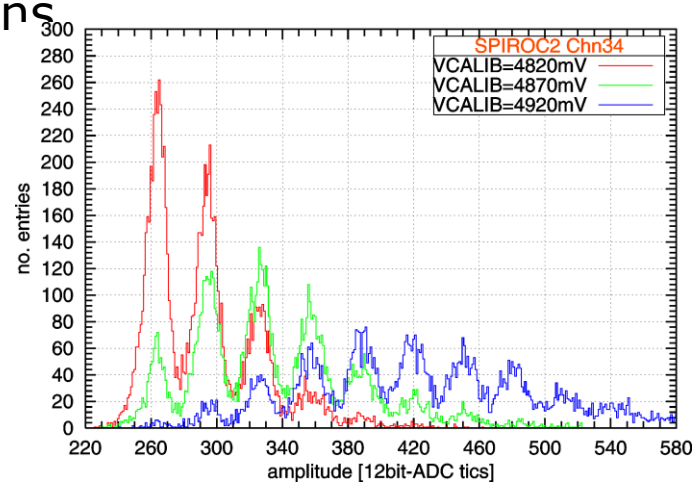
(0.36m)² Tiles + SiPM + SPIROC (144ch)





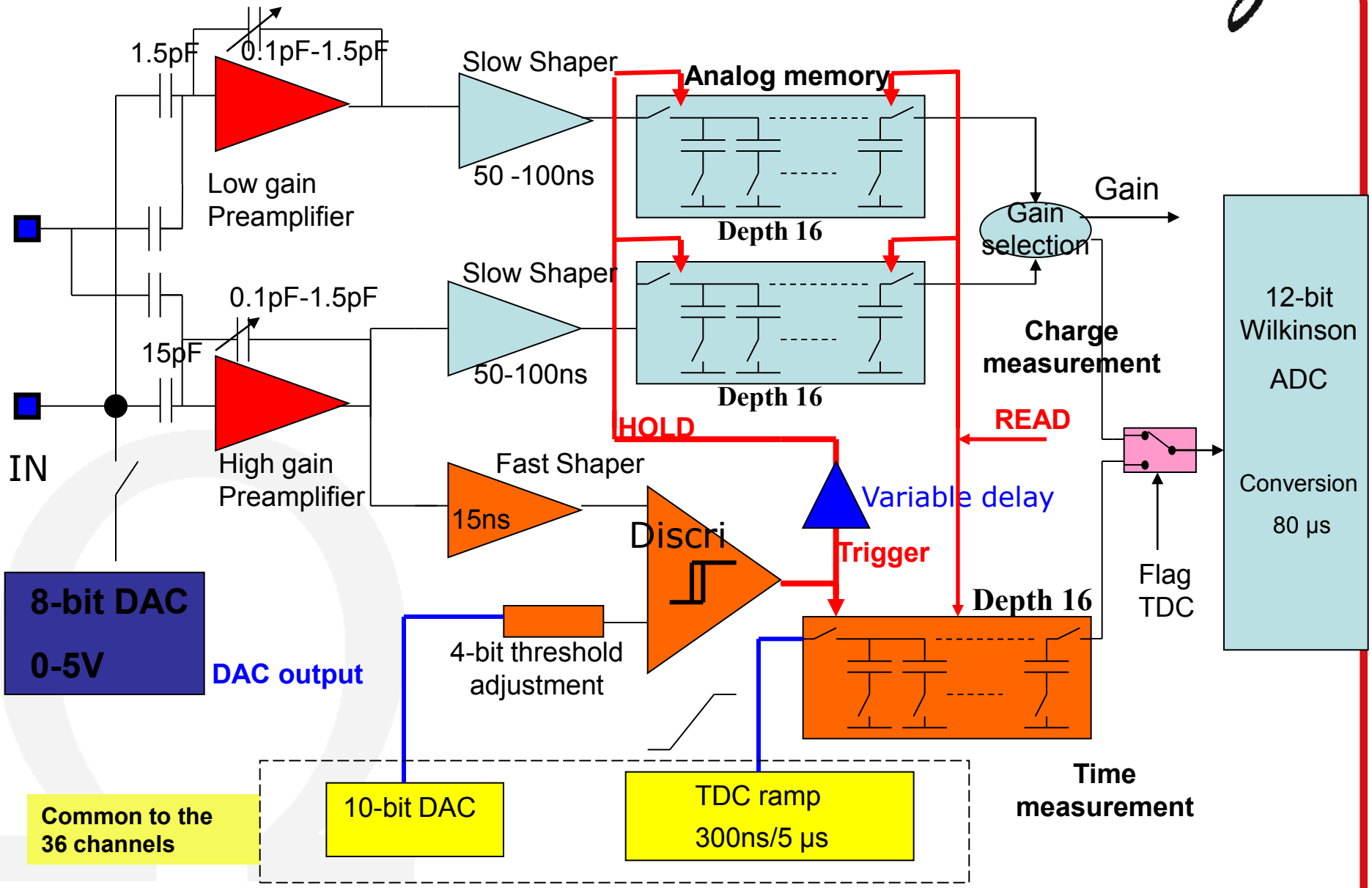
SPIROC main features

- Internal input 8-bit DAC (0-5V) for individual SiPM gain adjustment
- Energy measurement : 14 bits
  - 2 gains (1-10) + 12 bit ADC: 1 pe → 2000 pe
  - Variable shaping time from 50ns to 100ns
  - pe/noise ratio : 11
- Auto-trigger on 1/3 pe (50fC)
  - pe/noise ratio on trigger channel : 24
  - Fast shaper : ~10ns
  - Auto-Trigger on ½ pe
- Time measurement :
  - 12-bit Bunch Crossing ID
  - 12 bit TDC step~100 ps



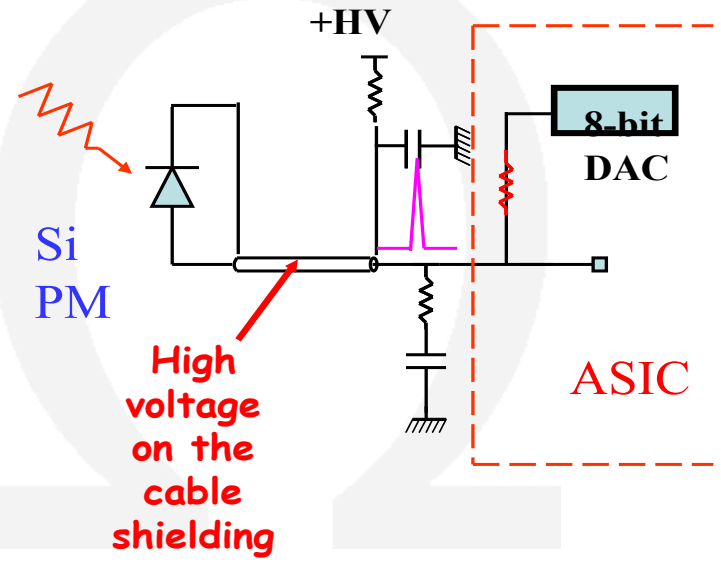
- Analog memory for time and charge measurement : depth = 16
- Low consumption : ~25µW per channel (in power pulsing mode)
- Individually addressable calibration injection capacitance
- Embedded bandgap for voltage references
- Embedded 10 bit DAC for trigger threshold and gain selection
- Multiplexed analog output for physics prototype DAQ
- 4k internal memory and Daisy chain readout

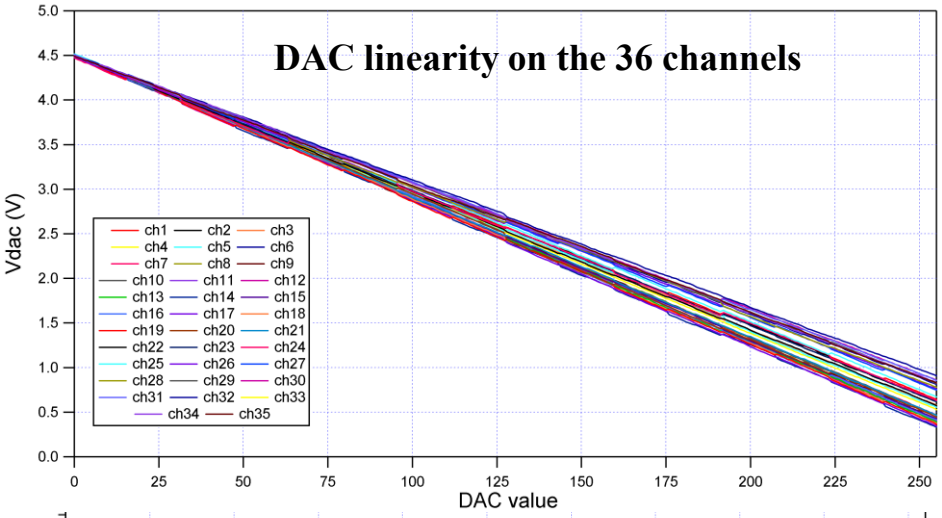
SPIROC : One channel schematic

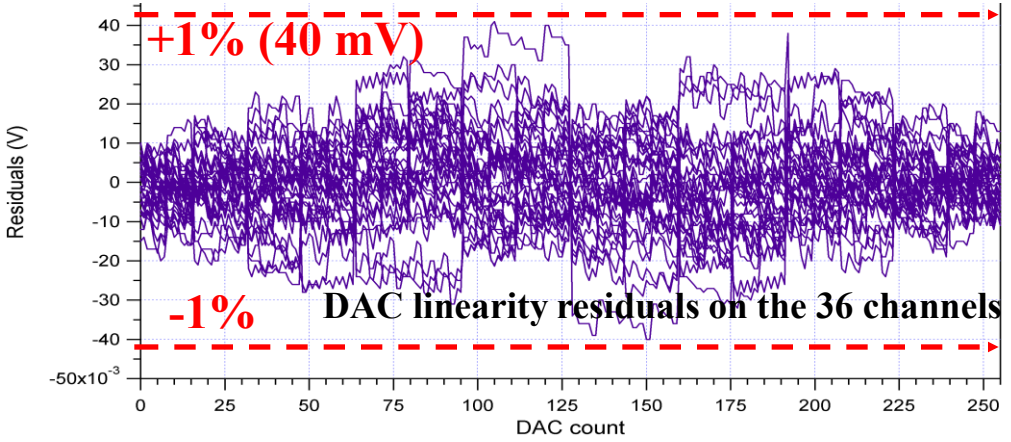


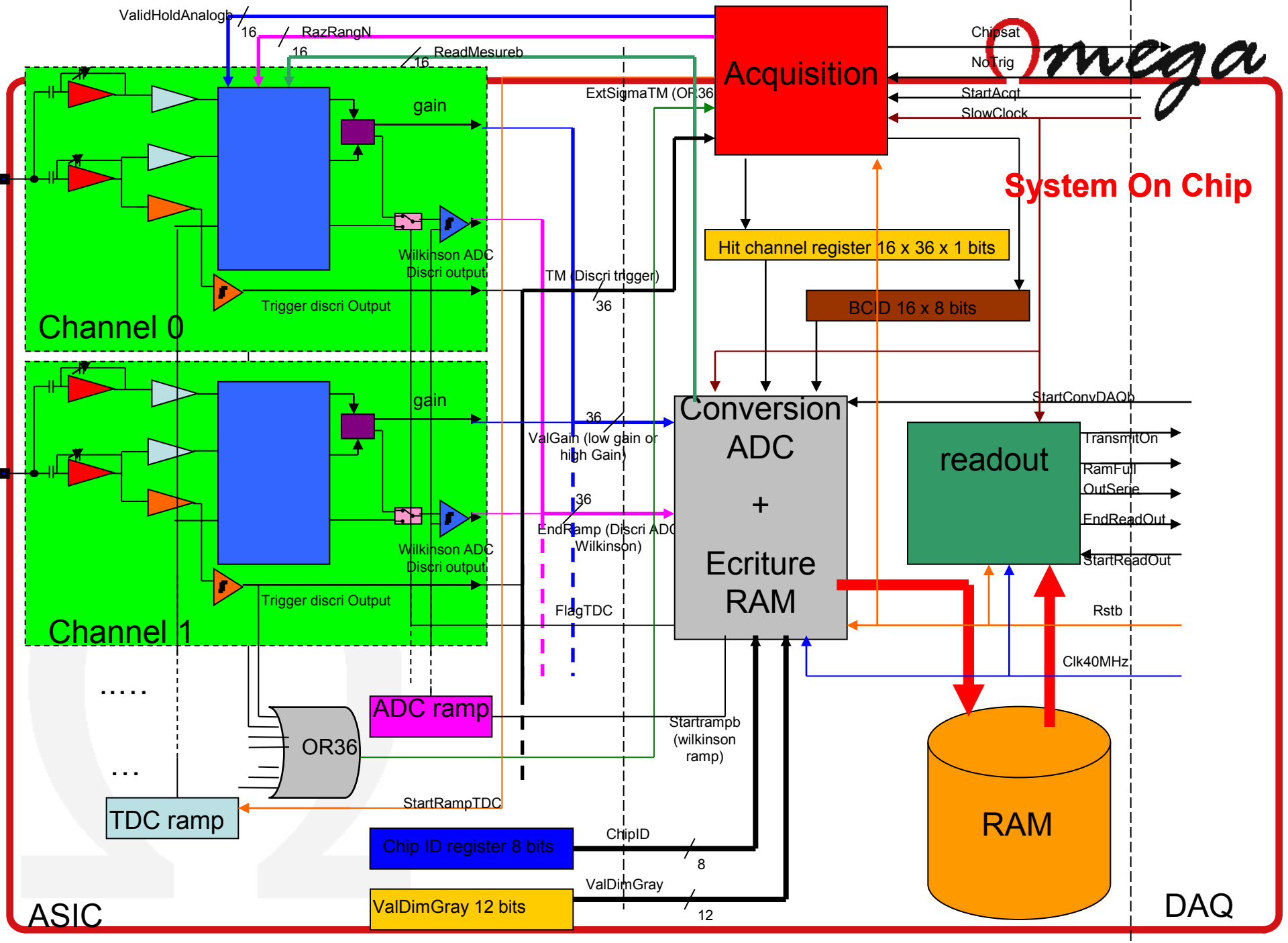
SPIROC2B: Input DAC

- Input DAC to optimize SiPM bias voltage
- 8-bit DAC, 5V range, LSB=20mV
- 36 DAC (one per channel)
- Ultra low power (<1µW) : no power pulsing
- Can sink 10 µA leakage current
- Linearity : ± 1%
- DAC uniformity between the 36 channels : ~3%



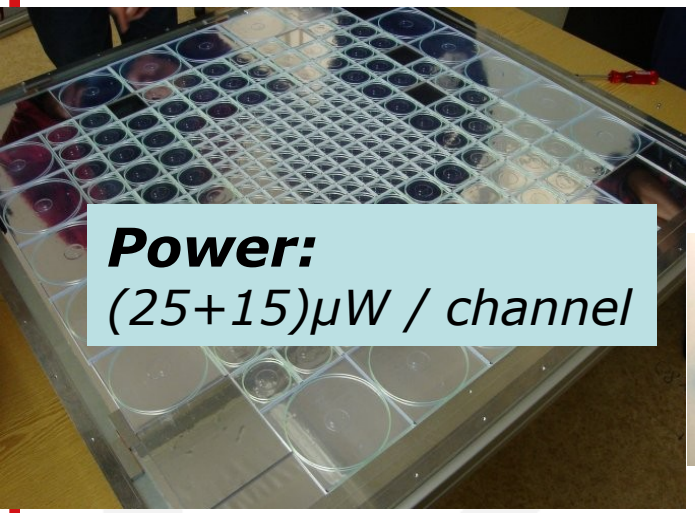




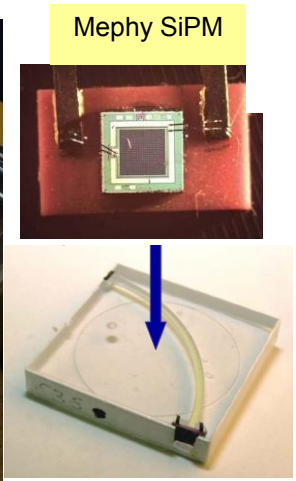

ValidHoldAnalogb
16
RazRangN
16
ReadMesureb
16
Acquisition
Chipsat
NoTrig
StartAcqt
SlowClock
ExtSigmaTM (OR36
Omega
System On Chip
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 0
TM (Discri trigger)
36
Hit channel register 16 x 36 x 1 bits
BCID 16 x 8 bits
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 1
36
ValGain (low gain or high Gain)
36
EndRamp (Discri ADC Wilkinson)
FlagTDC
Conversion ADC + Ecriture RAM
StartConvDAQb
readout
TransmitOn
RamFull
OutSerie
EndReadOut
StartReadOut
Rstb
Clk40MHz
.....
...
OR36
ADC ramp
Startrampb (wilkinson ramp)
TDC ramp
StartRampTDC
Chip ID register 8 bits
ChipID
8
ValDimGray
ValDimGray 12 bits
12
RAM
ASIC
DAQ

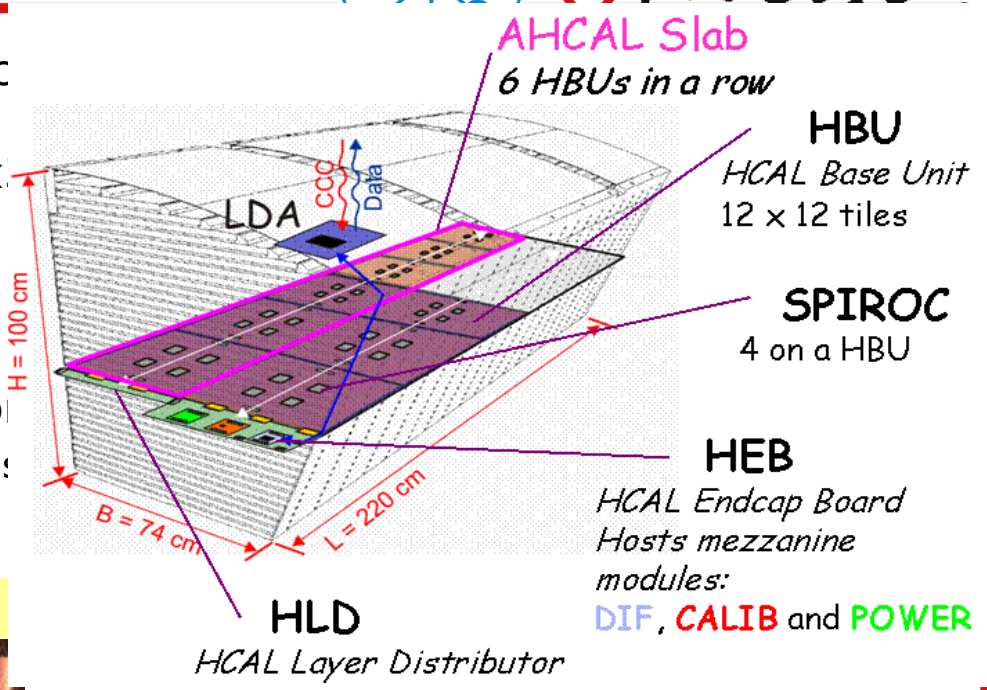
AHCAL: Technological prototype

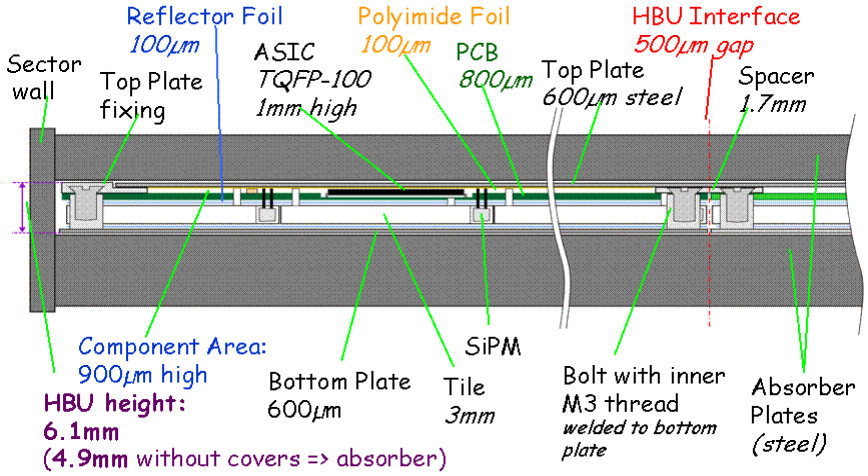
- SiPM detector: 40 layers of 1.5 m^2 2c thick steel plates interleaved with cassettes of 296 scintillating tiles (3x cm^2) readout by SiPMs
- 8 Millions of channels
- Few external components
- FE Chip embedded inside the detecto
  - Thickness:critical issue: Mother boards (HBU) are sandwiched between 2 absorber plates



@Peter Goetlicher's talk

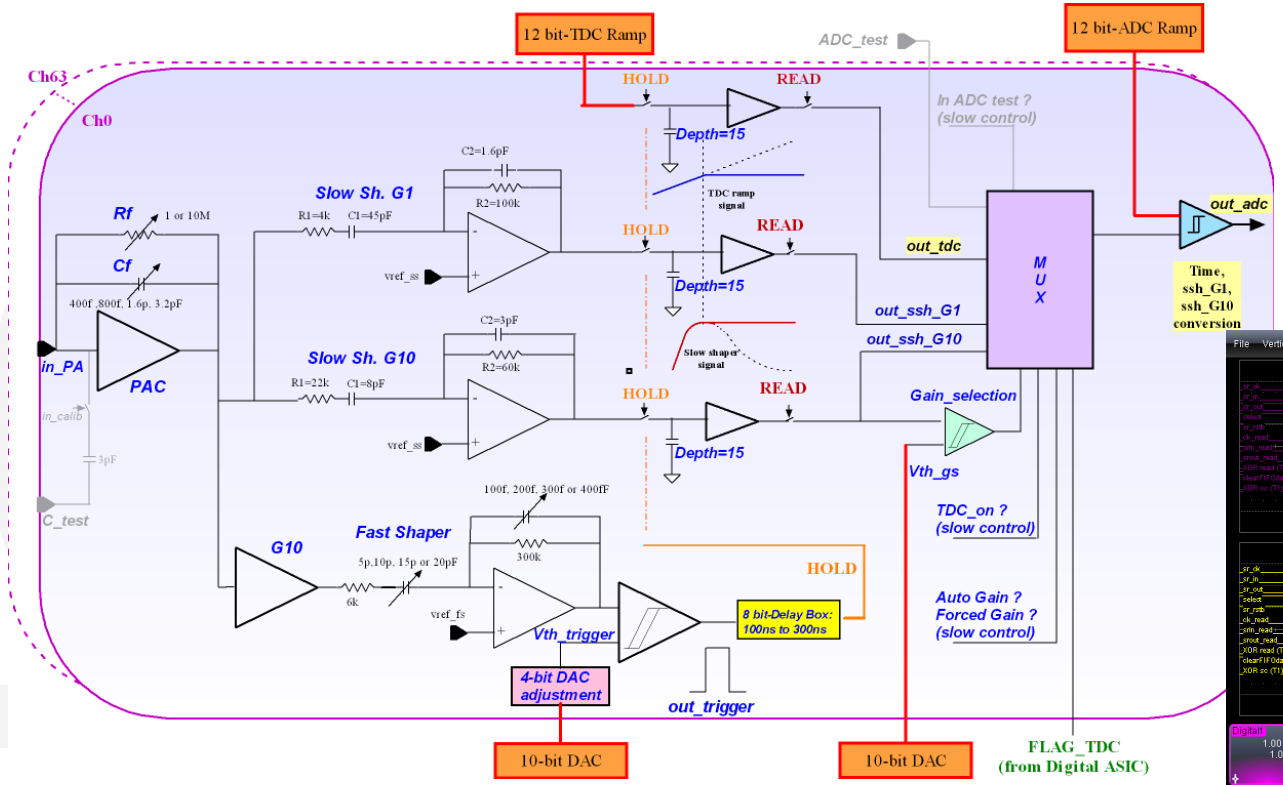


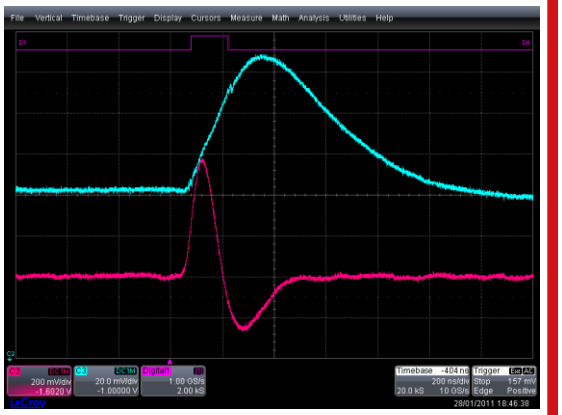




SKIROC2

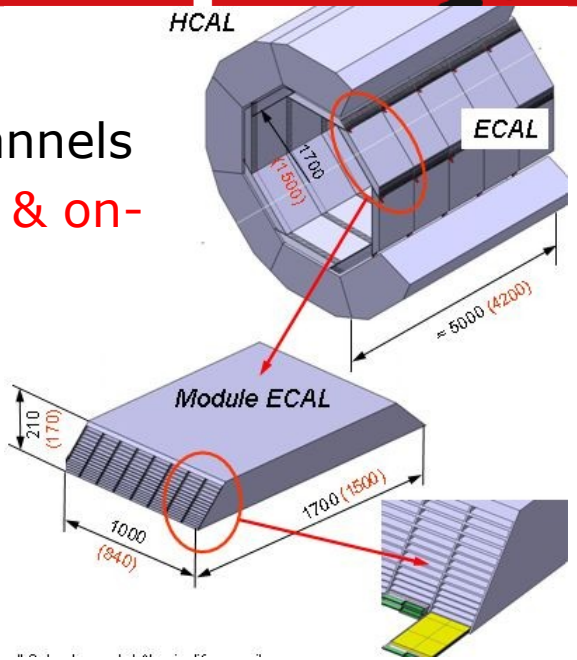
- 64 channels to readout Si pin diodes of the Si-W ECAL
  - Autotrigger on MIP (4 fC)
  - 15 depth SCA for Charge measurement (up to 10 pC) and Time measurement (< 1 ns)
  - 1 memory of 4K bytes to handle Charge and Time measurements from the internal ADC
  - Internal 12 bit ADC/TDC
  - Pulsed power: **25 µW/ch** (1 % duty cycle)

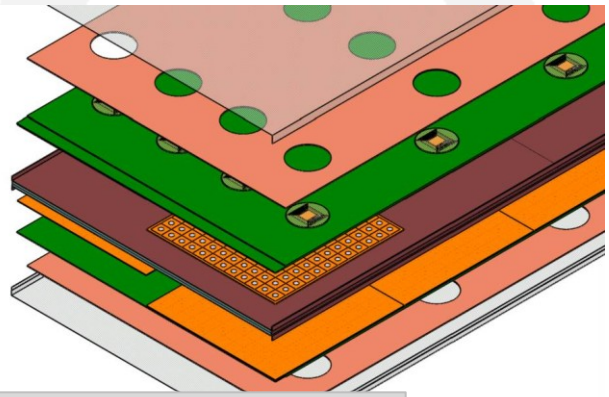




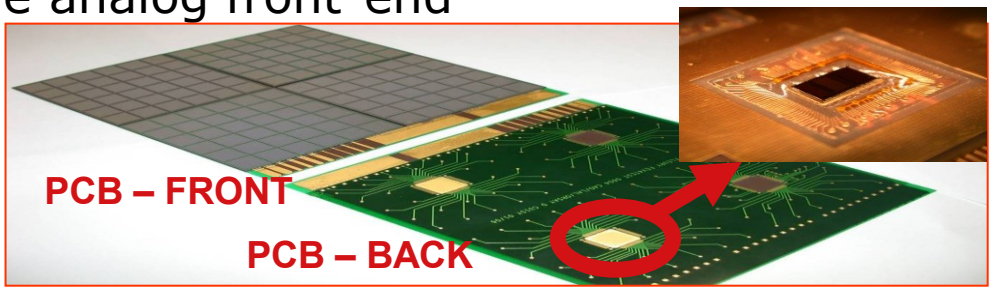
ECAL module: integration issues

- Front-end ASICs embedded in detector
  - Very high level of integration (100 Millions Channels
  - Ultra-low power: pulsed mode and Digitization & on-chip processing
  - Target 0.35 µm SiGe technology
- All communications via edges
  - 8,000 ch/slab, minimal room, access, power
  - small data volume (~ few 100 kbyte/s/slab)
- « Stitchable motherboards »
- No external component
  - Digital activity with sensistive analog front-end





See Remi Cornat's talk



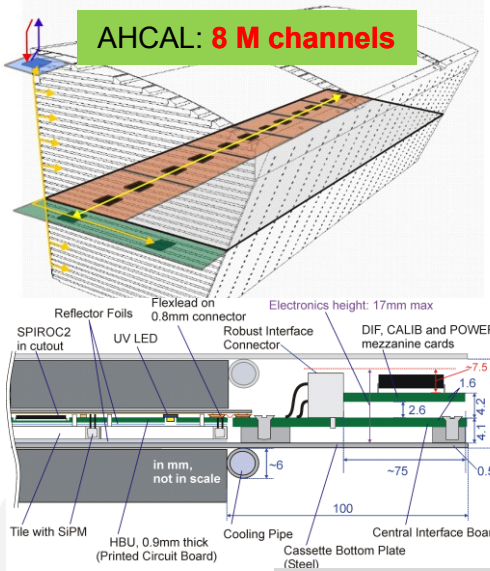
An ASU (Active Sensor Unit)

Elementary motherboard 'stitchable' 18*18 cm ~1024 ch. ~ 16 FE ASICS
1 FEV= 4 wafers 9X9 cm2 = 4x4 chips skiroc2 64 ch => 1024 pads.

ILC ROC CHIPS: INTEGRATION

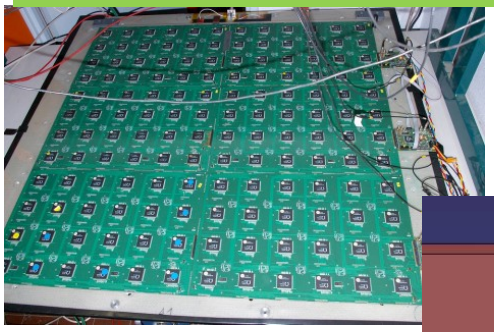
- High granularity of the calorimeters => huge number of electronic channels

AHCAL: **8 M channels**

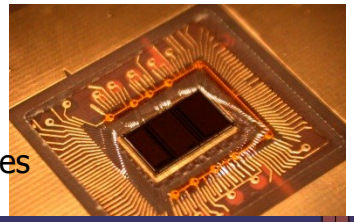


DHCAL: **50M channels**

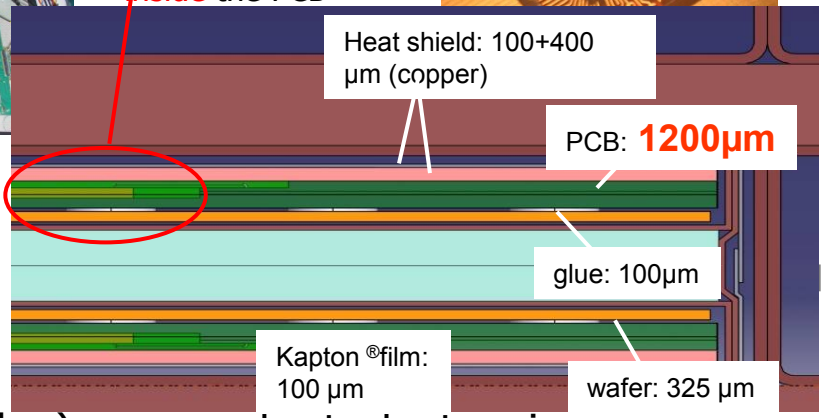
1 m2:144 chips x 64 ch ~ 10 000 Ch.
A few external components



ECAL: **100 M channels**
Chips directly bonded
0 external components



Chips and bonded wires **inside** the PCB



See Robert Kiefer's talk

- Compactness and reduction of cracks (cables) => readout electronics **embedded** in the detector, a few external components possible for AHCAL and SDHCAL but NO external components for the ECAL

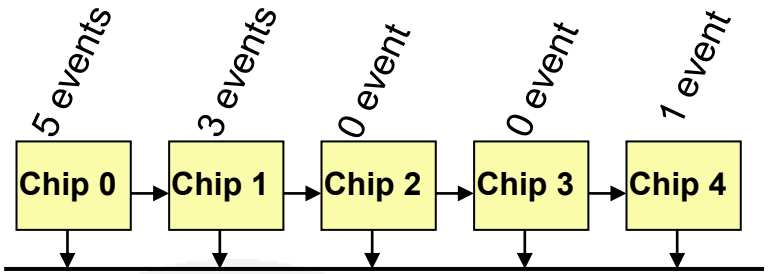
⇒ **MINIMISATION OF THE POWER:**

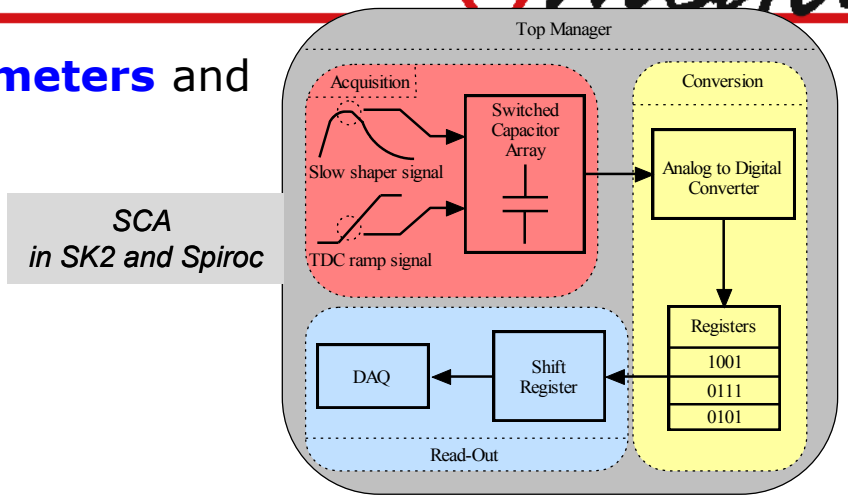
⇒ **DAISY CHAIN READOUT and POWER PULSING** taking into account the future duty cycle of the ILC beam

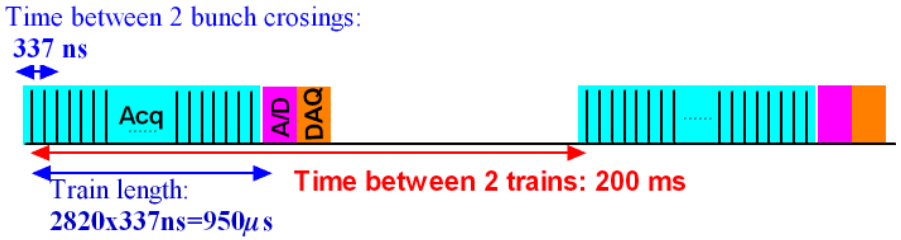
COMMON READOUT: TOKEN RING Mode

Readout architecture **common to all calorimeters** and **minimization of data lines & power**

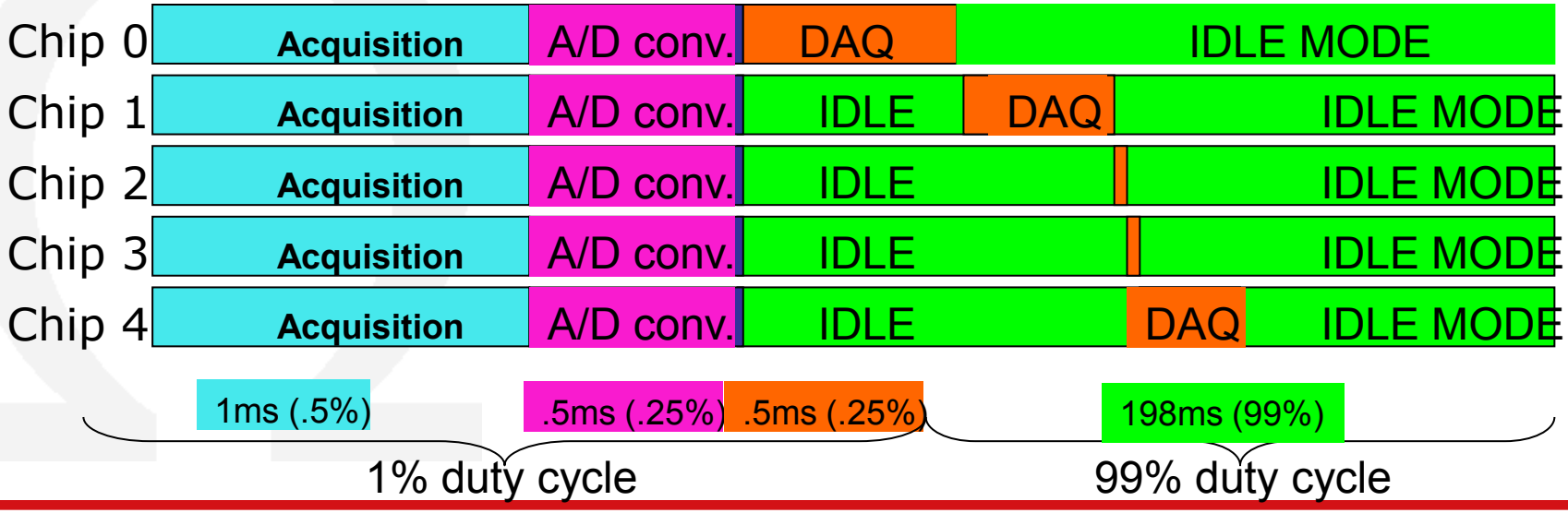
- **Daisy chain** using token ring mode
- Open collector, low voltage signals
- Low capacitance lines





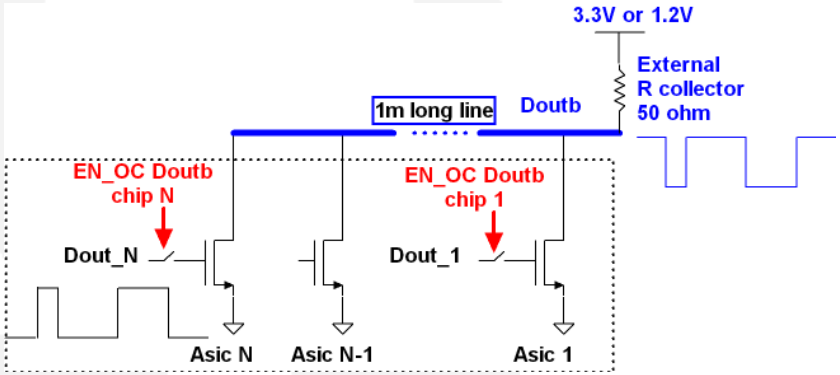


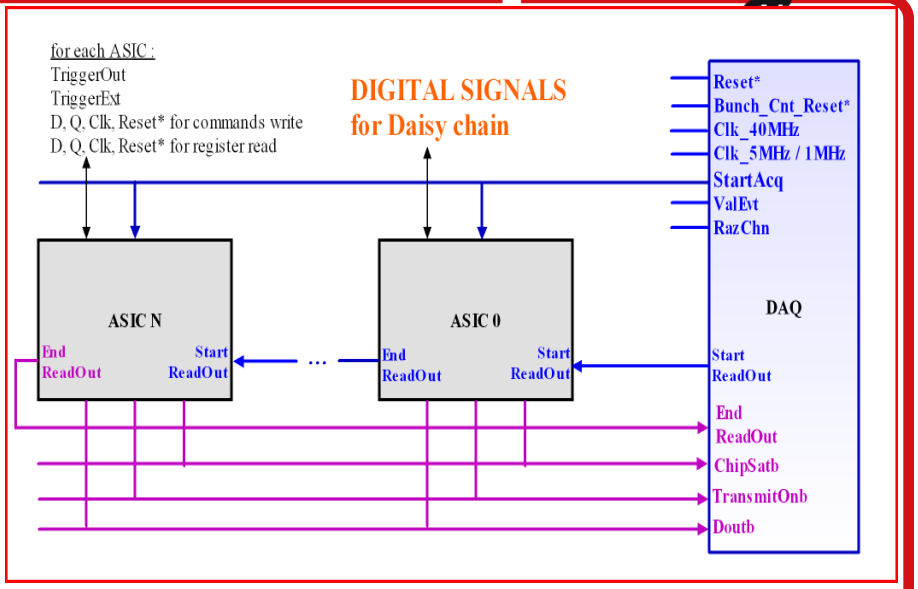
Data bus



DAISY CHAIN: only 6 signals

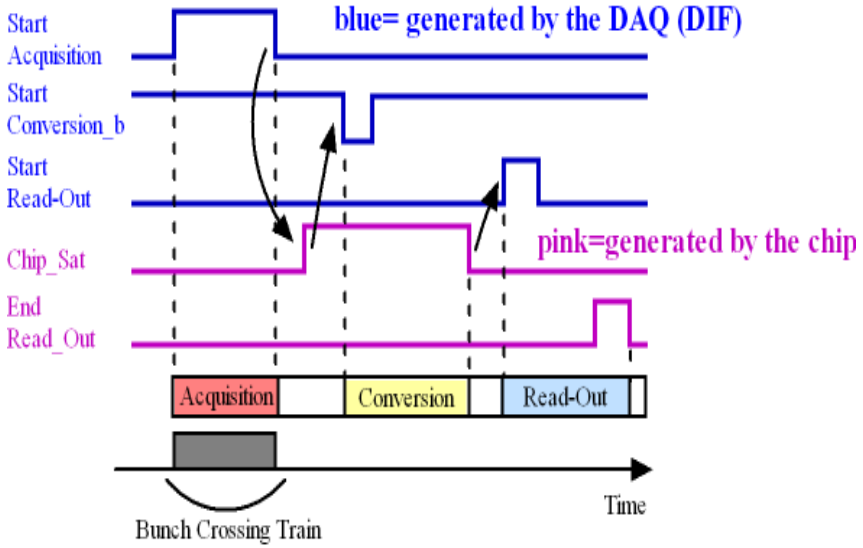
- **COMMON to all the ROC chips**
  - **StartAcq**
    - Start acquisition, generated by DAQ
  - **StartReadout:**
    - Generated by DAQ, start of the readout
  - **EndReadout**
    - Generated by chip, End of the readout
  - **ChipSat** (**O**pen **C**ollector signal):
    - Generated by chip, « 1 »: digital memory is full or acq finished
  - **Dout:** data out (OC signal)
  - **TransmitOn** (OC signal)
    - Generated by chip, Data out are transmitted
- Buffers integrated for OC signals





ILC

No conversion in Hardroc



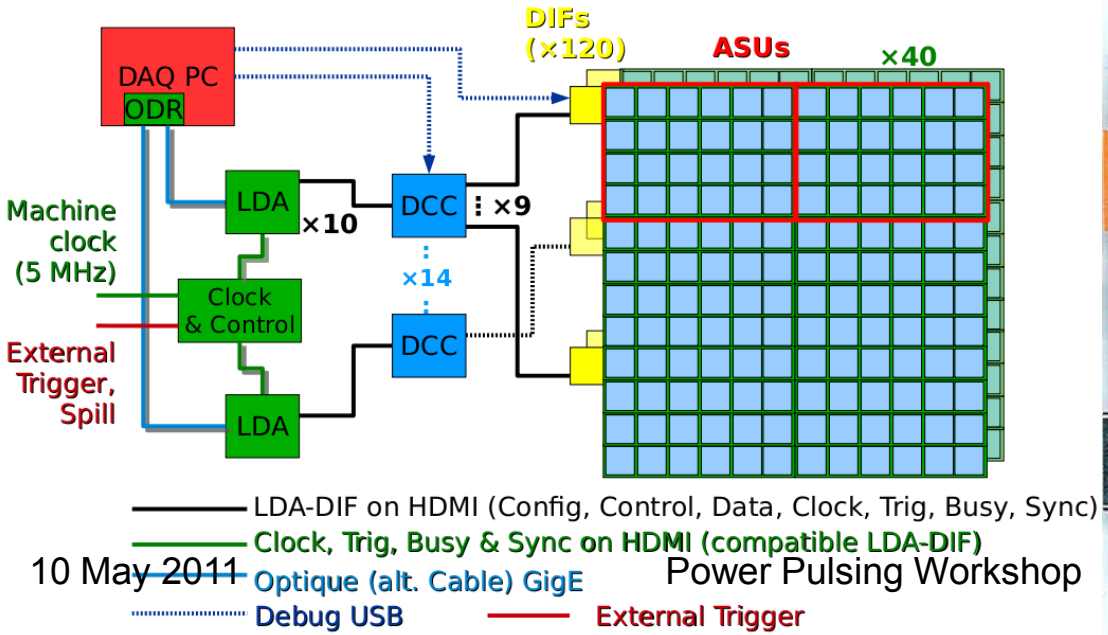
INTERFACE DAQ-ROC= DIF board

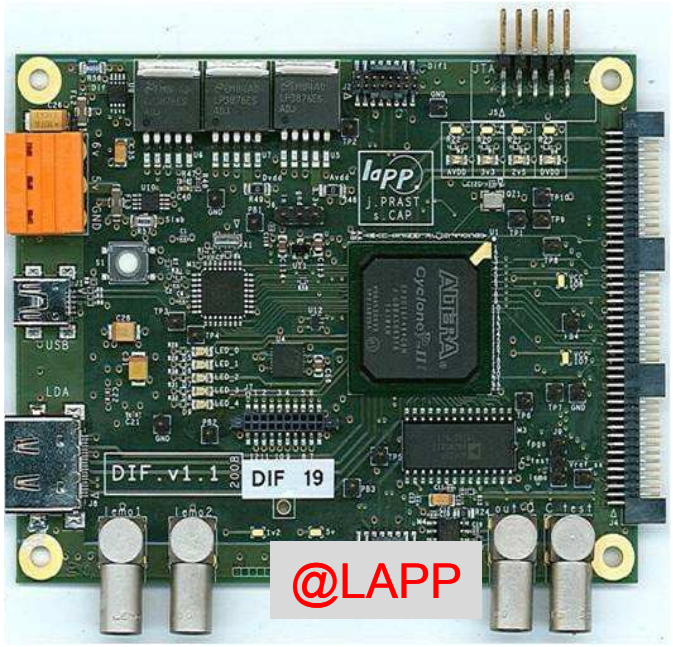
- Reception of the Slow Control parameters from a PC and transmission to the ASICs, launch acquisition, perform analog/digital readout and send all the data received from ASICs to a PC.

- Communication
  - with other DIFs
  - with DAQ either by USB or by HDMI

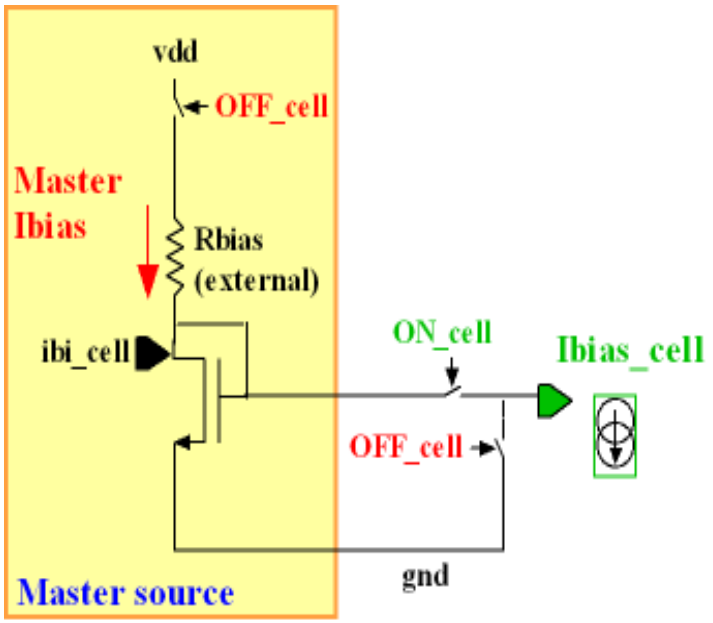
- The DIF should be able to handle more than 100 ASICs theoretically. The max which has been tested is 48

- **Regulators + Decoupling capacitors located on the DIF**

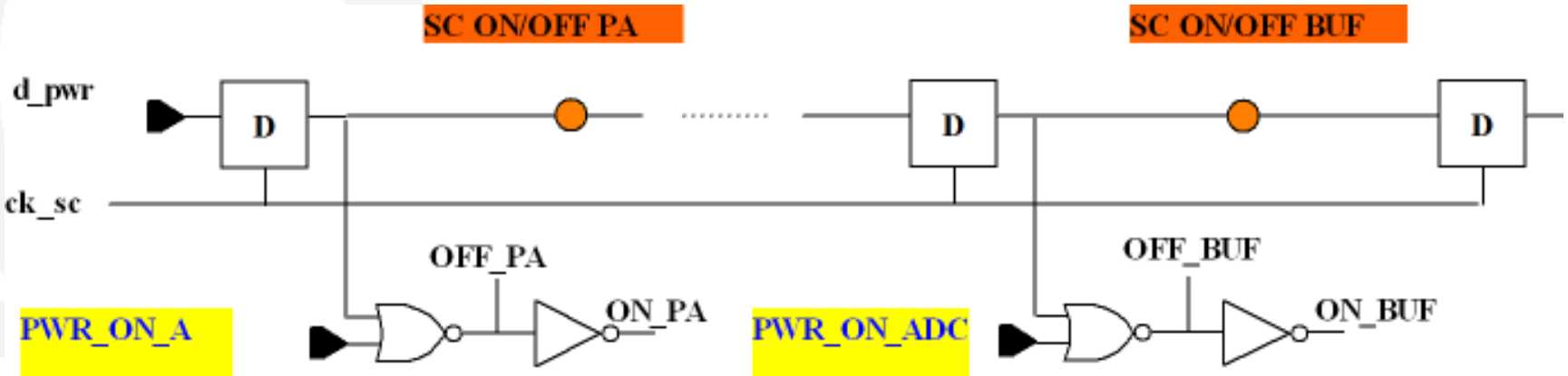




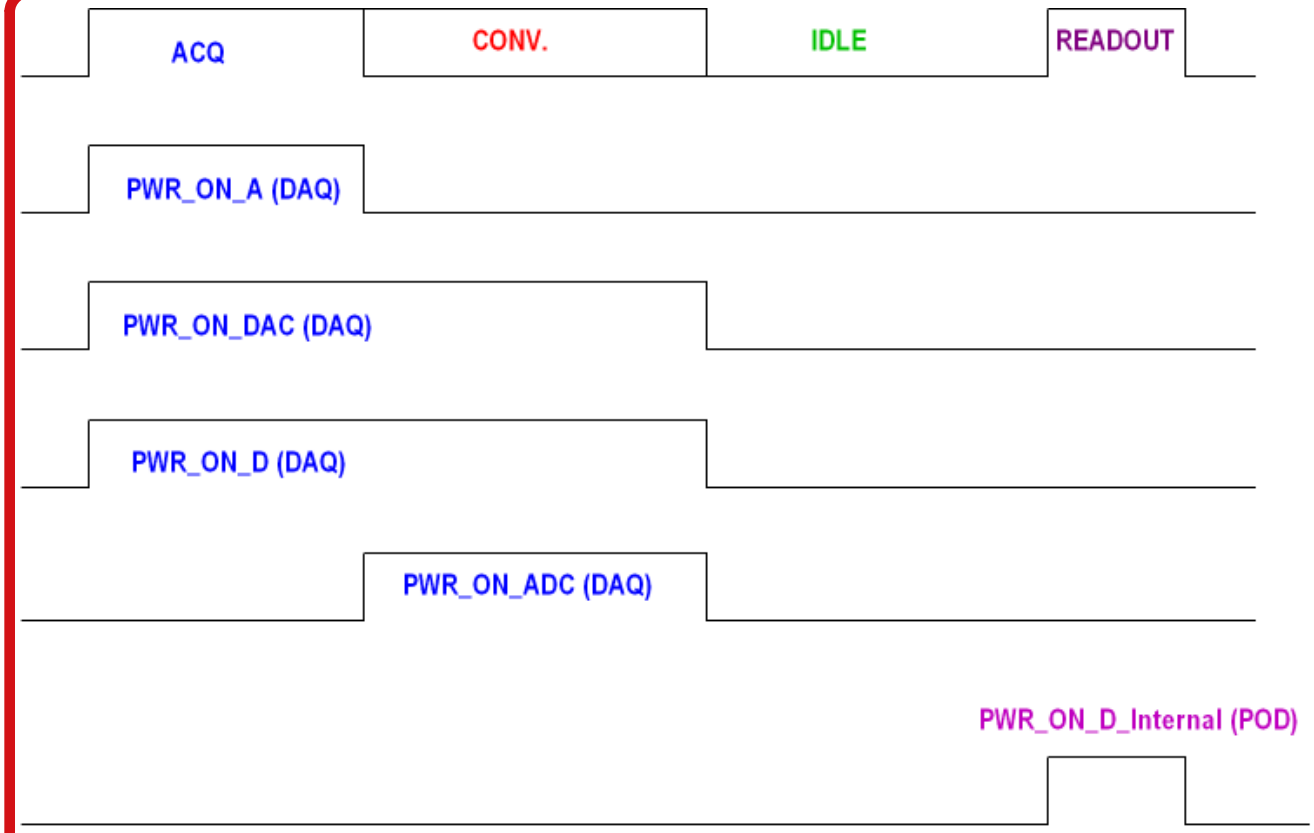
ILC ROC CHIPs: POWER PULSING



- **Power pulsing:**
  - Bandgap + ref Voltages + master I: switched ON/OFF
  - **Shut down bias currents and reference voltages with vdd always ON**
- **4 Power pulsing lines handled by the DAQ** : analog, conversion, dac, digital
  - Most of the power in pwr_on analog
- Each stage can be forced **on/off by slow control**



Power pulsing lines timing



CONVERSION:

HARDROC2: NO conversion

SPIROC2: max time (Full chip)= 16 SCAx 2 (HG or LG/Time) x103 µs=3.2ms

SKIROC2: max time (Full chip)= 15 SCA x2 (HG or LG/Time) x103 µs= 3 ms

READOUT:

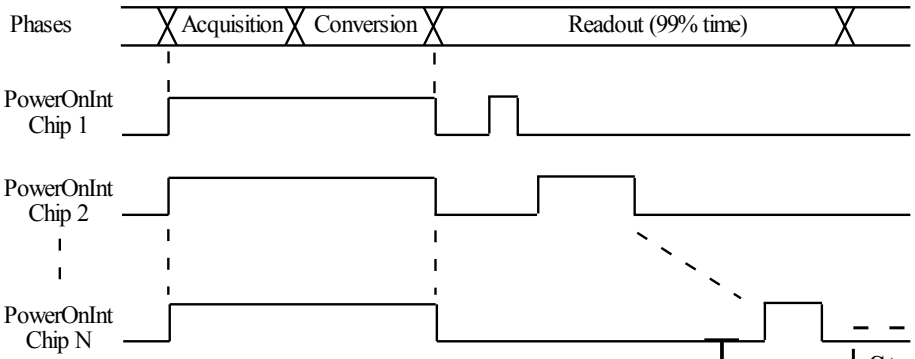
HARDROC2: 127 (memory depth)x [64 channelsx 2 trigger bits + 24 BCID bits + 8 Header bits]=20 320 bits => 200 nsx20k=4 ms/ Full Chip (WORST case)

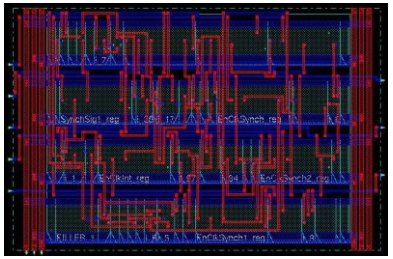
SPIROC2: 16 SCAx2 (HG or LG/Time) x 36 ch x 16 ADC bits + 16 SCAx16 BCID bits + 16 Header bits= 18 704 bits => 3.8 ms/Full Chip (Worst case)

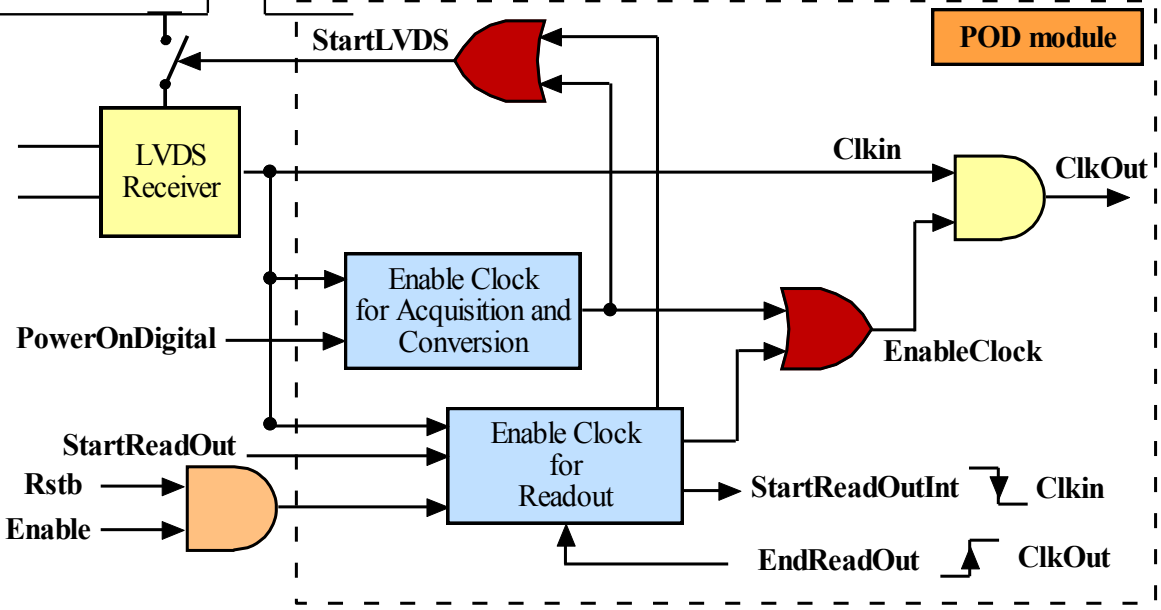
SKIROC2: 15 SCAx2 (HG or LG/Time) x 64 ch x 16 ADC bits + 15 SCAx16 BCID bits + 16 Header bits= 30 976 bits => 6 ms/Full Fhip (Worst case)

Power On Digital Module: POD

- POD module ("Clock-gating") to handle for the 2 LVDS receivers clock (40 MHz and 5 Mhz) and save power:
  - Starts and stops the Clocks, switches OFF LVDS receivers bias currents



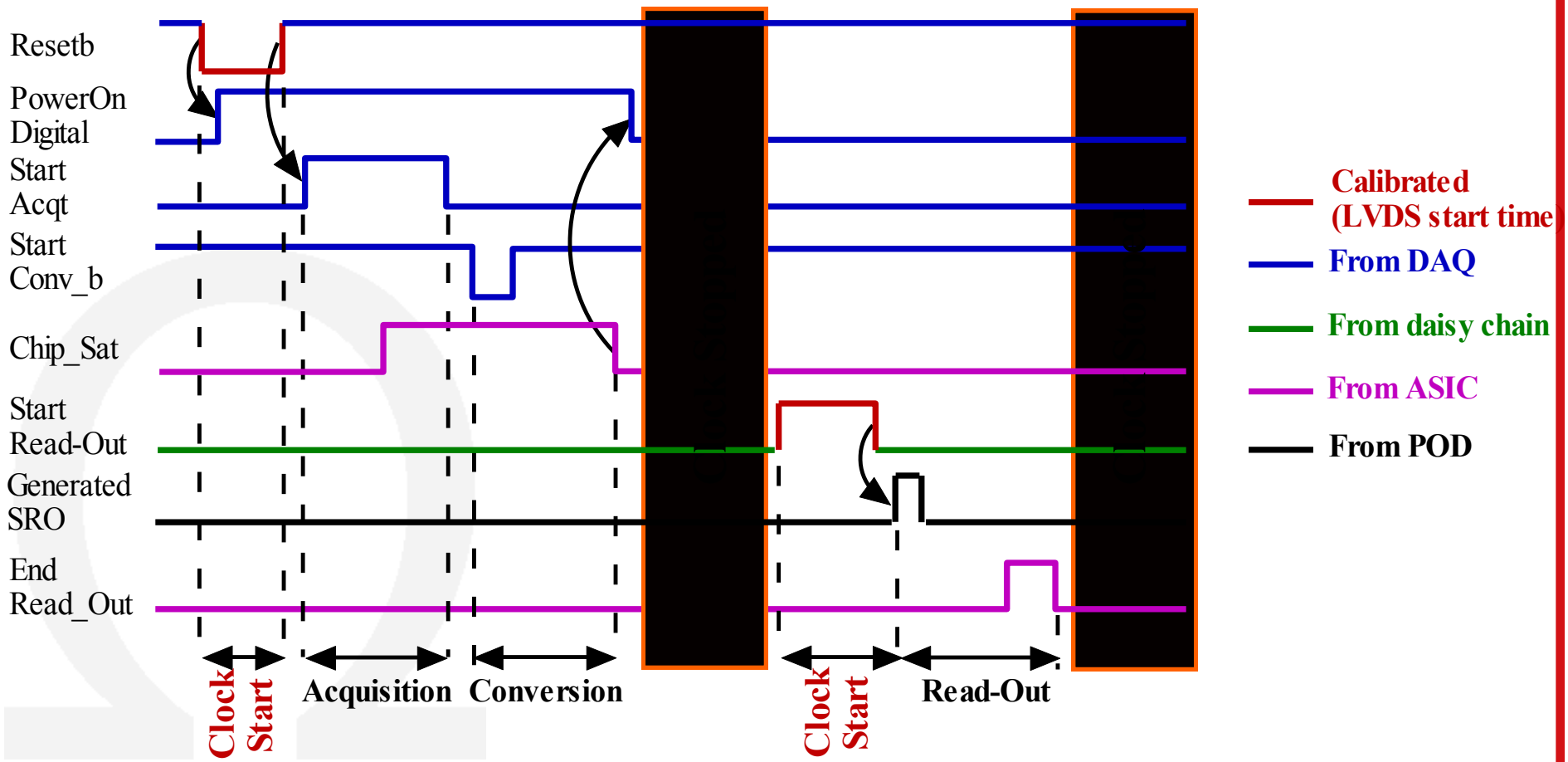




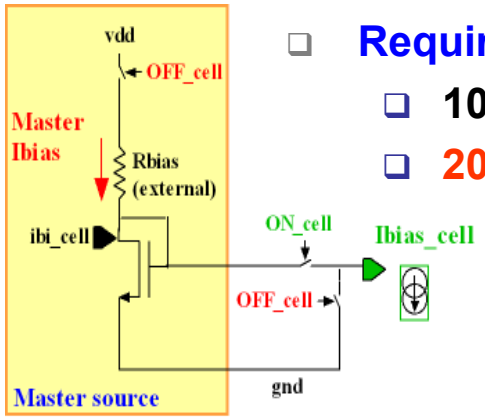
2 others LVDS receivers (RazChn/NoTrig and ValEvt) active during PowerOnAnalog (during bunch crossing)

Power On Digital Sequence

- **End of Conversion**: clocks stopped as not needed and LVDS receivers bias switched OFF
- **Readout**: Start ReadOut signal generated by the POD and stands for a PwrOnD => starts LVDS receivers and Clk.
- **End of the ReadOut**: The chip generates a EndRout signal which will be used by the next chip in the daisy chain to be read out.



POWER PULSING: HARDROC example

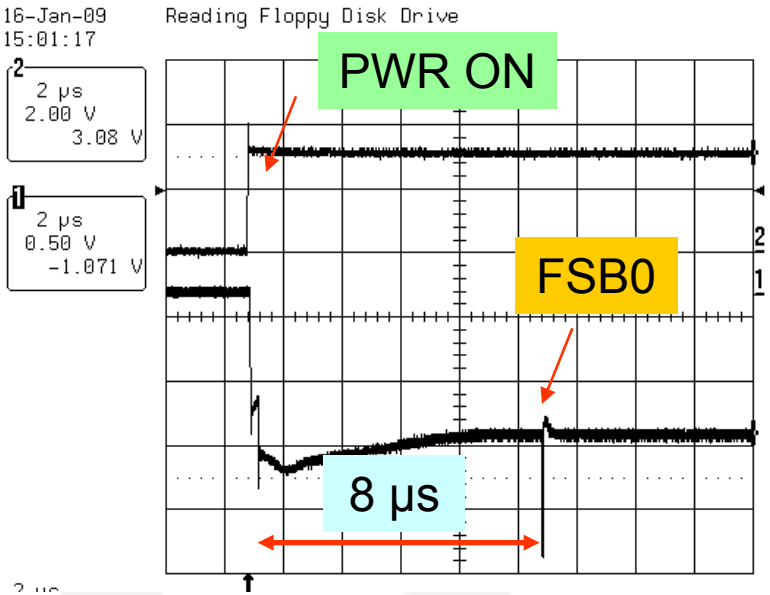


- **Requirement:**
  - **10 µW/ch with 0.5% duty cycle**
  - **200 µA for the entire chip (64 channels)**
- **Power pulsing:**
  - Bandgap + ref Voltages + master I: switched ON/OFF
  - **Shut down bias currents with vdd always ON**
- **HR2 power consumption measurement:**
  - 29 mA x 3.3V ≈ 100 mW => **1.5 mW/ch**
  - **7.5 µW/ch with 0.5% duty cycle**

HR2	ON
Vdd_pa	5.5 mA
Vdd_fsbx3	12.3 mA
Vdd_d0,1,2	7.3 mA
Vdd_bandgap	1.2 mA
Vdd_dac	0.84 mA
Vddd	0.67 mA
vddd2	0.4mA (=0 if 40MHz OFF)
Total (noPP)	29 mA
Total with 0.5% PP	145 µA

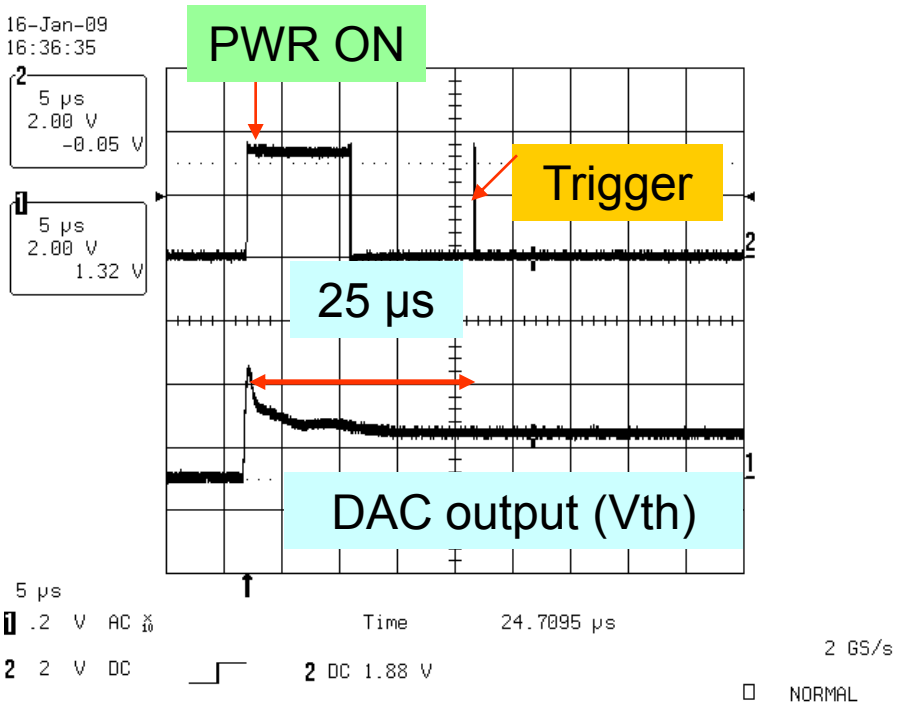
Pwr_on_a alone	26.5mA
Pwr_on_dac	1.0 mA
Pwr_on_d	1.0 mA
ALL OFF	<4µA

POWER PULSING: « AWAKE TIME »



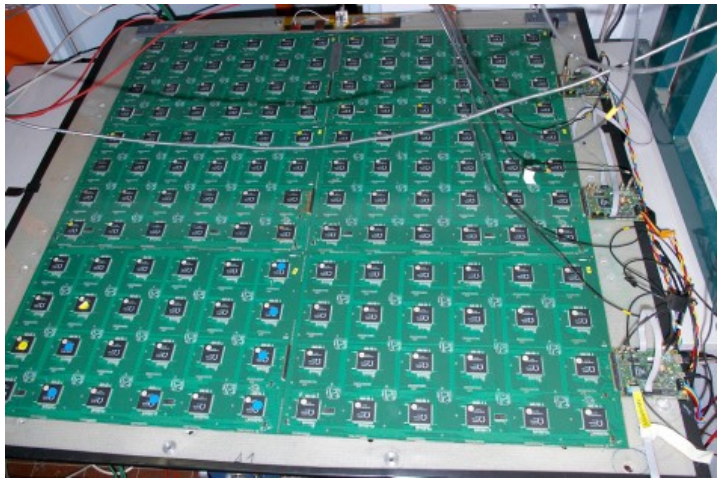
- **All decoupling capacitors removed on bias voltages**
- PWR ON: ILC like (1ms,199ms)
- PP of the analog part:
  - Input signal synchronised on PWR ON
  - Awake time= 8 µs

- **Power pulsing of the 10 bit-DAC:**
  - **25 µs (slew rate limited)**



SDHCAL: POWER PULSING in TESTBEAM

See Robert Kiefer's talk



1 m²
PADs 1x1 cm²

1 m² associated to GRPC detector in test beam

Semi-digital electronics readout system validated in beam conditions (daisy chain, stability, efficiency, no external component)

Power pulsing was successfully tested on a 24-ASIC electronic board. The board associated to a GRPC was also successfully tested in a 3-Tesla B field in June (SPS-H2)

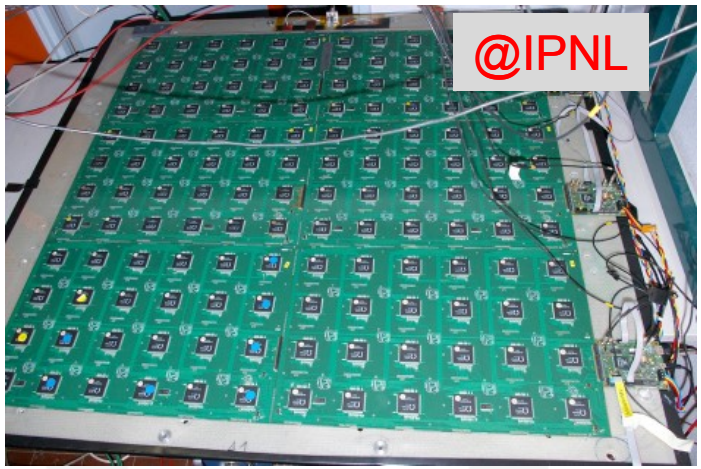
Daisy chain measurement

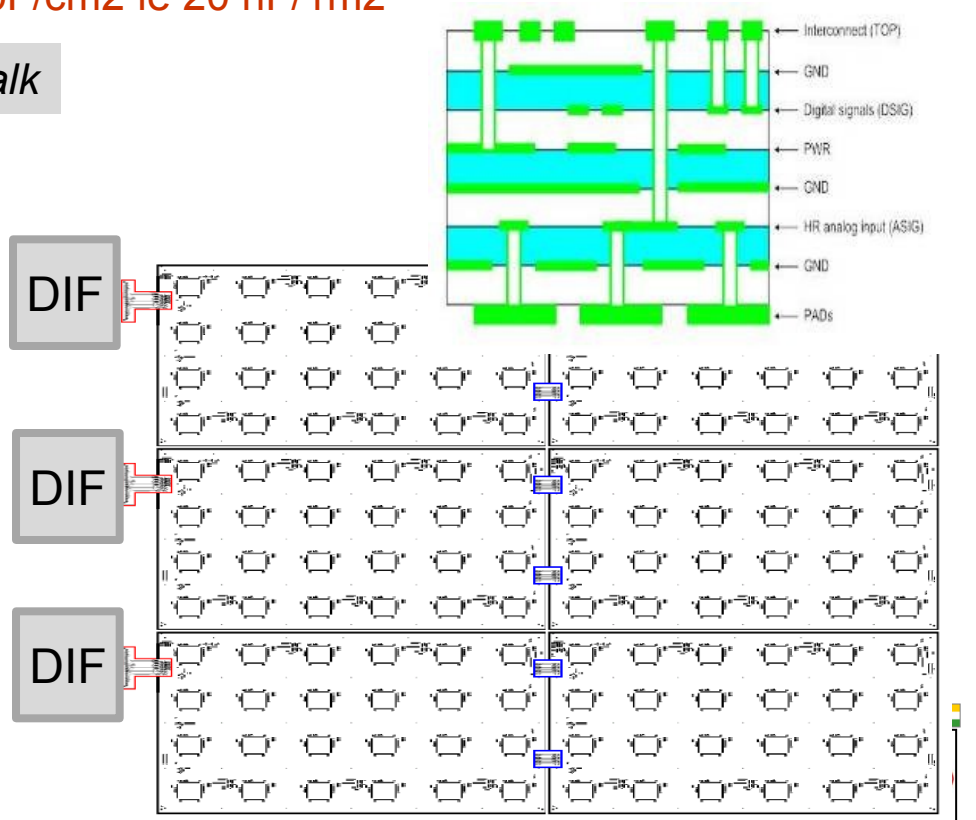
Readout frame:
Header (8bits), then BCID (24bits),
then 128 bits for trig0<0-63> and trig1<0-63>

ILC ROC CHIPS: POWER and DECOUPLING

- DHCAL: 7.5 µW/ch => 2.5 µA/ch => <>=25 mA/m2 (10 000 channels/m2)
- 2AA battery: 1500 mAh => 60 hours
- I peak=5 A during 1 ms acquisition => need of energy storage, ΔV=1V (regulators) => C=Idt/dV =5 mF, on the DIF.
- DHCAL/AHCAL 100 nF (for HF decoupling) possible near the chip, ECAL: 0 external components => decoupling C at the edges (DIF board)
- Decoupling vdd/gnd on PCB= About 20 pF/cm2 ie 20 nF/1m2

See Remi Cornat's talk

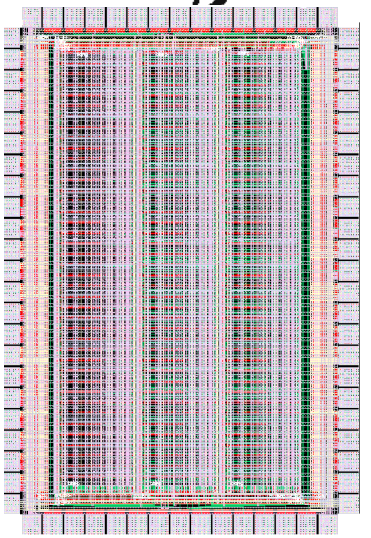


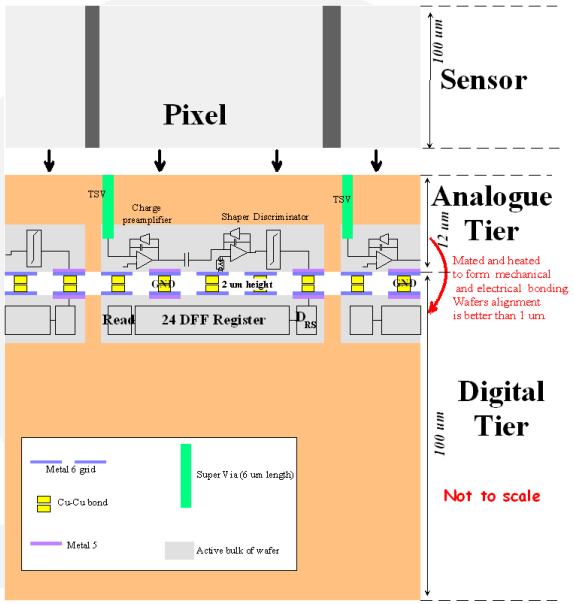


Ultra low power:
60h operation for 10 000 channels with a 2 AA battery

OMEGAPIX: 3D ATLAS pixels at SLHC

- Double tier pixel readout for ATLAS sLHC
  - 50x50 µm pixels, 64x24 readout channels:
    - **Low power 3 µW/ch**, low threshold 1000e-=0.160 fC
      - Target Cd = 100 fF, Pd=3µW, Gain : 50 mV/1000 e-, ENC=100 e-
  - Analog tier: preamp, shaper, discri
  - Digital tier: shift register with a read logic in each ch
  - decrease of digital activity by handling the digital data after Level 1 trigger (dynamic memory)
  - Chartered (130 nM CMOS)/Tezzaron run may 2009
  - Collab with CPPM and LPNHE





	FEI4	LAL
Pixel size	50 x 250	50 x 50
Pixel capacitance	250 fF	80 fF
Array size	64 x 320	
DC leakage tolerance	100 nA	10 nA
noise	300 e-	100 e-
Threshold	2000 e-	1000 e-
Threshold dispersion	100 e-	100 e-
Power dissipation (analog)	12 µW/ch	2 µW/ch
Power dissipation (digital)	12 µW/ch	1 µW/ch
Max trigger rate	200 kHz	
Radiation tolerance	200 Mrad	
Charge measurement	4 bits	

JEM/EUSO : SPACIROC ASIC

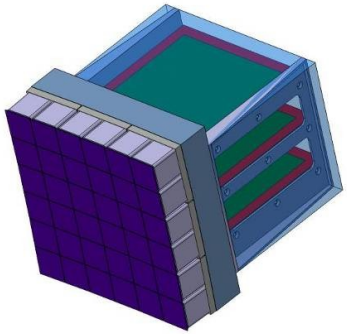
ASIC Functions:

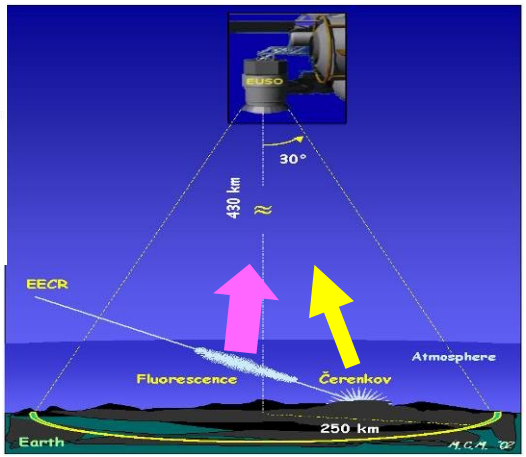
Analog part:

1. Photoelectron counting @100MHz (implemented LAL)
2. Time Over Threshold (collab. JAXA/Riken)

Digital part (LAL):

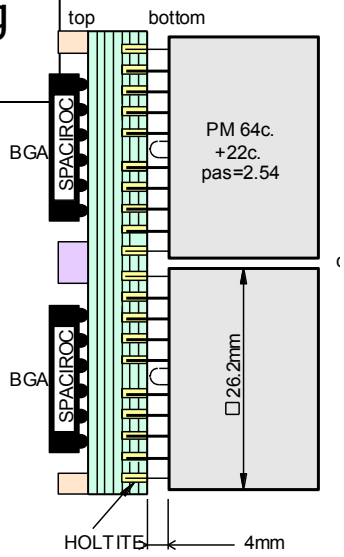
1. Digitization,
2. Memory,
3. Send data to FPGA for triggering

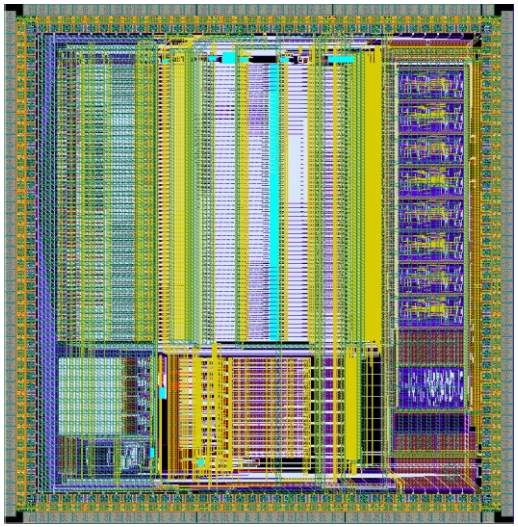




Crucial points

- Power consumption < 1 mW/ch
- data flow ~ 384 bits / 2.5 µs
- Radiation tolerance

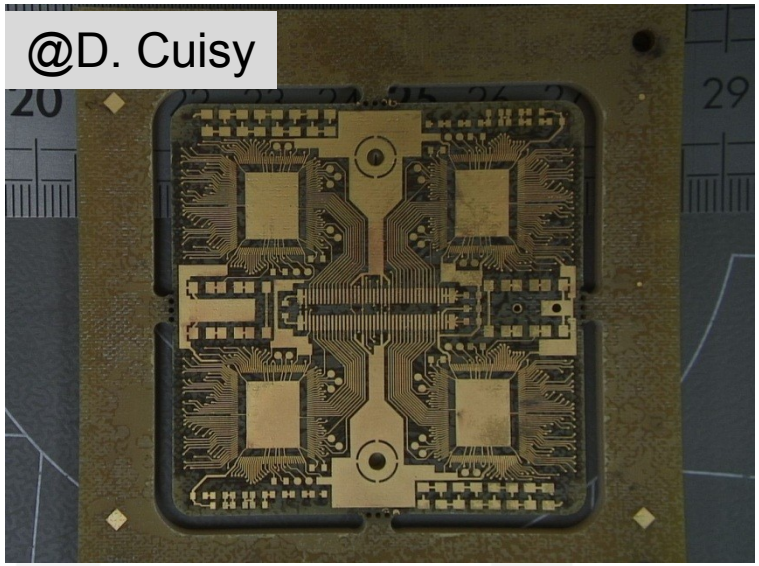


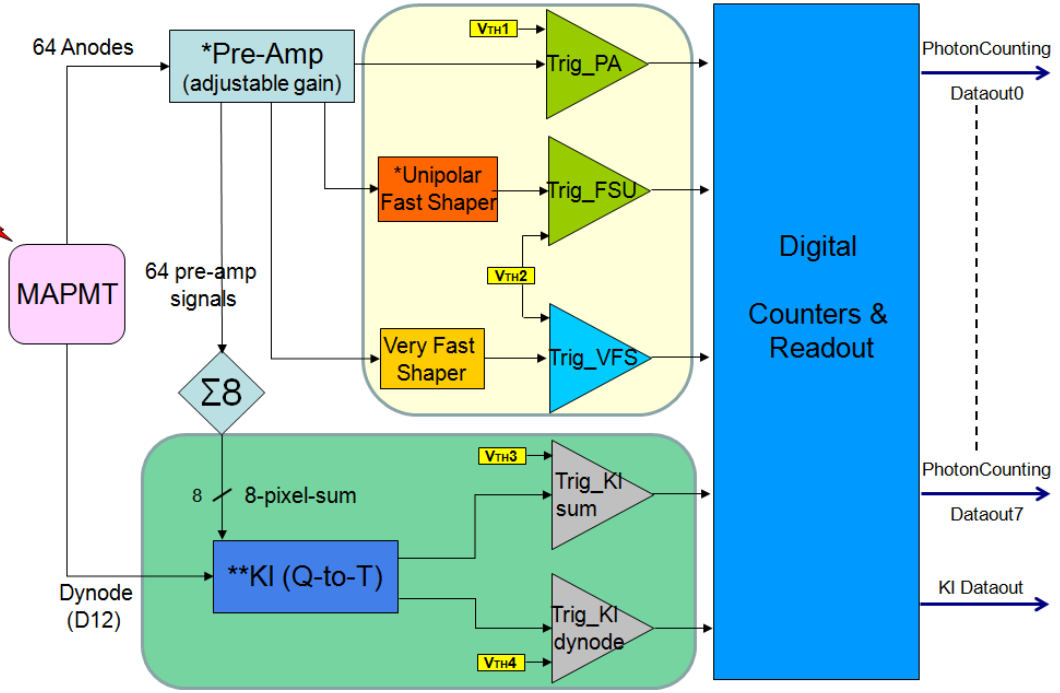


SPACIROC: power reduction

1- Silicon Germanium 0.35 µm BiCMOS
technology => High speed and low power

2- Digital processing inside the chip





Specifications:

- Consumption: 1mW/channel
- Photon counting: 100% trigger efficiency@50fC (1/3pe, 10^6 Gain)
- KI input range : 2pc – 200pc (??10pe - 100pe)
- Radiation hardness
- Data out : Startbit + 64 bits + Parity

CONCLUSION

- LOW power = key issue for ILC design
  - Power pulsing integrated at chip level
    - Now been demonstrated at detector level with the DHCAL (No ADC)
    - Will be more difficult with Spiroc and Skiroc : 12 bits ADC
  - Next generation of ROC chips: channel handled individually, 0 suppression
- When power pulsing is not possible:
  - Low power at the design level
  - Silicon Germanium technology
  - Digital processing inside the chip

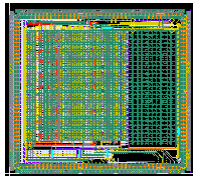
Backup slides

ILC ROC CHIPs: POWER PULSING

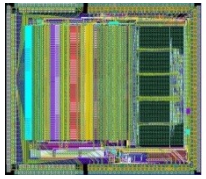
Calorimeter	Sensitive Medium	Absorber	Granularity	Number of Channels	Readout Chip	Consumption (PowerPulsed)
Si-W ECAL (ILD oriented)	Silicon Diodes	Tungsten	0.5x0.5 cm^2	≈100M	**SKIROC**	25µW/ch Tot: ≈2500W
Si-W ECAL (SiD oriented)	Silicon Diodes	Tungsten	0.13 cm^2	≈73M	KPiX	<20µW/ch Tot: <1460W
Scint-W ECAL (ILD oriented)	Scin. Tiles + SiPM	Tungsten	0.5 x 4.5 cm^2	≈11M	**SPIROC**	(25+7)µW/ch Tot: ≈352W
AHCAL	Scin. Tiles + SiPM	Iron	3x3 cm^2	≈8M	**SPIROC**	(25+15)µW/ch Tot: ≈320W
SDHCAL (ILD oriented)	GRPC or µMegas	Iron	1x1 cm^2	≈50M	**HARDROC**	7.5µW/ch Tot: ≈375W
DHCAL	GRPC	Iron	1x1 cm^2	≈50M	DCAL III	<4 mW/ch No Pow. Puls. Tot: <20kW

@Robert Kieffer

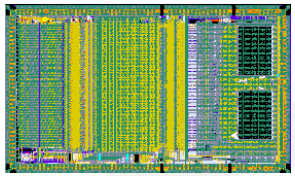
ROC chips for ILC = System On Chip



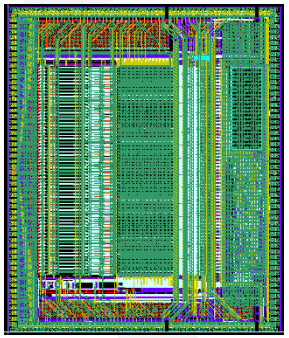
- HARDROC/MICROROC for SDHCAL: 64 channels to readout RPC or µmegas)
  - Auto trigger on 10fC (2fC) up to 10 pC (500fC),
  - Semi digital readout (3 thresholds, 2bits-encoding)
  - 5 0.5 Kbytes memories to store 127 events
  - Pulsed power: **10 µW/ch** (0.5 % duty cycle)



- SPIROC for AHCAL: 36 channels to readout SiPM
  - Autotrigger on MIP or spe (150 fC)
  - 16 depth SCA for Charge measurement (up to 300 pC) and Time measurement (< 1 ns)
  - 2 memories of 2K bytes to handle Charge and Time measurements from the internal ADC
  - Internal 12 bit ADC/TDC
  - Pulsed power: **25 µW/ch** (1 % duty cycle)



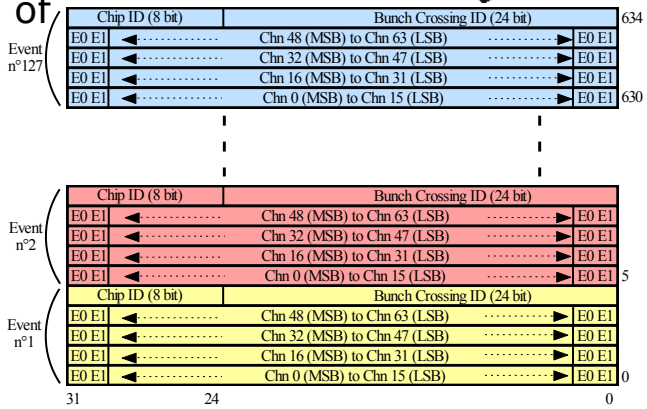
Physics simulation: 2 or 3 SCA are enough



- SKIROC for ECAL: 64 channels to readout Si-W
  - Autotrigger on MIP (4 fC)
  - 15 depth SCA for Charge measurement (2500 Mip=10 pC) and Time measurement (< 1 ns)
  - 1 memory of 4K bytes to handle Charge and Time measurements from the internal ADC
  - Internal 12 bit ADC/TDC
  - Pulsed power: **25 µW/ch** (1 % duty cycle)

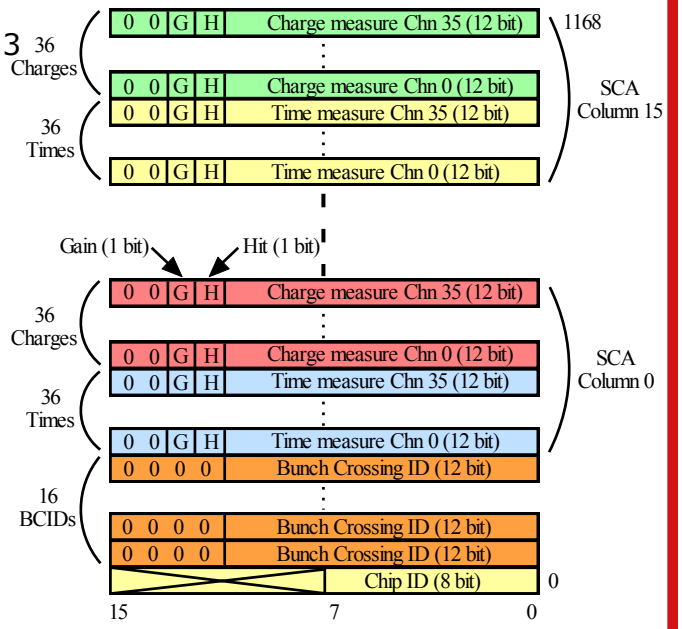
MEMORY MAPPING of the ROC CHIPs

- HARDROC2: 127 events on 2 bits for 64 channels. Maximum of stored data is 20320 bits
  - No conversion
  - Readout worst case: 200 nsx20k=4 ms/ Full Chip (WORST case)

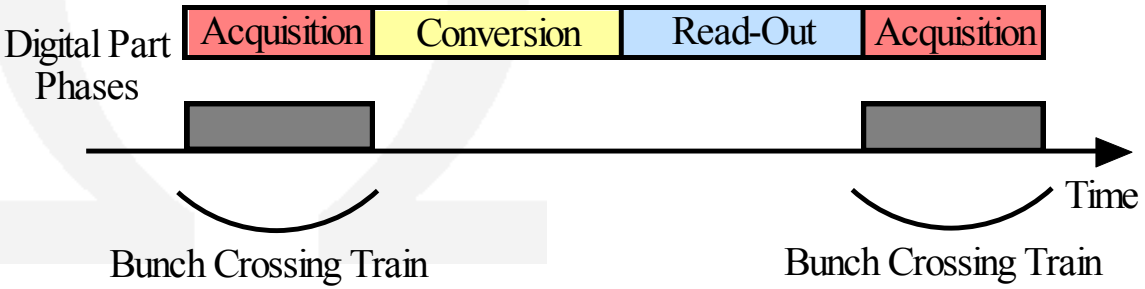


- SPIROC2: 16 events, 36 channels. 12 bits ADC for time and charge => max stored data= 18707 bits
  - Conv.: max time (Full chip)= 16 SCA x 2 (HG or LG/Time) x103 µs=3.2ms
  - RO: 3.8 ms/Full Chip (Worst case)

- SKIROC2: 15 events, 64 channels. 12 bits ADC for time and charge => max stored data= 30976 bits
  - Conv.: max time (Full chip)= 15 SCA x2 (HG or LG/Time) x103 µs= 3 ms
  - ReadOut: 6 ms/Full Fhip (Worst case)

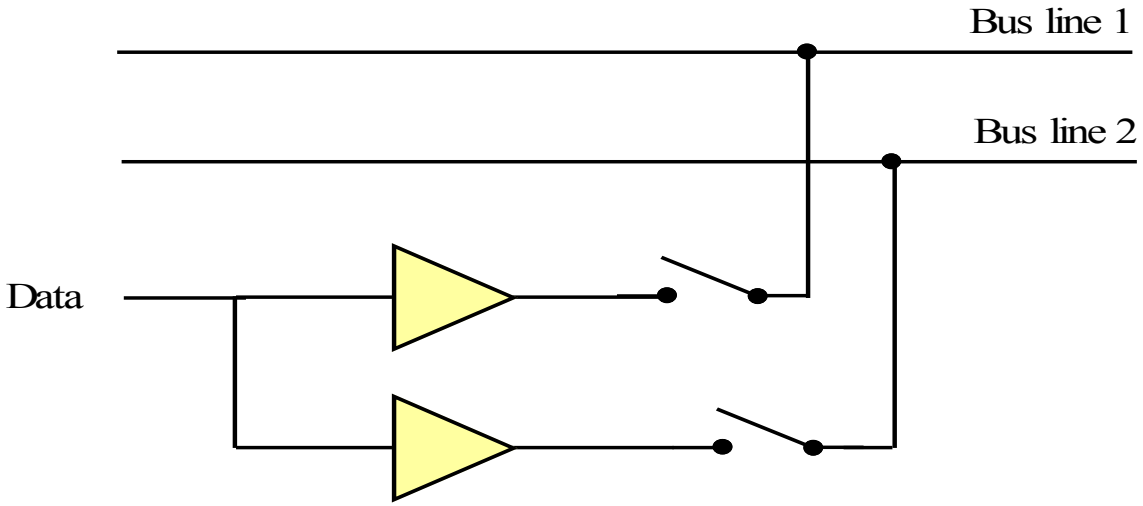


Physics simulation: 2 or 3 SCA are enough



Doutb and TransmitON: Redundancy and bypass of the OC lines

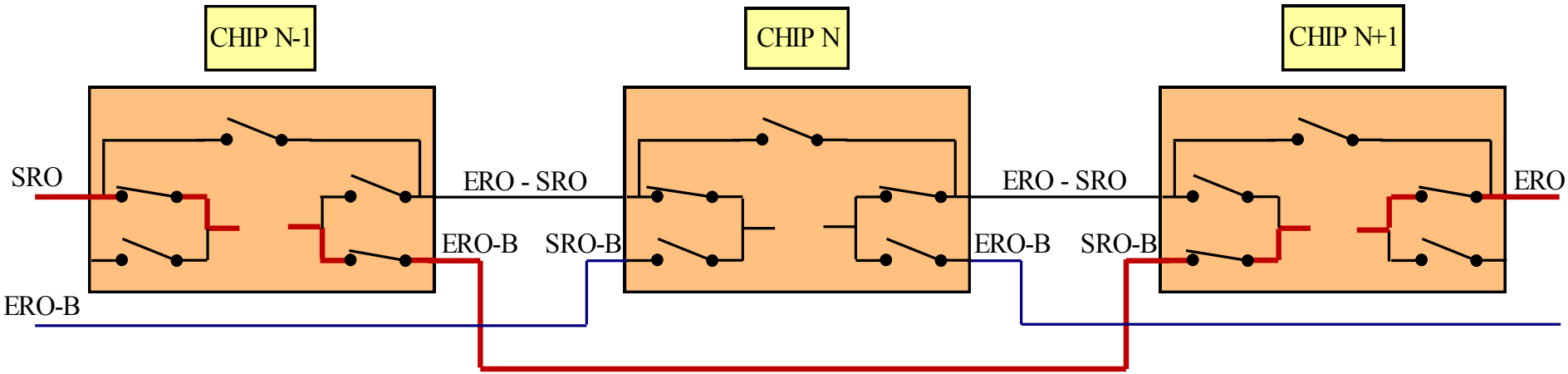
- 2 data line/chip (Dout1b and Dout2b), chosen via SC
- 2 TransmitOn lines /chip
- Each one is removable from bus line by SC



- Allow to remove one buffer that stick the bus line

StartReadOut and EndReadOut: redundancy and bypass

- Add bypass for these 2 signals (SRO, ERO ➔ SRO-B, ERO-B).

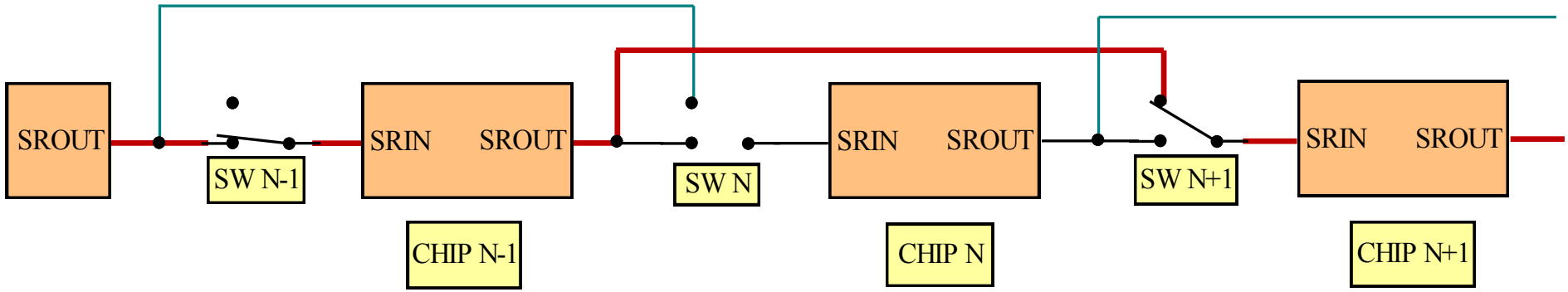


In red, StartReadOut and EndReadOut flow if chip “N” fails

- Chip N can bypass itself by SC
- Chip “N-1” and chip “N+1” can bypass chip “N” by SC
- If Chip N fails :
  - Chip N-1 sends EndReadOut signal on EndReadOutBypass
  - Chip N+1 reads StartReadOut signal on StartReadOutBypass

Slow Control: bypass

- Add bypass jumpers on PCB



In red, SC flow if chip “N” fails

- Default position is chip “N” reads chip “N-1”
  - If Chip N fails :
    - Switch N removed
    - Switch N+1 ➔ in position to read chip “N-1”