Vertex Detector and Silicon Tracker Power Delivery and Pulsing Considerations

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Motivations for Optimizing Power Delivery

- At least three design considerations are closely linked: the material budget, cabling material, and cooling.
  - Higher cable mass ➔ More efficient cabling ➔ Worse material budget
  - Lower cable mass ➔ Less efficient cabling ➔ More heat to remove ➔ More cooling system mass (possibly) ➔ Worse material budget
- We need to consider all three and also see if alternative approaches, such as power cycling, DC-DC conversion, and serial powering, can lessen the impact of the linkages.
- Naturally, lower power needs by the tracker and vertex detector would be even more helpful.

Motivations for Optimizing Power Delivery

- Material budget
  - The goal for material in a vertex detector layer was 0.1% X0 for SiD.
  - CLIC is considering a more realistic goal of 0.2% X0.
  - For the silicon tracker, the SiD goal was ~0.9% X0 per layer.
  - Contributions to the budget from cables and power control devices can easily exceed the goals and need to be minimized.
  - The net effects of excess material are the production of secondaries, which complicate track finding and reconstruction, and multiple scattering, which worsens momentum resolution.
- Heat removal
  - To limit material, air cooling has been assumed for vertex detector and tracking elements within the fiducial volume.
  - The required air flow rates are high from the start and become higher when power delivery losses are considered.
    - We need to optimize power delivery to minimizes those losses.
  - Though alternatives to air cooling may turn out to be needed in portions of the detector, those portions should be minimized and located to minimize their impact.
- Cost and convenience are considerations, but the first two issues are critical.

Issues

- What power dissipation per unit area should be assumed?
- Should there be power cycling?
  - If so, where should the devices to do it be located?
    - Power cycling capability is built into the KPIX chips for the SiD tracker.
    - Is it practical to include it in CLIC sensors or should it be external to the sensors?
    - Are vibrations induced by power cycling?
- Should there be serial power?
  - If so, where should the devices to do it be located?
  - What is the reliability?
  - Are electrical noise or vibrations induced by serial power?
- Should there be DC-DC converters?
  - If so, where should the devices to do it be located?
  - What is the reliability?
  - Are electrical noise or vibrations induced by DC-DC converters?
- In what regions is cooling via gas flow effective?
- Is liquid or two-phase cooling needed for some tracker and vertex detector regions?
- Are vibrations induced by coolant flow?

Tracker Requirements

- Others are far more knowledgeable about TPC cooling requirements. Accordingly, I'll restrict my comments to silicon portions of the tracker and to the vertex detector.
- Early evaluations for the SiD outer silicon tracker for the ILC assumed a power dissipation of 17.4 μW per channel averaged over a pulsed power cycle.
  - Measurements of KPIX prototypes suggested a slightly higher value: 20 μW per channel or ~0.4 milliwatt per cm^2.
  - Pulsed power was based on a ratio of 80 in peak to average power.
  - Though ramping and stabilizing power will be more difficult with the CLIC rep rate of 50 Hz (versus 5 Hz for the ILC), it seems reasonable to assume the same gain in peak to average power.
  - Removing a milliwatt per cm^2 should be straight-forward with air cooling provided good flow paths can be established.
  - Conductors need to be sensibly sized.
  - Locations for devices to control pulsed power need to be determined.
  - Paths for gas flow and gas sources need to be provided.
  - There could be surprises!
- Gas cooling of vertex detector elements, with a significantly higher power dissipation per unit area, presents greater difficulties.

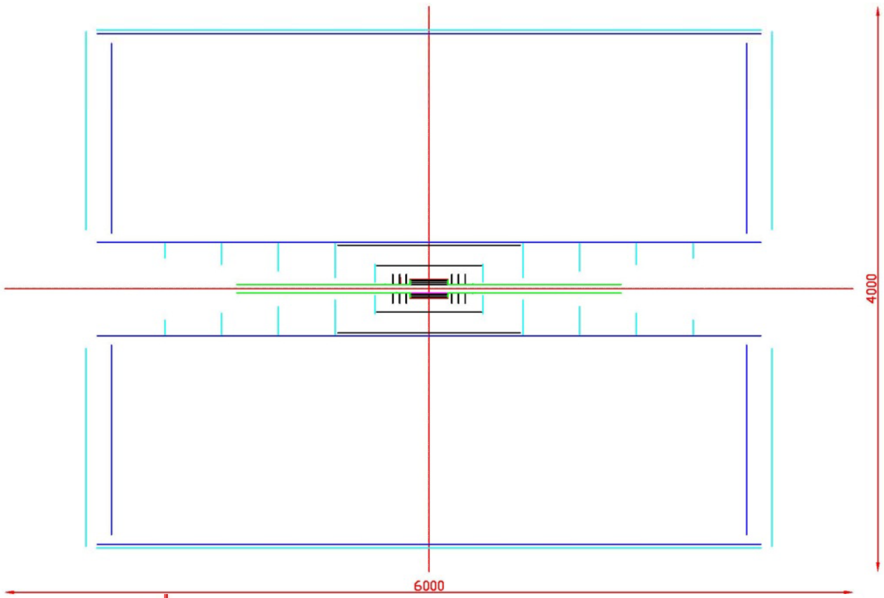
VTX Requirements

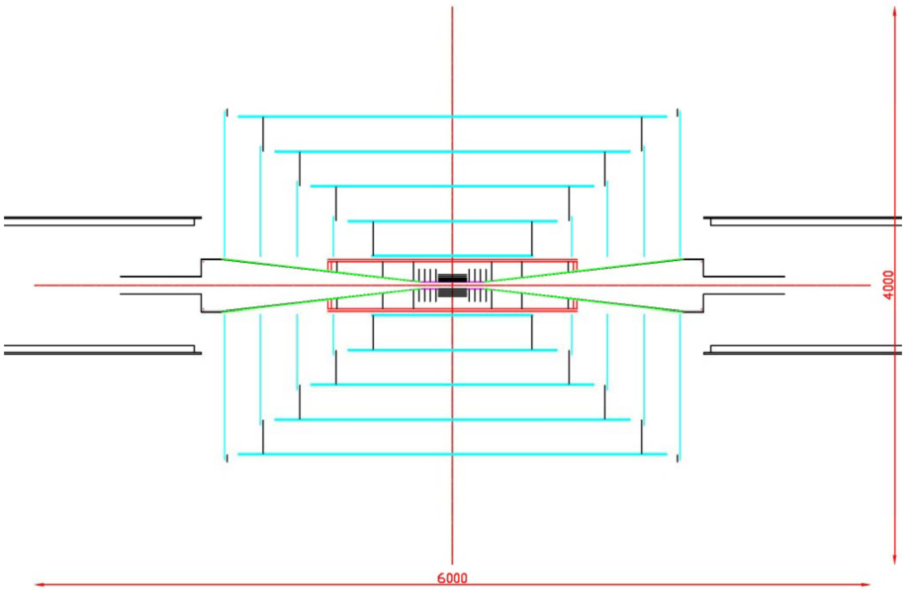
- Power dissipation to be expected in a vertex detector remains less well known.
  - R&D on pixel sensors has been ongoing.
- To provide guidance, heat removal from pixel barrels with sensor layouts similar to that of ILD and SiD were calculated.
- To avoid the need for studies of vibrations associated with forced-flow gas cooling, the calculations assumed that flow along the length of the barrel would be laminar with dry air as the cooling gas.
  - Maximum Reynolds number = 1800
  - That led to a total power for five barrel layers of 20 watts and a power dissipation of ~ 0.0131 W/cm^2.
- More recent estimates suggest that the VTX barrel power dissipation could be as high as 0.1 to 0.13 W/cm^2, or higher by a factor of 7.5 to 10 (~2 W/ladder for SiD VTX Layers 2-5).
- Initial calculations of heat removal via dry air flow have been made assuming 0.13 W/cm^2 and geometries similar to those proposed for the VTX barrel of SiD, CLIC-ILD, and CLIC-SiD.

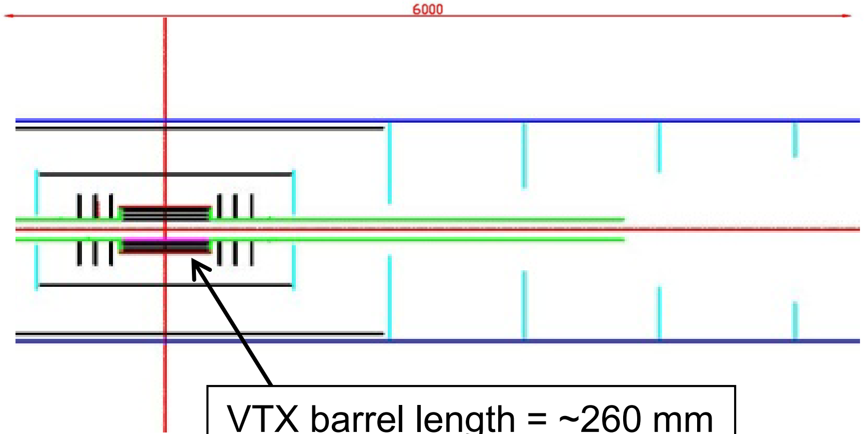
Representative Concept Layouts

- CLIC-ILD at left, CLIC-SiD at right
  - Dimensions are preliminary and under study

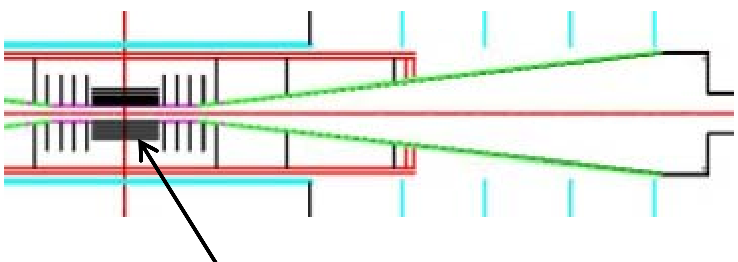
Note that cable paths (in green) vary and are under study.







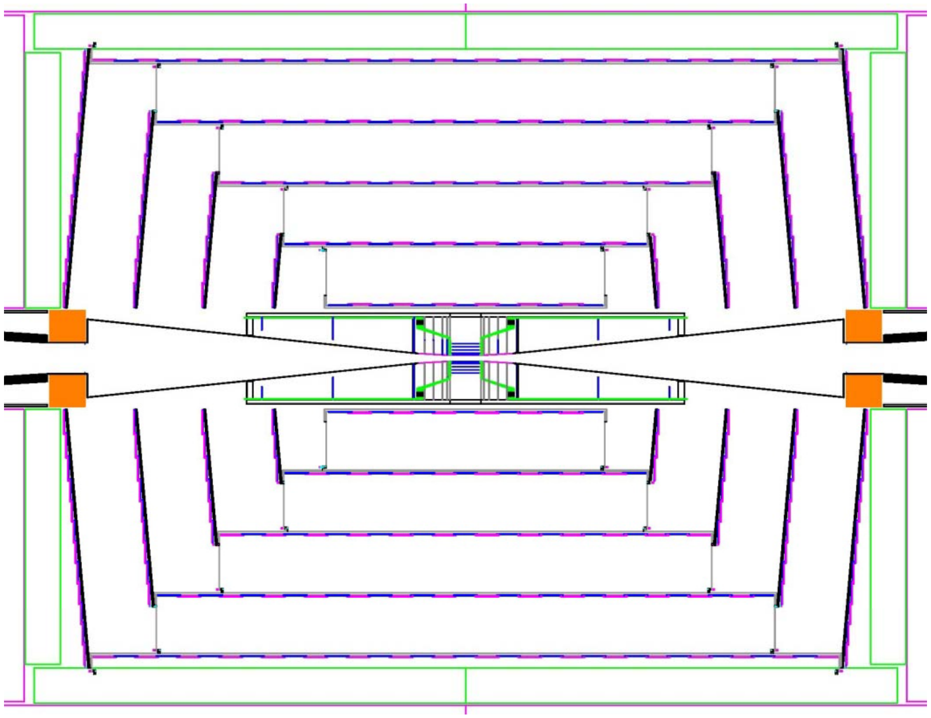
VTX barrel length = ~260 mm

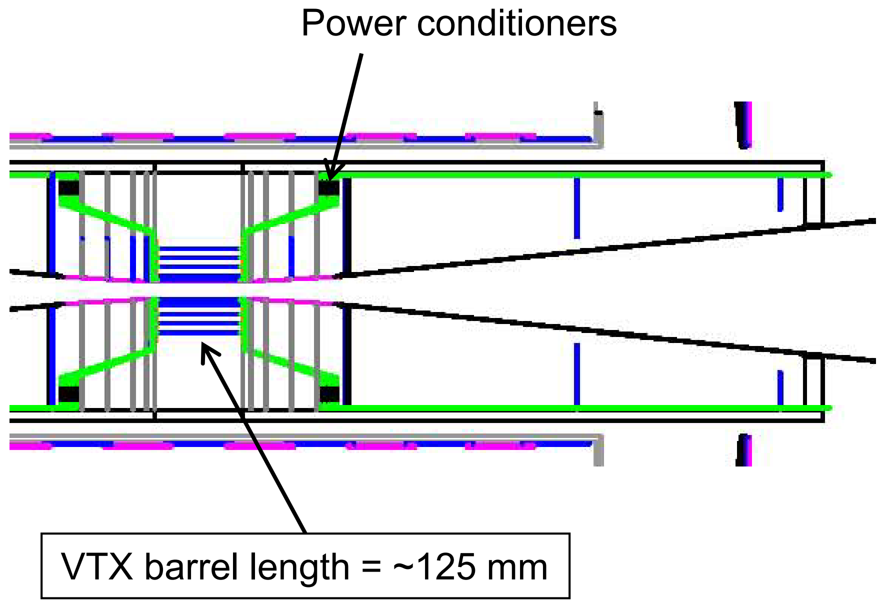


VTX barrel length = ~200 mm

Representative Concept Layouts

- SiD

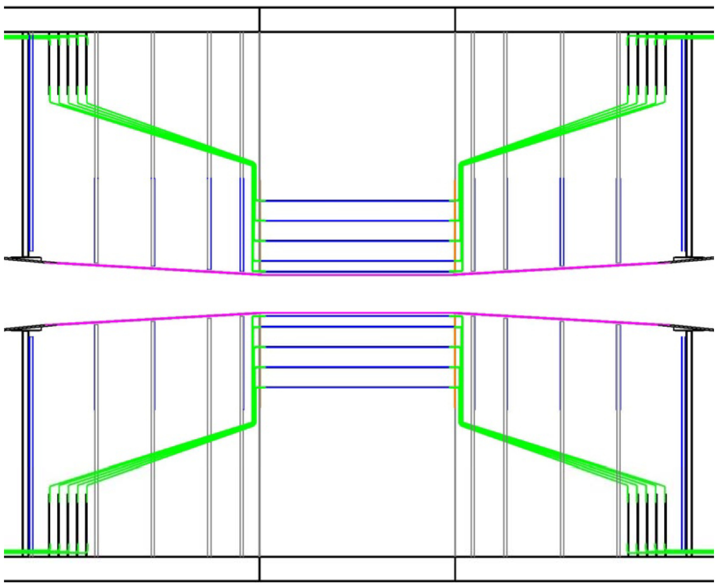




- Note that VTX barrel cables run outboard of the nearest disks.
- Disk cable paths were not determined.

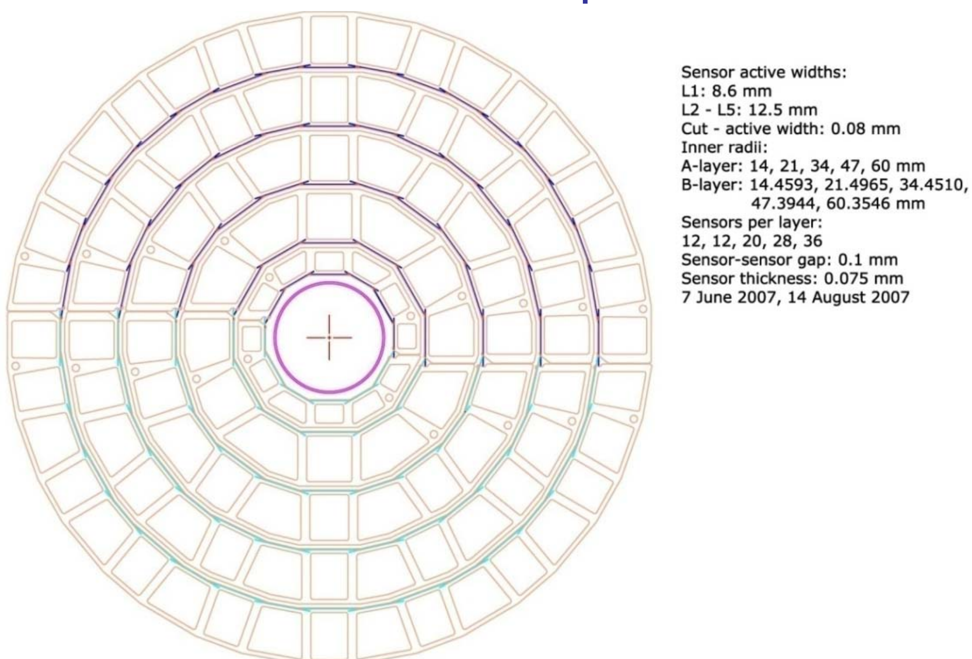
SiD VTX Barrel with Forced Air Cooling

- Gas flow is end-to-end (say left-to-right).
- Gas is delivered via a double-walled outer support cylinder with distribution openings in the inner wall.
- The calculations assume that the available pressure difference to drive flow is independent of the barrel layer, that is, pressure at each end of the barrel is uniform.
  - Not completely correct, since pressure drop from the support cylinder to a given barrel layer is clearly dependent on the location of the layer
  - In addition, cables can obstruct air flow and the gap between the first disk and the barrel end limits flow.
- More detailed and precise calculations can be made, but these calculations should give a reasonable idea of the issues.



Calculation Method

- A flow rate was chosen for one layer.
- The Reynold's number was calculated.
  - It should be less than 2000 for laminar flow and above 3000 for turbulent flow.
  - The transition region (from 2000 to 3000) should be avoided, since the flow regime (laminar or turbulent) and heat transfer depend on the detailed way in which flow was established.
- Flows in other layers were adjusted to obtain the same pressure drop.
- The net end-to-end pressure was checked to be sure it was small enough.
  - High pressure drop could lead to barrel motion in the Z-direction.
- Temperatures were checked.
- The process was iterated.



Silicon and Air Temperatures

SiD VTX Barrel.
0.13 W/cm^2

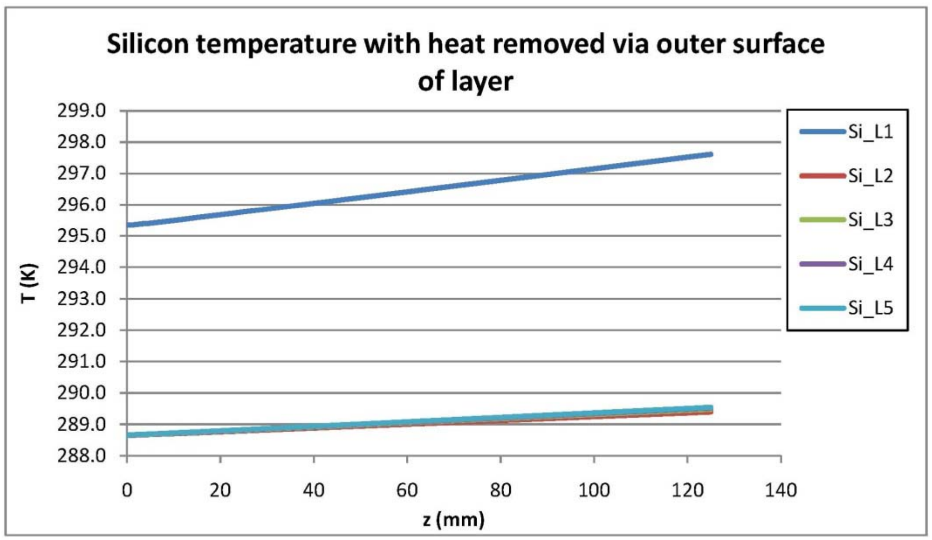
- Heat removal from one silicon surface (outer surface)

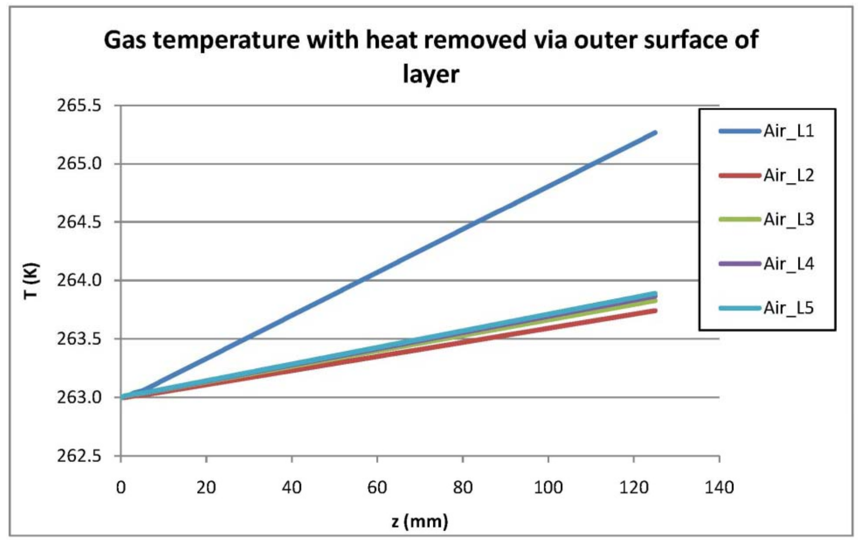
End-to-end pressure	7.72 Pa 0.00112 psi	SiD	0.13 W/cm^2 Heat removed via outer surfaces			
Gap	Flow g/s	Reynold's number	Flow velocity m/s	Heat removed W	Average T_silicon - T_gas K	T_rise of gas K
Beam pipe to L1	0.21	307	1.19	0.00		
L1 to L2	6.21	6766	6.04	14.37	32.35	2.30
L2 to L3	28.40	19719	9.43	21.52	25.65	0.75
L3 to L4	41.81	19719	9.43	34.79	25.65	0.83
L4 to L5	55.21	19719	9.43	48.06	25.65	0.87
L5 to outer shell	68.62	19719	9.43	61.34	25.65	0.89
Totals	200.46			180.08		

Initial air temperature was taken to be 263 K.

Silicon temperature is well above cooling air temperature.

L1 behaves differently from L2-L5 due to the smaller gap from L1 to L2.





Silicon and Air Temperatures

SiD VTX Barrel.
0.13 W/cm^2

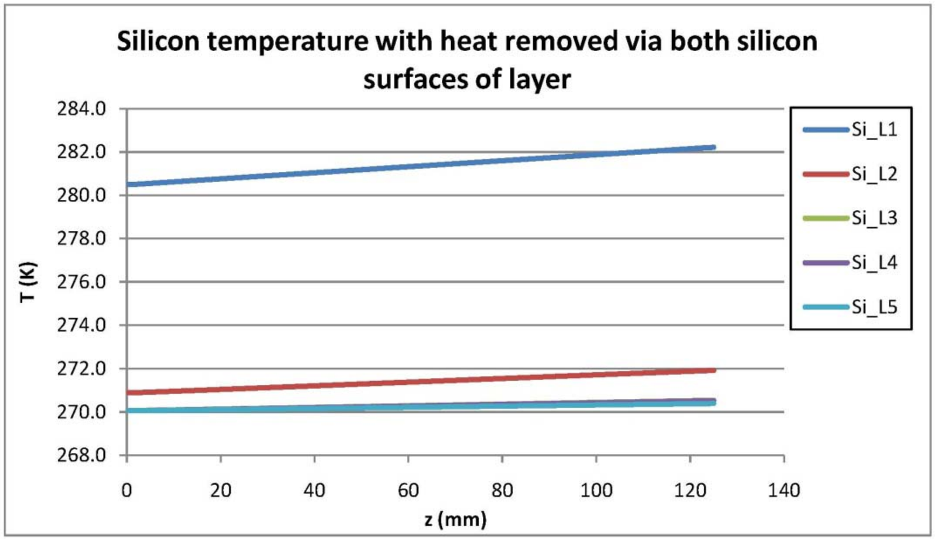
- Heat removal from both silicon surfaces

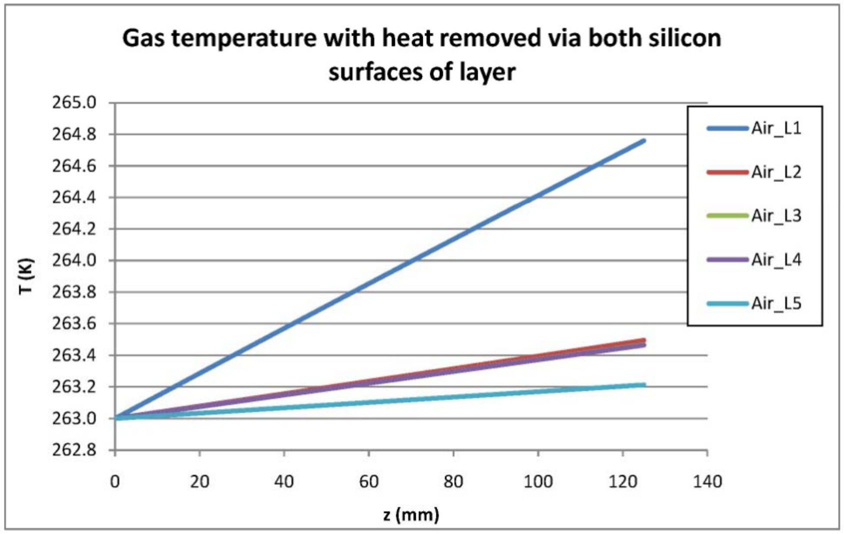
End-to-end pressure	7.72 Pa 0.00112 psi		SiD	0.13 W/cm^2 Heat removed via both surfaces		
Gap	Flow g/s	Reynold's number	Flow velocity m/s	Heat removed W	Average T_silicon - T_gas K	T_rise of gas K
Beam pipe to L1	0.21	307	1.19	0.19	15.95	0.87
L1 to L2	6.21	6766	6.04	27.15	15.03	2.73
L2 to L3	28.40	19719	9.43	25.98	10.18	0.71
L3 to L4	41.81	19719	9.43	41.39	12.81	0.85
L4 to L5	55.21	19719	9.43	54.44	12.83	0.87
L5 to outer shell	68.62	19719	9.43	30.94	12.94	0.45
Totals	200.46			180.08		

Higher cooling area leads to lower silicon temperatures.

Flow between the beam pipe and L1 is too low for significant heat removal.

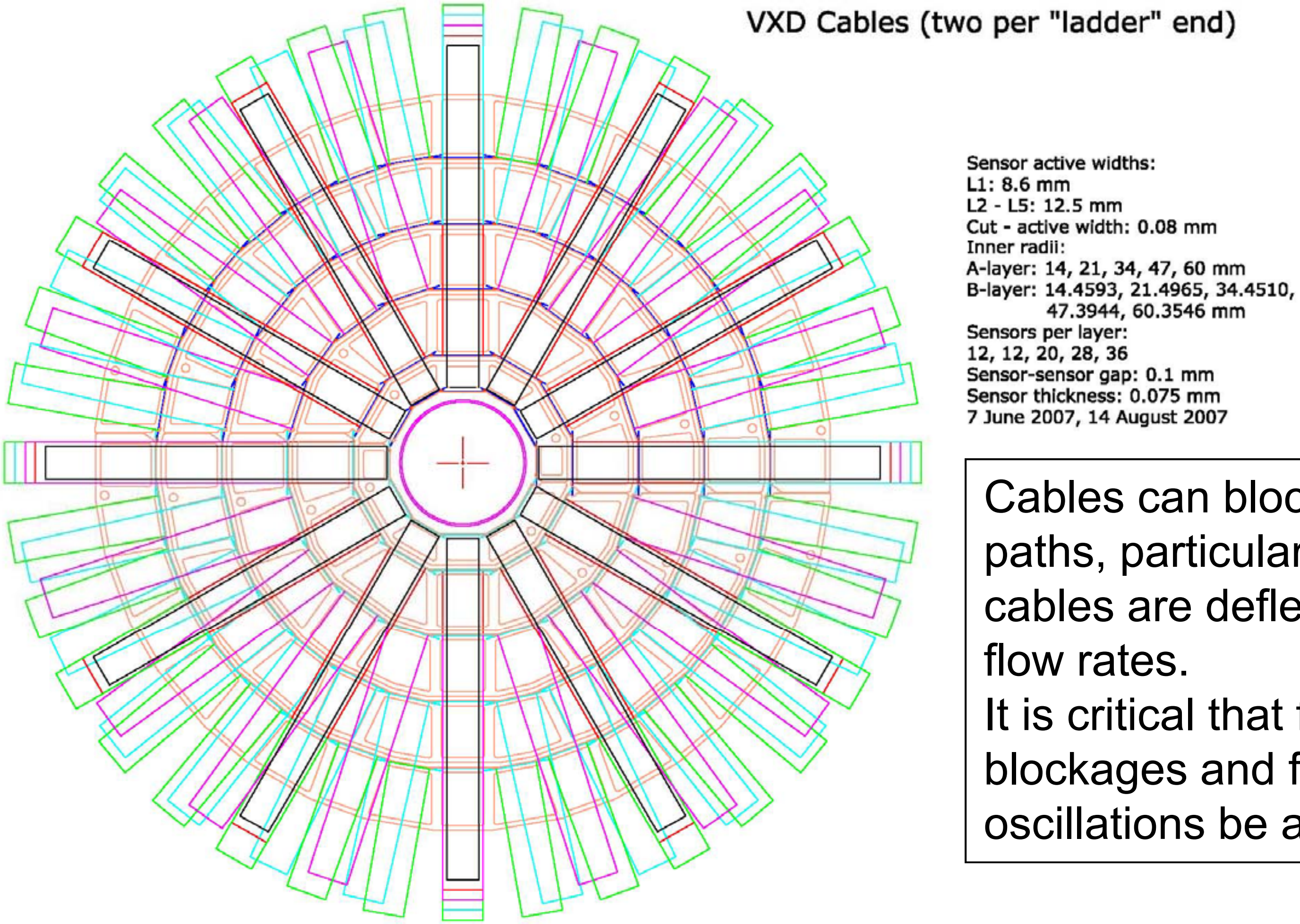
L1-L2 flow carries away most of L1 and a portion of L2 heat.





SiD Barrel End View with Cables

- Cable contributions to material are significant.
- The original goal of 0.1% X0 per layer did not include cables.



Cables can block air flow paths, particularly if the cables are deflected by high flow rates.
It is critical that flow blockages and flow oscillations be avoided.

Conclusions based on SiD

- For the same pressure drop, heat removal from both silicon surfaces leads to lower silicon temperatures.
  - Roughly a factor of 2 lower temperature difference from silicon to air, which is not surprising given that the heat removal area is doubled
  - Thermal conductivity of module backing materials should be carefully considered.
- The gap from the innermost silicon layer to the beam pipe is too small for significant flow. As a result, heat removal from the inner surface of that layer is minimal.
  - Cooling the beam pipe actively would help, but obviously adds material.
- An outer cylindrical shell is needed to guide flow outside Layer 5.
- We need to control the locations of cables.

Silicon and Air Temperatures

CLIC-SiD Barrel.
0.13 W/cm^2

- Heat removal from both silicon surfaces

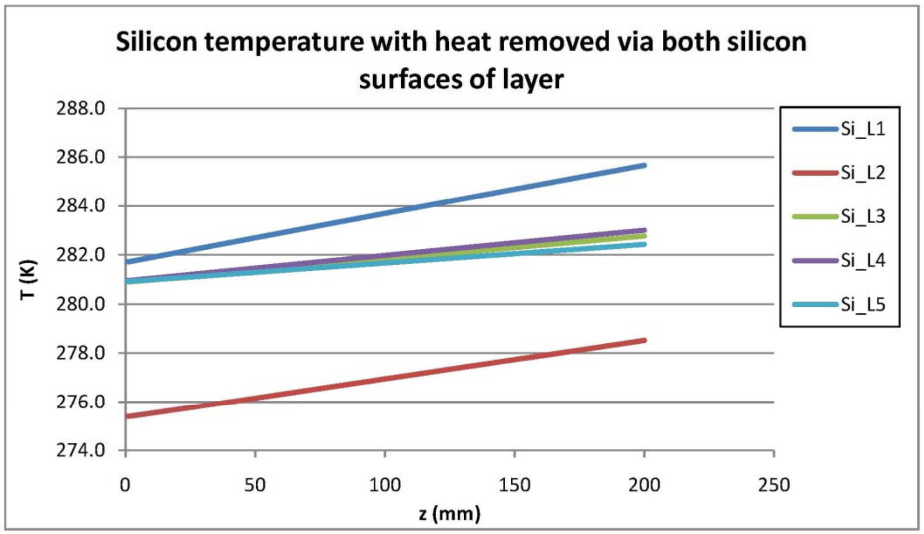
CLIC-SiD Barrel   Heat removed from both surfaces

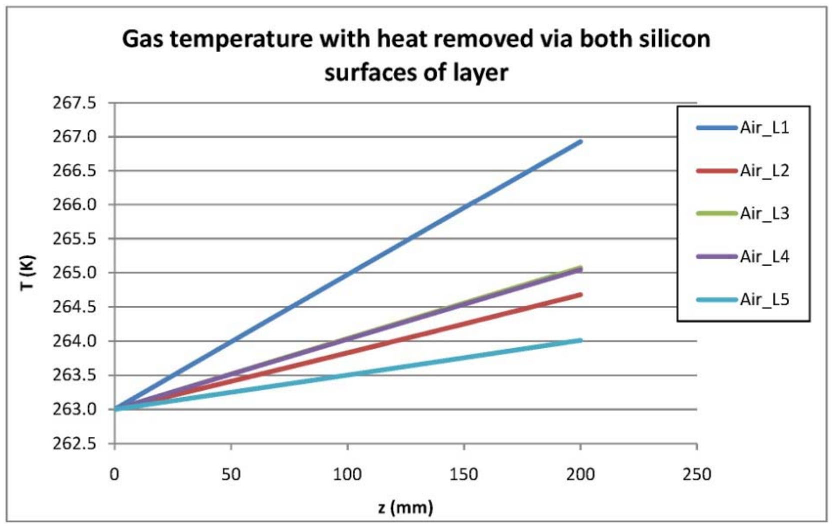
Gap	Flow g/s	Reynold's number	Flow velocity m/s	Heat removed W	Average T_silicon - T_gas K	T_rise of gas K
End-to-end pressure	5.77 Pa					
	0.00084 psi					
Beam pipe to L1	0.03	22	0.16	0.27	15.92	9.37
L1 to L2	15.77	9602	5.42	80.47	18.72	3.93
L2 to L3	30.00	13178	6.19	62.79	13.07	1.68
L3 to L4	42.74	14313	6.40	94.09	17.79	2.08
L4 to L5	47.11	12769	6.11	112.89	17.95	2.05
L5 to outer shell	63.77	14509	6.44	64.76	18.15	1.01
Totals	199.41			415.28		

Initial air temperature was taken to be 263 K.

Flow between the beam pipe and L1 is too low for significant heat removal.

L1 behaves differently from L2-L5 due to the smaller gaps to L2 & the beam pipe.





Silicon and Air Temperatures

CLIC-ILD Barrel.
0.13 W/cm^2

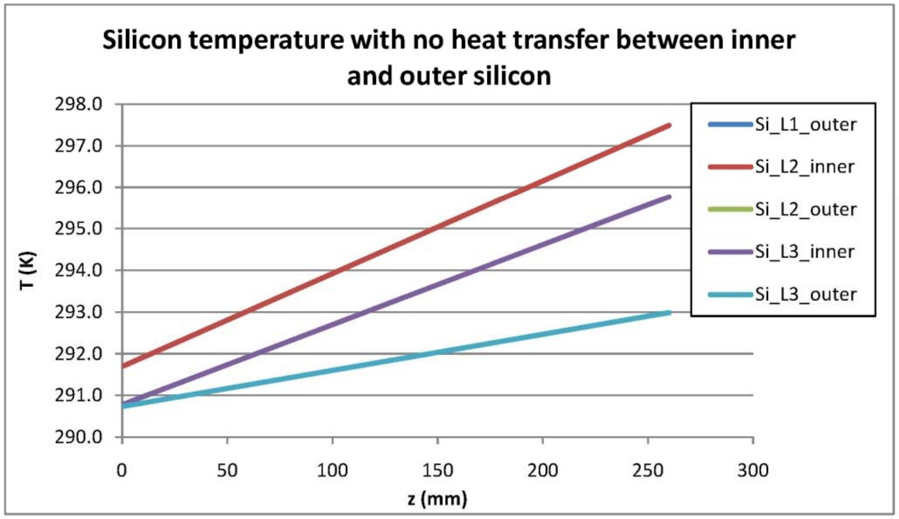
- Insulation between the 2 surfaces of a layer

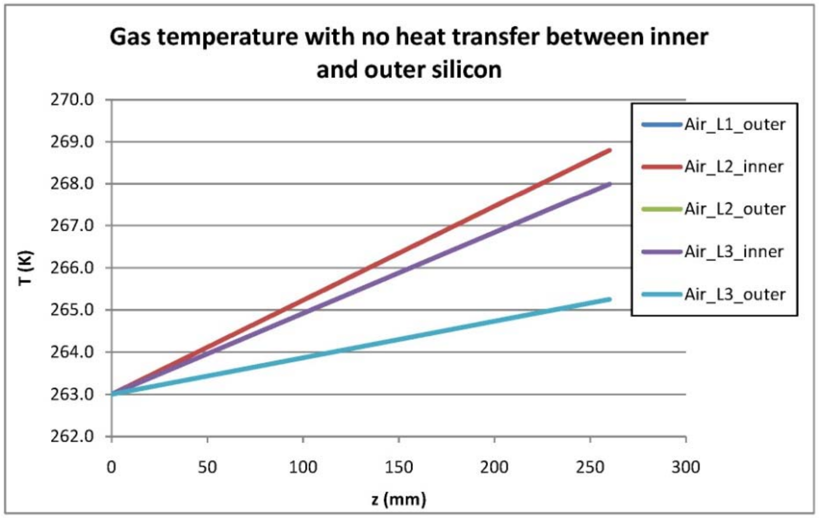
End-to-end pressure	14.38 Pa 0.00209 psi	CLIC-ILD Barrel Two surfaces thermally insulated				
Gap	Flow g/s	Reynold's number	Flow velocity m/s	Heat removed W	Average T_silicon - T_gas K	T_rise of gas K
Beam pipe to L1_inner	0.39	250	1.00	65.73	2858.16	165.52
L1_outer	28.04	13935	7.87	70.08	28.69	5.80
L2_inner	28.04	13935	7.87	93.34	28.69	5.80
L2_outer	44.00	16187	8.37	97.69	27.78	4.99
L3_inner	44.00	16187	8.37	123.07	27.78	4.99
L3_outer	56.27	16303	8.40	127.42	27.73	2.25
Totals	200.75			577.33		

L1 inner sensors cannot be adequately cooled if heat cannot be transferred outward, rather than inward.

The same issue can be expected in L1 of CLIC-SiD.

A higher total flow rate would give better cooling.





Silicon and Air Temperatures

- The bottom line is that, with air cooling, either power per unit area needs to be reduced, the gap from the beam pipe to L1 needs to be increased, or the support structure for L1 must have good thermal conductivity.
- Please note that turbulent flow is needed to provide adequate cooling with air.
  - That suggest vibration studies will be necessary
- Volumetric flow is high.
  - 200 g/s corresponds to 8.91 m^3/min. = 315 cfm.
- Disk cooling still needs attention.
- Options to air cooling include liquid cooling and two-phase cooling.
  - Micro-channel structures have been described in a recent CLIC WG4 meeting and appear promising.
    - http://indico.cern.ch/conferenceDisplay.py?confId=134712
  - Options carry a mass penalty, possibly less with micro-channels than, for example, evaporative CO2.
- We also need to consider coolant delivery paths and heat removal from power conditioners and cabling.

SiD VTX Cables

- Assumptions for sizing flat line cable conductor near the VTX:
  - Conductor = aluminum with resistivity = 2.8×10^{-6} Ω-cm.
  - Voltage input to the cable = 1.6 volts
  - Voltage delivered by the cable = 1.2 volts
  - Conductor length = 30 cm (one way)
  - No remote sensing; voltage drop in the cable is chosen to be large to minimize conductor mass; control of power pulsing is external to the sensor.
  - If portions of the sensor need to remain active between spills, those portions would be powered separately and are assumed to represent a small fraction of the total power.
- With those assumptions, we need to determine whether average power or peak power is more relevant to conductor sizing.
- With power ramped up, current = 4.06 W / 0.4 V = 10.15 A.
- Conductor resistance = 0.0394 Ω for 60 cm.
- Conductor cross-section = $60 \times 2.8 \times 10^{-6} / 0.0394 = 0.00426$ cm^2.
- For a width of 1 cm, conductor thickness = 0.00426 cm.

Conductor sizing – SiD VTX

- Two conductor layers represent ~0.10% X0
  - Comparable to the material budget of a VTX layer (0.1% to 0.2% X0), so cable contributions to the budget are significant.
- Conductor temperature rise in 200 ms / 80 = 2.5 ms:
  - Aluminum mass = 0.2556 cm^3 x 2.70 g/cm^3 = 0.690 g
  - Specific heat of aluminum = 0.91 j/(g-K)
  - So ΔT = 4.06 W x 0.0025 s / 0.91 j/(g-K) / 0.69 g = 0.0162 K.
- Since the temperature increase is small during the 2.5 ms, power removal can be reasonably averaged over the full cycle (200 ms).
- Average cable heat flux = 4.06 W / 80 / 60 cm / 1 cm = 0.00085 W/cm^2 (small compared to that of a sensor).
  - OK provided cables are not bundled too tightly.
- Coaxial cables can also be considered.
  - End connection methods would need to be developed.
  - Aluminum may be significantly more difficult than copper.
  - The resistance per unit length of the shield should be comparable to the resistance per unit length of the center conductor.

DC-DC Converters

- At least two efforts have been underway:
  - Katje Klein – CMS / RWTH Aachen
    - http://web.physik.rwth-aachen.de/~klein/
    - http://web.physik.rwth-aachen.de/~klein/1748-0221_5_07_C07009.pdf
    - http://web.physik.rwth-aachen.de/~klein/CR2010_043.pdf
    - http://indico.cern.ch/materialDisplay.py?contribId=2&sessionId=9&materialId=slides&confId=68677
  - Satish Dhawan – SiD / Yale University
    - http://shaktipower.sites.yale.edu/
    - http://shaktipower.sites.yale.edu/sites/default/files/IEEE_RT_Beijing_2009_TNS_Submission.pdf
    - http://shaktipower.sites.yale.edu/sites/default/files/Twepp_2009_Proceedings_Dhawan_0.pdf
- Circuit concepts are quite similar and are evolving.
- Component details differ.

DC-DC Converters

- Katje has sought to satisfy all CMS constraints.
  - Applicability to CLIC / ILC and power pulsing have not been specific goals.
  - One goal has been 2 A per module (higher for some applications) and 1.2 V output with a step down factor of ~8 and ~80% efficiency.
    - That efficiency has been difficult to achieve, particularly at higher step-down ratios and higher currents.
  - Though weights and several material thicknesses are given, I'm not aware of published values for the number of radiation lengths represented by prototypes.
    - An air-core inductor is assumed.

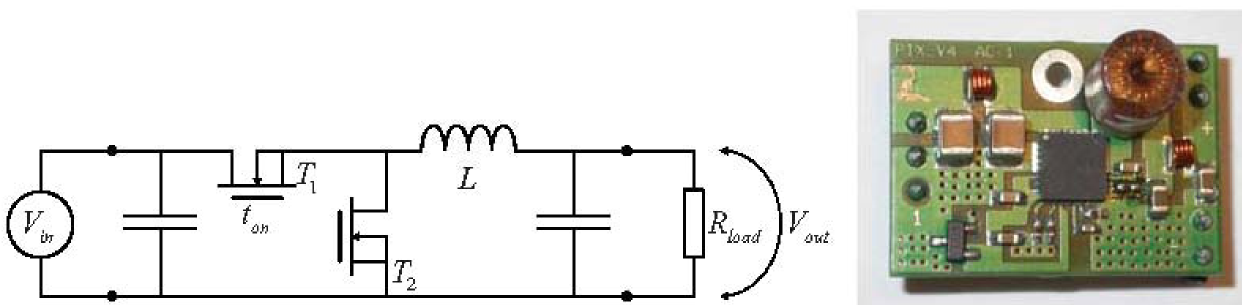


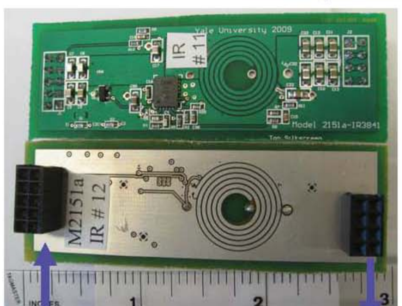
Figure 1. Schematic drawing of the basic circuit of a buck converter (left), and photograph of the 25 × 18 mm^2 AMIS2_PIX_V4 buck converter prototype (right).

DC-DC Converters

- Satish has concentrated on functionality with good results.
  - Reduction of mass has been kept in mind, but will be addressed later.
  - Air core inductor, radiation hard components, current delivery up to10 A at 1.2 V, ~80% efficiency with a voltage step-down factor of 8, larger step down factors are possible if radiation hardness is not so important
  - Cable testing with power pulsing is underway.
  - Vibration tests in a magnetic field are planned.

10 A max during testing

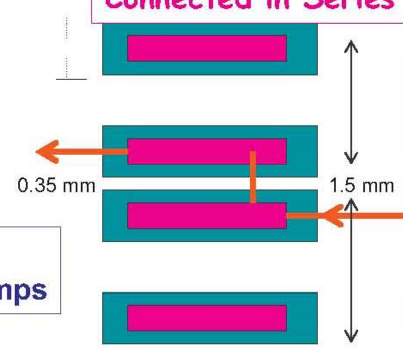
Plug In Card with Shielded Buck Inductor

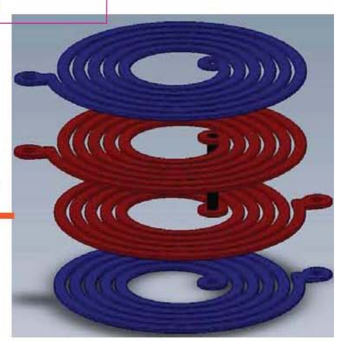


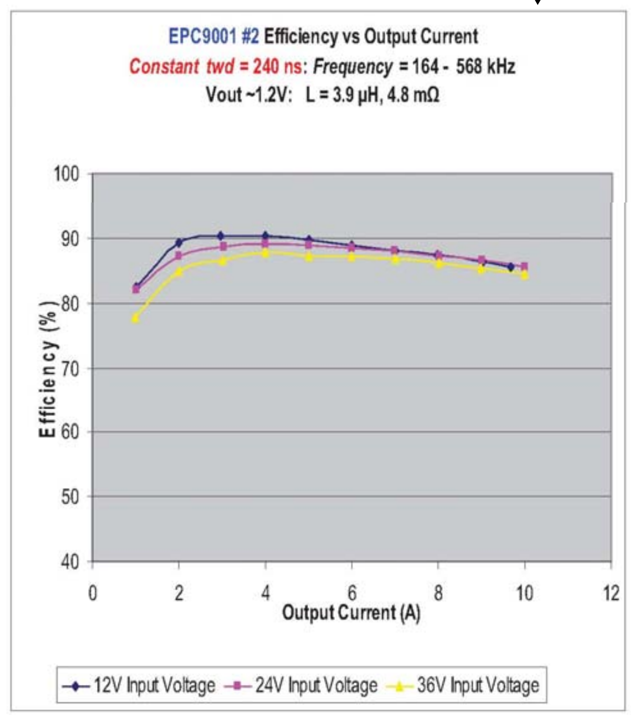
12 V

2.5 V
@ 6 amps

Coupled Air Core Inductor
Connected in Series







DC-DC Converters

- For the moment, assume performance similar to what Satish has achieved and a material budget of 3.5% X0 distributed over 4.5 cm^2.
- Please note that the 10 A maximum output current during Satish's testing was for steady-state operation.
- It matches the 10.15 A per cable with power ramped up.
- The simplest solution would be to provide one DC-DC converter per cable, that is, 432 converters (a lot!).
- With aluminum conductor and a kapton thickness = 0.005 cm, each cable represents approximately 0.113% X0 at normal incidence.
- Then, one converter board of average thickness 3.5% X0 would be equivalent to 3.5/0.113x4.5 cm = 139 cm of cable length.
  - That argues for increasing the length of converter output cables.
- We need reductions in board material and increases in board output current.
  - A reasonable goal might be 2% X0 or less over a region not more than 4.5 cm^2.
  - It possible, a converter should supply several cables.

DC-DC Converters

- It isn't obvious how pulsed power affects DC-DC converter performance.
  - It seems clear that output voltage and current can be ramped up and down in a straight-forward way.
  - It isn't at all clear how much the output current can be ramped up during a spill above the steady-state design value.
  - That is equivalent to making a study at higher currents of how efficiency falls off with current delivery.
  - The result directly impacts the number of cables a DC-DC converter can supply with pulsed power.

Power Delivery to SiD VTX Barrel

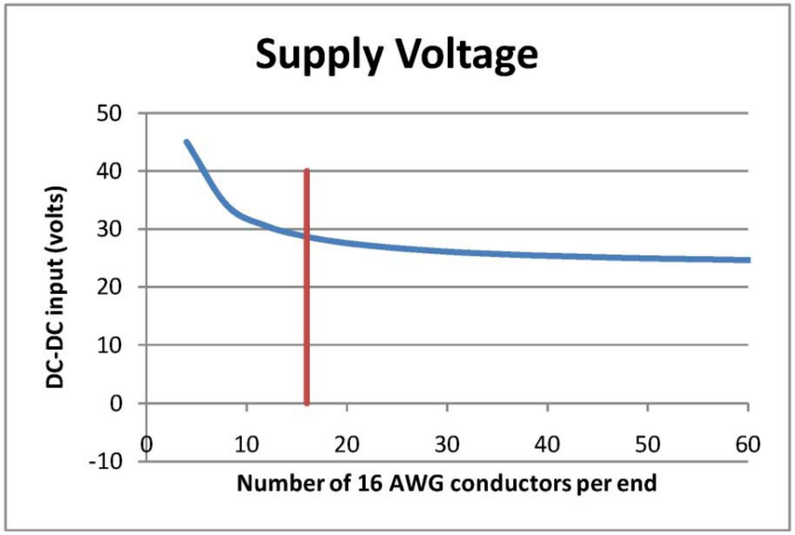
One end of VTX	Ramped up	Average		
P_barrel	7200	**90**	**watts**	
Pulsed power factor	80	80		
DC-DC converter out	2.9		volts	
Sensors	2.5		volts	
I_sensors	2880		amp	
P_cables	1152	**14.4**	**watts**	**VTX Region**
R_cables	0.000139		ohms	
P_total	8352	**104.4**	**watts**	
P_cables/P_total	0.138			
DC-DC converter eff.	0.8			
P_into_DC-DC	10440	**130.5**	**watts**	**1.45 P0**
Step-down ratio	8			
V_DC-DC_in	23.2		volts	
I_DC-DC_in	450		amp	
# conductors per end (supply + return)	18			
I_conductor	50		amp	
Conductor AWG	16			**Tracker region**
Conductor diameter	1.29032		mm	
R/L	13.17248		Ohms/km	
L	3		m	
R_conductor	0.03952		ohms	
P_cables	1778	**22.2**	**watts**	
V_cable	2.0		volts	
V_total	27.2		volts	
P_total	12218	**152.7**	**watts**	**1.70 P0**

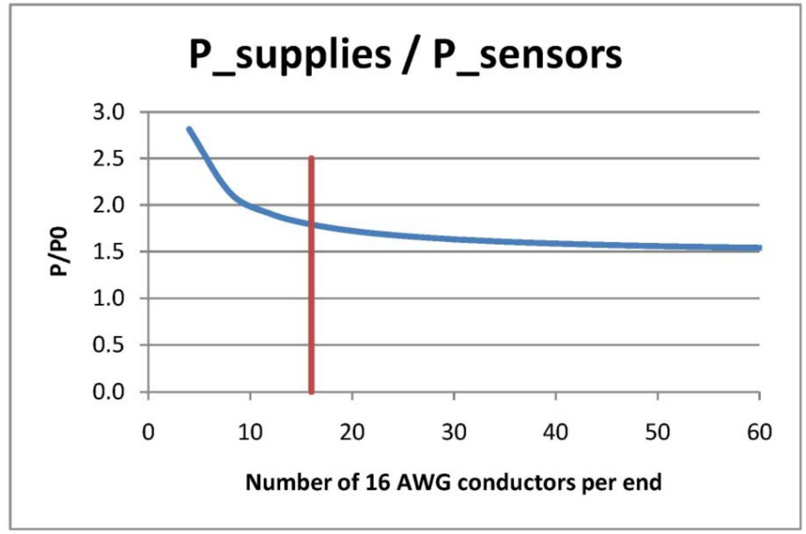
0.13 W/cm^2 sensor power dissipation

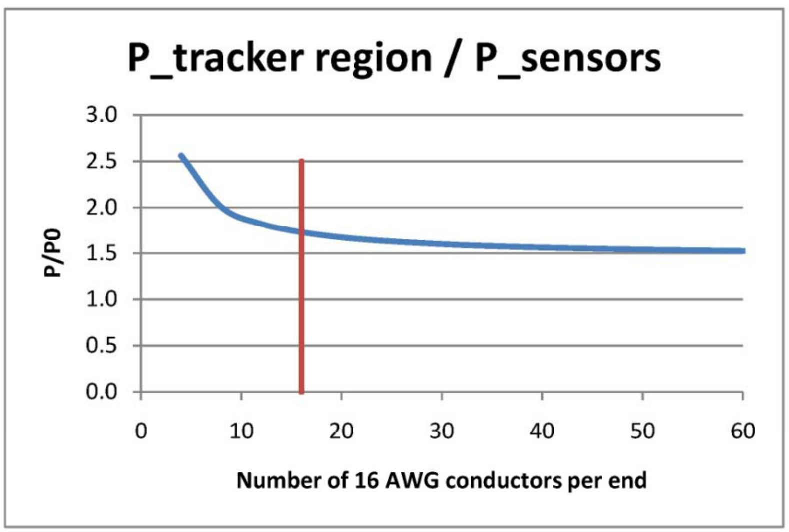
	Ramped up	Average		
# conductors per end (supply + return)	18			
I_conductor	50		amp	
Conductor AWG	6			
Conductor diameter	4.11		mm	**Calorimeter + Muon**
R/L	1.29593		Ohms/km	
L	7		m	
R_conductor	0.00907		ohms	
P_cables	408.2	**5.1**	**watts**	
V_cable	0.45		volts	
V_total	28.06		volts	
P_total	12627	**157.8**	**watts**	**1.75 P0**

Power Delivery to SiD VTX Barrel

- DC-DC converters are within the cooled silicon region.







P_VTX_region /P_sensors = 1.45

Power Delivery to VTX Disks

- The same power dissipation per unit area was assumed as for the barrels: 0.13 W/cm^2.
- Since pixel size might be lower for the outer three disks, final power dissipation might be significantly lower, 150 watts per end rather than the 340 watts per end which was assumed.

Disk	P W
1	21.9
2	21.9
3	21.3
4	21.3
5	108.8
6	88.5
7	55.7
Total per end	339.5
Total (2 ends)	679.0

Power Delivery to VTX Disks

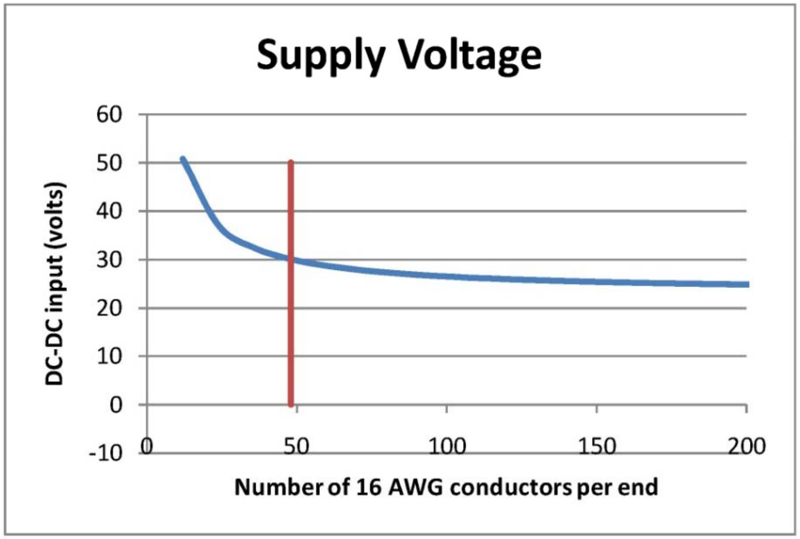
One end of VTX	Ramped up	Average		
P_disks	27200	**340**	**watts**	
Pulsed power factor	80	80		
DC-DC converter out	2.9		volts	
Sensors	2.5		volts	
I_sensors	10880		amp	
P_cables	4352	**54.4**	**watts**	**VTX Region**
R_cables	0.000037		ohms	
P_total	31552	**394.4**	**watts**	
P_cables/P_total	0.138	0.138		
DC-DC converter eff.	0.8			
P_into_DC-DC	39440	**493**	**watts**	**1.45 P0**
Step-down ratio	8			
V_DC-DC_in	23.2		volts	
I_DC-DC_in	1700		amp	
# conductors per end (supply + return)	48			
I_conductor	70.83333		amp	
Conductor AWG	16			**Tracker region**
Conductor diameter	1.29032		mm	
R/L	13.17248		Ohms/km	
L	3		m	
R_conductor	0.03952		ohms	
P_cables	9517	**119.0**	**watts**	
V_cable	2.8		volts	
V_total	28.8		volts	
P_total	48957	**612.0**	**watts**	**1.80 P0**

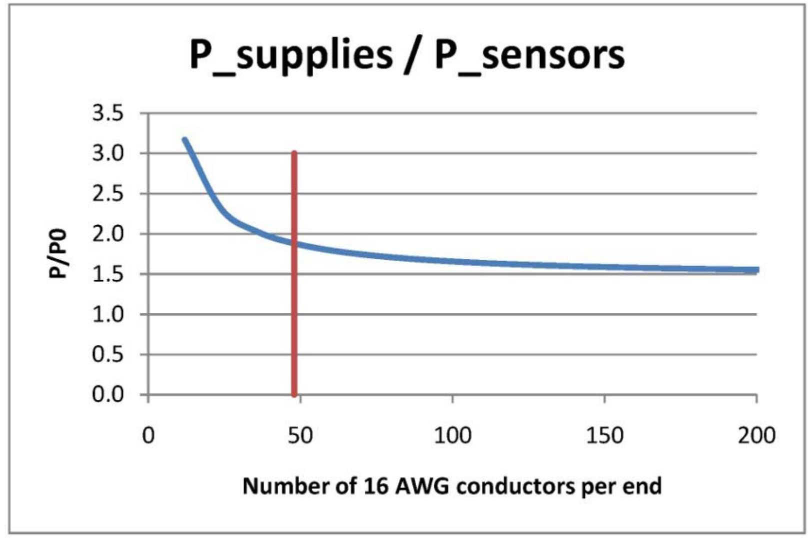
0.13 W/cm^2 sensor power dissipation

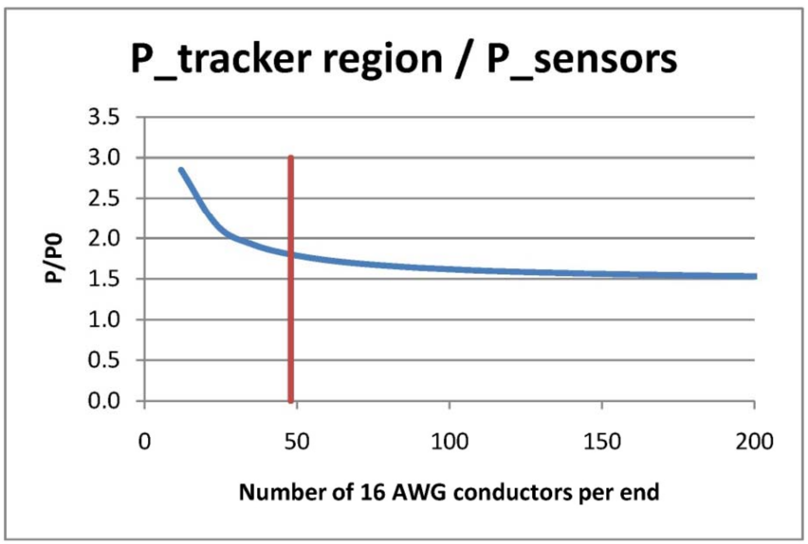
	Ramped up	Average		
# conductors per end (supply + return)	48			
I_conductor	70.83333		amp	
Conductor AWG	6			
Conductor diameter	4.11		mm	**Calorimeter + Muon**
R/L	1.29593		Ohms/km	
L	7		m	
R_conductor	0.00907		ohms	
P_cables	2184.7	**27.3**	**watts**	
V_cable	0.64256		volts	
V_total	30.08		volts	
P_total	51142	**639.3**	**watts**	**1.88 P0**

Power Delivery to VTX Disks

- DC-DC converters are within the cooled silicon region.







P_VTX_region /P_sensors = 1.45

In Conclusion

- Air cooling is pushed rather hard by power dissipation in the VTX barrel if power dissipation approaches 0.13 W/cm^2.
  - Layer 1 cooling needs attention and could be marginal..
  - We should understand how to cool the VTX disks.
  - We will need to investigate vibrations.
- The outer tracker presents its own issues.
  - Barrel air flow needs to be directed more effectively.
  - The disks need attention.
- Power cycling and DC-DC converters should work and appear to be necessary to meet the material budget.
  - DC-DC converters help with cable mass before the converter, but not with mass after it.
  - Serial powering is an option.
  - Optimizing the benefits of power pulsing should be part of DC-DC converter development for CLIC.
  - A proper trade-off between cable material and power conditioner material should guide the locations of power conditioners.
  - Systems should be designed with high reliability and fail-safe operation in mind.
  - Back-up systems, monitoring, alarms, and interlocks can help avoid damage.